the meter pointer away from zero. Now place a dial knob on VR6 spindle, without disturbing the potentiometer setting, and align so that the "0" division on the dial is vertical and opposite the pointer mark on the surface of the front panel. Tighten the dial knob grub screw.

Switch off S6 and replace the 0–1V meter with the 0–10V d.c. meter which has been chosen to serve as a voltage standard for the computer, while retaining the same meter lead polarity. Rotate VR6 dial until the "10" division is opposite its pointer, and switch on S6. Now adjust slider resistor VR1 from the back of the UNIT "A" box, for a precise reading of 10V on the "standard" meter. Repeat the above procedures for outputs VS2, VS3, VS4, and VS5, and remember to adjust only the particular slider (VR1–VR5) which is associated with the output being set up.

When all the voltage source dials are aligned, return to VS1 and make sure that its output is still +10V. Switch off S6, reverse the "standard" voltmeter leads, and set S1 for a negative output. Switch on S6 again and check the voltmeter reading; if it is not exactly 10V, go to the back of the UNIT "A" box and trim the power pack control VR2 (Fig. 3.4), this ensures that voltage source negative and positive outputs are equal.

SETTING UP THE COEFFICIENT POTENTIOMETERS

Insert a patching lead to link CP1/SK3 to CP1/SK4 (Fig. 2.7), and do the same for CP2, CP3, and CP4. Take a long patching lead from VS1/SK1 to CP1/SK1. Remove the dial from VR11 (Fig. 2.5) and rotate spindle fully clockwise. With the negative lead connected to any earth socket, insert the "standard" meter positive lead into CP1/SK2 after first setting S1 for a positive output. Adjust VS1 dial for a meter reading of 10V. Rotate CP1 spindle carefully anti-clockwise until the meter pointer just beings to drop below the 10V division. Replace CP1 dial knob on VR11 spindle, align the "10" division with the pointer, and tighten the grub screw. Repeat for CP2, CP3, CP4.

With a 10V input to CP1/SK1, and a 0–10V meter connected to CP1/SK2, it is a simple matter to check the agreement between dial divisions and voltage output from the coefficient potentiometer. If there are serious discrepancies between voltage output and dial reading this will indicate that the effective electrical rotation of the potentiometer differs from the 270 degree dial calibration. Errors can often be minimised by slight readjustment of the dial knob on its spindle, to spread the error over the entire scale. Generally

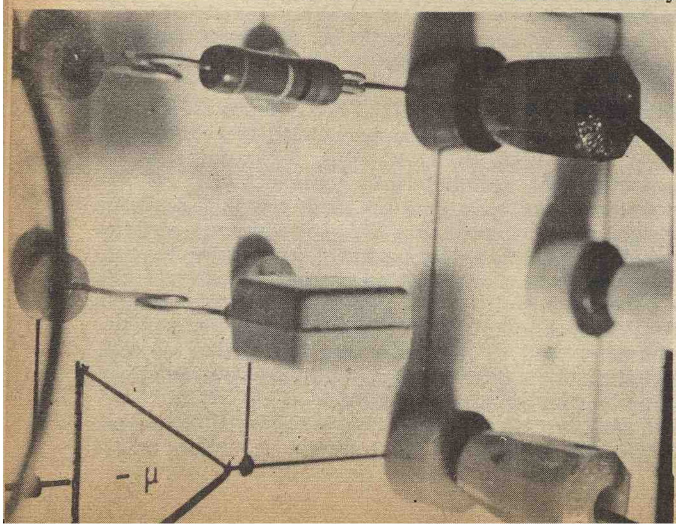

TABLE 4.1
SUGGESTED VALUES OF COMPUTING RESISTOR FOR STANDARD CLOSED-LOOP GAINS

Op-amp gain $\frac{R_f}{R_{in}} = -G$	All resistors ±2% unless otherwise stated: R_{in}	R_f
0·1	100kΩ	10kΩ
0·2	100kΩ	20kΩ
0·3	33kΩ	10kΩ
0·4	40kΩ ± 1%	10kΩ
0·5	20kΩ	10kΩ
0·6	33kΩ	20kΩ
0·7	13kΩ	9·1kΩ
0·8	20kΩ	16kΩ
0·9	20kΩ	18kΩ
1·0	10kΩ	10kΩ
	100kΩ	100kΩ
2·0	10kΩ	20kΩ
3·0	3·3kΩ	10kΩ
	33kΩ	100kΩ
4·0	4kΩ ± 1%	10kΩ
	40kΩ ± 1%	100kΩ
5·0	20kΩ	100kΩ
6·0	3·3kΩ	20kΩ
7·0	13kΩ	91kΩ
8·0	2kΩ	16kΩ
9·0	2kΩ	18kΩ
10·0	10kΩ	100kΩ
20·0	5kΩ ± 1%	100kΩ
30·0	3·3kΩ	100kΩ
40·0	4kΩ ± 1%	100kΩ
50·0	2kΩ	100kΩ

speaking, the dial setting error should not be worse than 5 per cent at all settings between "1" and "10" dial divisions. The whole question of computing potentiometer accuracy will be raised later, in connection with the Master Potentiometer of UNIT "B".

SETTING UP THE OPERATIONAL AMPLIFIERS

It is usual to check operational amplifiers either before the start of a computation, or at the beginning of the day, but the computer builder may wish to assure himself that his amplifiers are all that they should be when first brought into service. The zero-setting procedure given at the end of Part 3 of this series will have eliminated all but obscure faults. The front panel balance controls (VR15, VR16, and VR17, Figs. 2.4 and 2.9) are deliberately designed to have a limited range of adjustment, so that an amplifier fault will be clearly indicated as an inability to zero-set from the front panel.

To quickly check each amplifier, insert 10 kilohm feedback resistors into miniature sockets SK11 and SK12 for OA1, OA2, and OA3 (Fig. 2.9), and ensure that the operational amplifiers are already linked to their summing networks. Insert 10 kilohm input resistors into S1/I1/SK3–SK4, S2/I1/SK3–SK4, and S3/I1/SK3–SK4 (Fig. 2.8). Patch VS1/SK1 to S1/I1/SK1 (Figs. 2.6 and 2.8) and connect the negative lead of a voltmeter to OA1/SK13, with the positive lead going to any convenient earth socket.

Check that OA1 output is exactly zero when S6 is off. If not, zero-set by means of balance control VR15. Obtain a positive voltage from VS1 by switching on S6 and setting S1 and VR6, and monitor VS1 output with a second voltmeter connected to SN1/SK2 red, and an