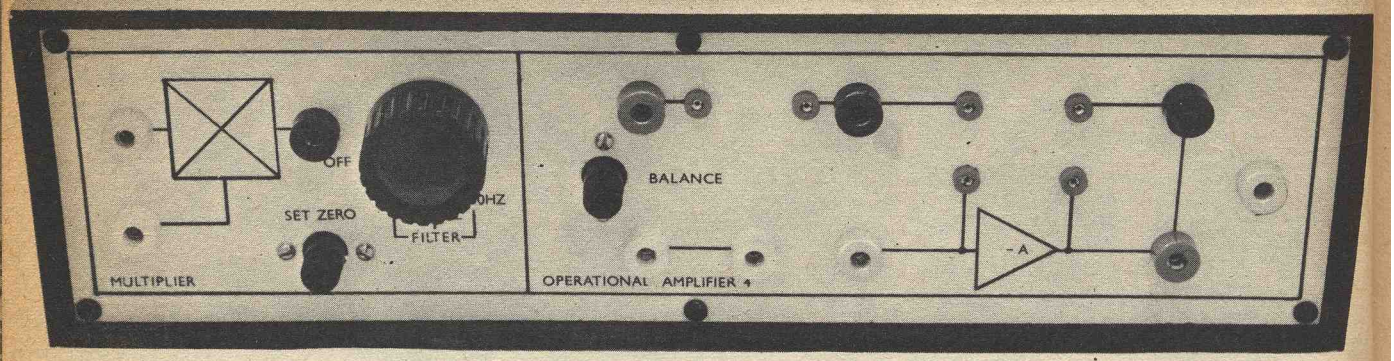

ANALOGUE COMPUTER PEAC

By D. BOLLEN

THIS month's article deals with UNIT "D"—the multiplier, which is the final piece of PEAC equipment. After a technical description, details of the construction and setting up are given.

The servo driven potentiometer has been widely employed in the past for multiplication of one variable voltage by another, but its frequency response, in most cases, is seldom better than 0–5Hz. Modern analogue computers now tend to use all solid-state multiplier circuits, which have a frequency response extending into the kHz region, but they are both complex and expensive. Taking the quarter-square multiplier as an example, it needs five operational amplifiers and two diode function generators to produce an accurate product voltage from two inputs. It follows, therefore, that analogue multiplier circuit design can be expected to present considerable difficulties when cost is an important consideration.

UNIT "D"—THE MULTIPLIER

Working on the premise that even a multiplier of restricted performance can make a worthwhile contribution to an analogue computer which lacks such a facility, an accuracy of $\pm 2{\cdot}5$ per cent and a frequency response of 50Hz under the most favourable conditions was considered to be an acceptable specification for the UNIT "D" multiplier. Although 0–50Hz seems rather limited by ordinary electronic standards, in the context of "parallel" computer circuit operation it represents a useful compute time which compares favourably with the servo multiplier.

UNIT "D" contains three distinct circuits, two operational amplifiers and a bistable reed relay driver. One of the amplifiers is identical to those used with UNIT "A", and is available as a multi-purpose operational amplifier when the multiplier is not in service.

TIME DIVISION

With the time division multiplier, a square wave is modulated in such a way that the mark/space ratio is proportional to one input voltage, while the amplitude of the waveform is proportional to another input voltage. The mean value of the resulting waveform is then proportional to the product of the two input voltages.

Looking at Fig. 9.1, which sets out the simplified multiplier circuit with associated waveforms, a voltage E_2 is compared with a fixed voltage E_3 at the input of the integrating amplifier. A bistable relay is arranged to switch S1 and S2 when the integrator output reaches a pre-determined value, conveniently about two thirds of the maximum available amplifier output swing. If the sign of E_3 at the S1 contacts is correct, the feedback will be positive, and a self-sustained oscillation at a frequency determined mainly by E_2 and C_f will result. When $E_2 = 0$ the output from the integrator will consist of a sawtooth or symmetrical ramp waveform, with identical rising and falling slopes, which is generated by E_3.

Assume now that a voltage E_2 is applied; this will be added to, or subtracted from E_3, depending on the position of the S1 switch. The ramp waveform is therefore modified to an asymmetric form where the rising and falling slopes become dependent on the level and sign of E_2.

Waveform (a) in Fig. 9.1 depicts the asymmetric ramp for $+E_2$ and $-E_2$, while waveform (b) shows the square wave generated by the switch, of mark/space dependent on the magnitude of E_2. As S2 is synchronised with S1, so the input resistor R1 will be alternately switched to the inverting and non-inverting inputs of the product amplifier, and will remain at each contact for a time dependent on the frequency and mark/space of the switching waveform.

The amplitude of the product amplifier output is