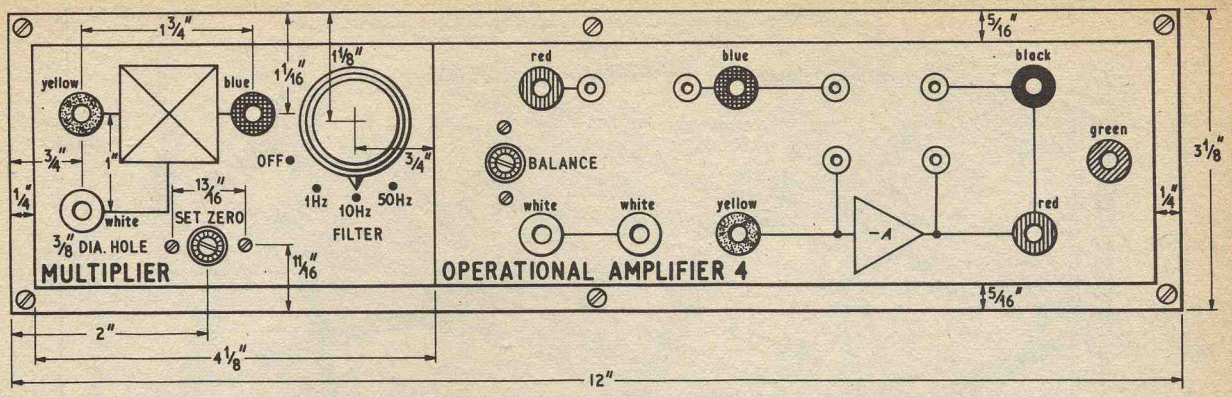


Fig. 9.3. Dimensions and engraving details for UNIT "D" front panel

UNIT "D" MULTIPLIER CIRCUIT

As the operational amplifier circuit has already been given in connection with UNIT "A", it appears in symbolised form only in the multiplier circuit of Fig. 9.2, with VR26 as the front panel balance control, and a fixed value of input resistor R12 provided internally for use with the multiplier. As the feedback capacitor C_f only affects the integrator waveform frequency, without altering other multiplier characteristics, it is useful to leave it as a plug-in component, so that the multiplier carrier frequency can be adjusted easily.

The output from the integrator, which it will be remembered from Fig. 9.1 carries information as to the magnitude and sign of input E_2, is fed via S11B to a diode resistor network composed of D1, D2, R15–R18, and VR2, the purpose of which is to allow the following bistable relay driver to be switched at precisely determined voltage levels. VR2 establishes the working point of the diode resistor network.

A conventional cross-coupled multivibrator is utilised as a relay driver, with reed coils RLA and RLB forming the respective collector loads of TR5 and TR6. D3 and D4 are used to ensure a "cleaner" switching action at high repetition rates, and the bistable circuit will function satisfactorily at frequencies in excess of 100Hz without undue relay contact bounce. The reference voltage, which was shown as $\pm E_3$ in Fig. 9.1, is extracted from a resistor network R23–R26 and VR25 in Fig. 9.2. VR25 allows positive and negative values of E_3 to be made equal. E_3 voltages are then fed, via RLA2 and RLB2 switches, and resistor R13, back to the summing junction of the integrator, thus completing the closed-loop to maintain oscillation.

SIGN CHANGE

The square wave switching cycle is presented to the input of the product amplifier by RLA1 and RLB1, with R14 acting as the input resistor. Changeover switch S12 is included to allow the sign of the multiplier output voltage to be changed to suit a particular problem set-up.

A product amplifier open-loop gain of about 1,000, which is the gain of the Fig. 9.2 circuit, is quite satisfactory for good accuracy when working with a fixed, closed-loop gain close to unity. Long-tailed pair TR1 and TR2 provide inverting and non-inverting inputs, while TR3 is the output transistor, and TR4 forms a constant current load for TR3, in place of a fixed resistor, thus enabling larger loads to be driven without excessive dissipation. VR1 serves to zero the amplifier output.

The ratio of resistors R7 and R14 gives a product amplifier gain (closed-loop) of 1·1, while R13/R12 yields an equivalent gain for the integrating amplifier of 0·91. The lower value of gain for the integrator enables E_2 to equal E_3 without stopping the integration cycle, and yet the overall gain of the multiplier is still unity because $1{\cdot}1 \times 0{\cdot}91 = 1$.

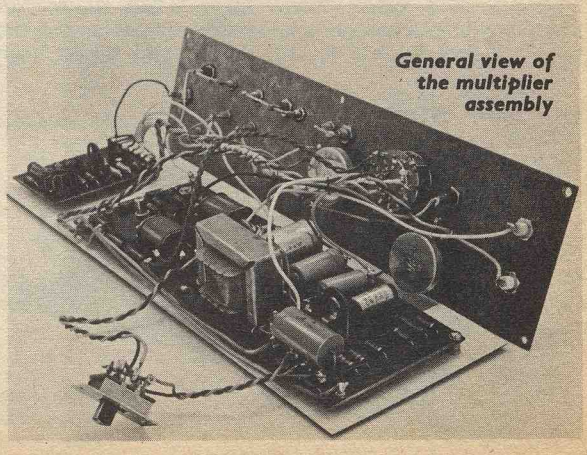
FILTER CIRCUIT

The purpose of the filter circuit L1, C2–C5, R6, and S11A, is to remove the square wave carrier without distorting the product waveform when input voltages are time varying. Bearing in mind that computer waveforms are extremely diverse, it is almost impossible to achieve near perfect results with one filter circuit, especially when the carrier frequency is not far removed from input frequencies. To allow compromise, therefore, the cut-off frequency of the Fig. 9.2 filter can be set by switch S11A to suit the circumstances of a particular problem set-up.

The three switch positions, 1Hz, 10Hz, and 50Hz, represent approximately the roll-off points given by the filter, and the bandwidth handled by the multiplier. In the 1Hz position the filter will virtually eliminate carrier ripple when input voltages are of very low frequency, but the 50Hz setting is used with fast integrator waveform inputs, where ripple may be less objectionable.

CONSTRUCTION OF UNIT "D" FRONT PANEL AND BOX

Details of the UNIT "D" front panel and box appear in Fig. 9.3 and Fig. 9.4. Note that the operational amplifier (OA4) socket positions and panel markings



General view of the multiplier assembly