DRAWING NO.	REV.NO.	PPS.	DESCRIPTION
A-SP-MAA5315	A	3	DL11-C,D,E ASYNC INTERFACE
A-SP-MAA5320	B	3	DLV11 SLU FOR 11/03
A-SP-MAA5321	A	12	DLV11-E ASYN INT.W/MODEM CTL.
A-SP-MAA5322	A	12	DLV11-F ASYN .LN.INT.W/20 MA.
A-SP-MAA5324	C	16	DLV11-J 4-LINE SERIAL INTERFACE
A-SP-MAA5330	B	12	DL11-W SLU/RT CLOCK OPT.
A-SP-MAA5510	A	3	KW11-L
A-SP-MAA5520	A	3	KW11-P PROG. CLOCK
A-SP-MAA5530	A	3	KW11-W WATCH DOG TIMER
A-SP-MAA5540	A	3	KW11-K DUAL PROG CLOCK
A-SP-MAA5550	B	4	KWV11-A
A-SP-MAA6110	A	2	AA11 D/A CONVERTER
A-SP-MAA6115	A	3	AAV11-A 4 CH 12 BIT D/A
A-SP-MAA6120	A	2	AD01-D A/D CONVERTER
A-SP-MAA6124	A	14	LPA11-K A/D CONVERTER
A-SP-MAA6125	A	4	AD11-K A/D CONVERTER
A-SP-MAA6126	A	4	AA11-K D/A CONVERTER
A-SP-MAA6127	A	4	AM11-K MULTIPLEXER EXP
A-SP-MAA6130	A	2	LPS-11 SYSTEM
A-SP-MAA6135	A	4	16 CH 12 BIT A/D FOR 11/03
A-SP-MAA6154	A	9	IB11
A-SP-MAA6160	C	16	ICS-11 SYSTEM INTEG.
A-SP-MAA6165	B	23	ICR-11 SUBSYSTEM
A-SP-MAA6170	A	21	DPM23
A-SP-MAA6175	B	7	ISB-11 DEC DATAWAY CONTR.
A-SP-MAA6176	C	24	DPM50 DIST I/O SUBSYSTEM
A-SP-MAA6180	A	2	AR11 SYSTEM
A-SP-MAA6190	A	2	NC11 GAMMA CAMERA
A-SP-MAA6192	A	6	NCV11 GAMMERA CAMERA INTERFACE
A-SP-MAA6205	A	4	DR11-A GENERAL DEVICE
A-SP-MAA6210	A	4	DR11-B DMA DEVICE
A-SP-MAA6220	A	4	DR11-C GENERAL DEVICE
A-SP-MAA6225	A	3	DRV11 16 BIT PLU-PDP11/03
A-SP-MAA6230	A	2	DT03 BUS SWITCH
A-SP-MAA6240	A	2	DA11-BD UNIBUS WINDOW
A-SP-MAA6260	A	4	DR11-K GENERAL I/O
A-SP-MAA6275	A	5	DR11-W GENERAL PURPOSE (DMA)
A-SP-MAA7110	A	2	BD03 A CII/BINARY
A-SP-MAA7120	A	2	BD04 DISK INT ALARM
A-SP-MAA7130	A	2	BD05 LINE CONTROL
A-SP-MAA7210	A	2	REORDER TRAP DEVICE
A-SP-MAA7510	C	14	LPD-11/LPC01 INTFRFACE

A53915

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DL11-C, D, E ASYNCHRONOUS INTERFACE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5315					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Jeleniewski	Tom	A	SP	MAA5315-0-0	A

MANUFACTURING SPECIFICATION

TITLE MODULAR APPROACH TO SYSTEMS TEST - APPENDIX A

DL11-C,D,E ASYNCHRONOUS INTERFACE

1.0 ABSTRACT

The following describes the system test procedure for the DL11-C through DL11-E. Basically, a "finished" DL11 is taken from the stockroom consisting of an M7800 module and cable. According to customer specification, jumpers must be cut on the M7800 to select data format, the proper crystal must be installed, and address and vectors must be assigned. Details of this process are described in A-SP-DL11-0-2 "Installation Procedure".

2.0 REQUIREMENTS

The minimum equipment requirements are:

A. PDP-11 with 4K of core memory.

B. DL11 interface and associated cabling.

C. Some type of terminal.

3.0 REFERENCE DOCUMENTS

MANUALS:	EK-DL11-TM-003 DL11 Eng. Drawings or later Rev. B-DD-DL11-0
CHECKOUT & ACCEPTANCE PROCEDURES:	A-SP-DL11-0-3
INSTALLATION PROCEDURE:	A-SP-DL11-0-2

MAINDEC LISTINGS:

DZKLA	TELETYPE TEST
DZDLA	DL11-E/C/D OFF-LINE TEST
DZDLA	DL11-E ON-LINE TEST
DZVTB	VT05 DISPLAY TERM. TEST
DZLAC	LA36 DIAGNOSTIC
DZVTC	VT50 DISPLAY TERM. TEST

4.0 TEST PROCEDURE

The normal test procedure is to run DL11 attached to the customer ordered DEC terminal such as LA30, VT05, LT33, LT35, or LA36. Refer to Section 3.0 for the appropriate MAINDEC number.

If the customer has not ordered a DL11 + terminal combination, then the DL11 should be attached to a VT05, if compatible. Any DL11 is "VT05 Compatible" if the DL11 conforms to the following format:

a. 8 data bits;
b. 1 or 2 stop bits;
c. parity off;
d. baud rate: 110, 150, 300, 600, 1200, 2400, 2400/150, 1200/150;
e. EIA or current loop.

The jumpers on the M7800 should not be altered to conform to the above list; however, the baud rate should be adjusted by switch - as long as it is within the range of the cyrstal - in order to conform to a VT05 speed.

If the DL11 is neither a DL11 + terminal combination nor "VT05 Compatible", then only an off-line maintenance test can be used.

Details of the test procedure follow:

DL11-C,D,E:

First run DZDLA Off-Line Test, Program 0, for 2 complete passes DL11-E's must be run with H315 connector. Then run the first applicable method below:

1. DL11 + DEC terminal: run appropriate terminal test. See MAINDEC write-up for procedure.

2. Attach to VT05 if "VT05 Compatible" and run DZVTB, Program 2, "Keyboard Test".

3. If neither 1 or 2 applies, no further testing can be done for DL11-C's and E's. For DL11-D's jumper pins 2 and 3 on EIA connector and run DZDLA, Program 0, Test 56.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DLV11 SERIAL LINE UNIT FOR PDP-11/03 - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	Prev. 7668001-0-5320					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelenkiewski	Tom Jelenkiewski	A	SP	MAA5320-0-0	B

DLV11 SERIAL LINE UNIT FOR PDP-11/Ø3

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic write ups for the purpose of expediency. The procedure has been kept brief, and to the point, to keep from confusing the user. For additional information, it will be necessary to refer to the diagnostic write up.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD 116)

2.2 11/0J Printset

2.3 LSI11 PDP 11/03 Configuration and Installation Guide EK LSI11-IN-001

2.4 LSI11 PDP 11/03 Users Manual EK LSI11-TM-002

2.5 DLV11 Engineering Specifications A-SP-DLV11-0-0

2.6 Microcomputer Handbook

3.0 REQUIRED TEST EQUIPMENT

3.1 DLV11 module

3.2 Wraparound test connecter

3.3 Output terminal

3.4 LSI-11 standard computer

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC 11-DVKAE DLV11 Test Diagnostic and Writeup

4.2 MAINDEC 11-DXDLA DEC/X11 Exerciser and Writeup

5.0 SPECIAL INSTRUCTIONS AND CHECKS

5.1 Insure wraparound connecter is installed to run DECX11.

6.0 TEST SETUP

6.1 Set up jumpers for address, vector, baud rate as required.

6.2 Remove capacitor C44 .005UF if serial line device is not a tele-typewriter.

6.3 Install appropriate cable in J1 of module A-EIA interface BC05C-X modem cable B-20MA current loop - BC05M-X cable assy.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 DLV11 Test (DVKAE)

7.1.1 Load program through appropriate load media.

7.1.2 Program starting address

7.1.2.1 Load address 200
7.1.2.2 Start 000000, software SR default value (1000 for wrap test) or on alternate setting (see 7.1.3)

7.1.3 Alternate software SR settings (loc 122)

7.1.3.1 SW 15 = 1 Continue on error
7.1.3.2 SW 14 = 1 Loop on error
7.1.3.3 SW 10 = 1 Loop on test
7.1.3.4 SW 9 = 1 Run wrap test

7.1.4 Testing other than console DLV11's

Supply correct address and vector to the following locations:

7.1.4.1 Loc 220 - Address of receiver CSR
7.1.4.2 Loc 222 - Address of receiver buffer
7.1.4.3 Loc 224 - Address of transmitter CSR
7.1.4.4 Loc 226 - Address of transmitter buffer
7.1.4.5 Loc 230 - Address of receiver vector
7.1.4.6 Loc 232 - Address of associated PSW
7.1.4.7 Loc 234 - Address of transmitter vector
7.1.4.8 Loc 236 - Address of associated PSW

7.1.5 Operator Action

7.1.5.1 Install test connector in J1
7.1.5.2 Type ?00G

7.1.6 Evidence of End of Pass andRun Time

7.1.6.1 Program will print "END OF PASS" time dependent on baud rate.

7.1.7 Acceptable errors:

None

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DLV11-E ASYNCHRONOUS SINGLE SERIAL LINE INTERFACE WITH MODEM

REVISIONS APPENDIX A CONTROL

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5321					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelenkewski		A	SP	MAA5321-0-0	A

DLV11-E ASYNCHRONOUS SINGLE SERIAL LINE INTERFACE WITH MODEM CONTROL

INTRODUCTION

This procedure establishes the minimum test and electrical standards that a DLV11-E must meet to be considered acceptable for customer shipment.

DESCRIPTION

The DL..1-E is an asynchronous line interface module that interfaces the LSI-11 bus to a serial communications line. The DLV11-E receives serial data from a peripheral device and assembles it into parallel data for the LSI-11 Bus. In turn, the parallel data from the LSI-11 Bus is converted into serial data and is transmitted to a peripheral device. The DLV11-E is unique from other DLV11s in that it offers full modem control.

Option	Qty/Contents	Description
DLV11-E	1 - M8017	Module
	1 - H315	Modem Test Conn.

1.0 REFERENCE DOCUMENTATION

1.1 Print Set MP00460

1.2 Technical Manual EK-DLV11-TM-(Rev)

1.3 Users Guide E[illegible]-DLV11-OP-(Rev)

1.4 Lib Kit Z[illegible]-243-RB

1.5 Ship List A-PL-DLV11-E

1.6 Packaging Inst. A-SP-3700297-40-0

2.0 REQUIRED TEST EQUIPMENT

2.1 PDP 11/03 with a minimum of 4K of memory and one available slot.

2.2 Scope: 465 or equivalent.

2.3 For power requirements, refer to Section 6.0.

2.4 Wire wrap gun (OK Speed Wrap Model #BW-515BF) or equivalent.

2.5 Unwrapping tool - hand type, unwraping tool.

2.6 Cable: (BC01V-X or BC05C-X) or turnaround connector. See page 10 for directions on making a turn around connector that will plug into the module.

3.0 AVAILABLE DIAGNOSTIC PROGRAMS

3.1 Kit # ZJ-243-RB

CVDVA - DLV11-E Off Line Tests paper tape and document

3.2 DECX11

DXDLA-H - DLV11 DECX11 Exerciser (Rev H or higher only)

4.0 INSTALLATION INSTRUCTIONS

4.1 If the DLV11-E is being tested as an option add-on, it is not necessary to change configured jumpers. See tables 4.1.1 and 4.1.2 for shipped configuration.

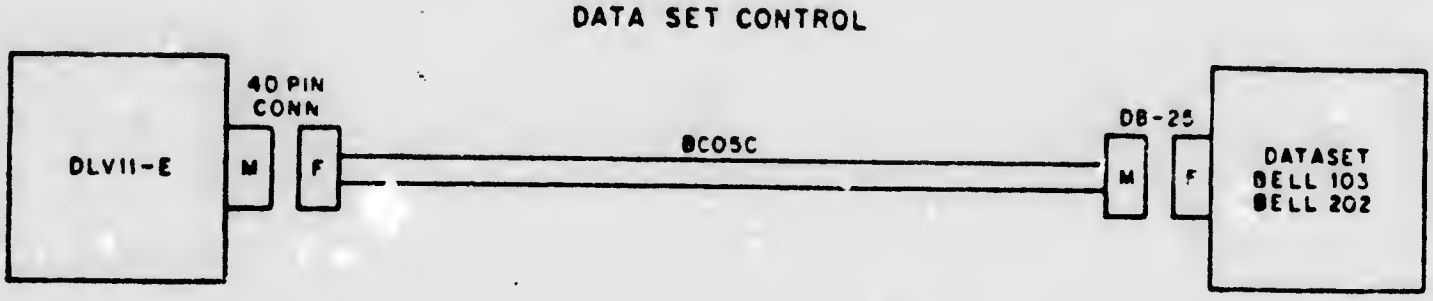
4.2 When being installed in a customer system, it may be necessary to change the jumpers as they are shipped. When configuring, refer to tables 4.1.1 and 4.1.2 for proper installation.

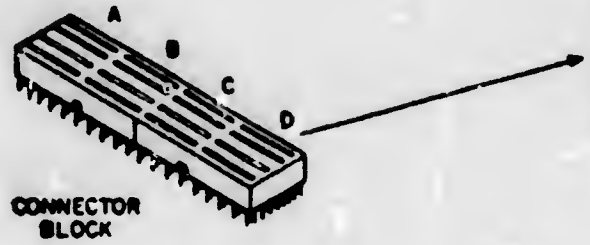
4.3 CAUTION #1 - When changing wire wrapings, always use equipment designed for that purpose, and calibrated. Note Sections 2.4 and 2.5 for type of equipment.

4.4 CAUTION #2 - All wire wraping must be done to Digital's workmanship standard; DEC Std 116. Reference should be made to Section 3. in that text.

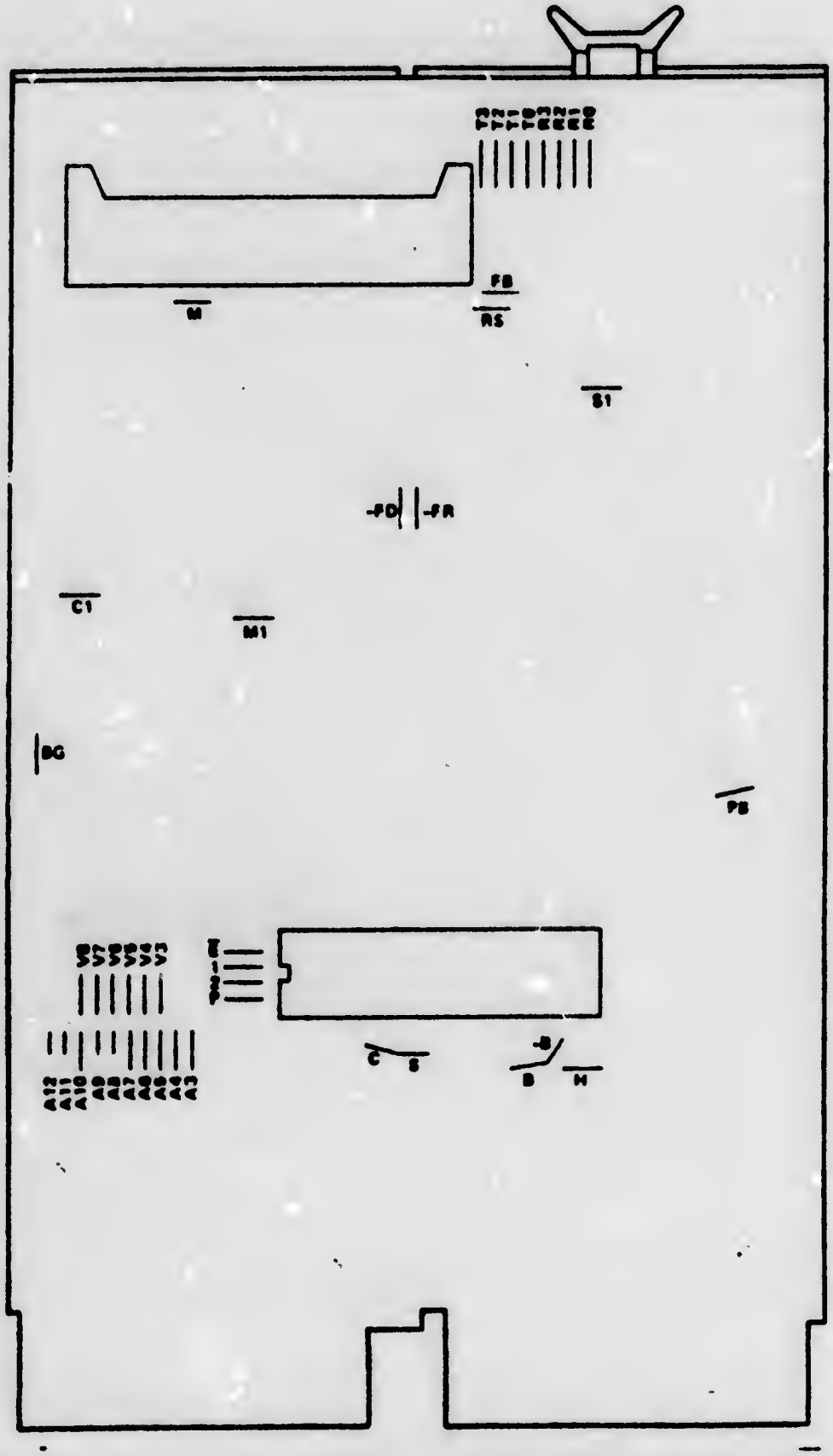
4.5 CAUTION #3 - All wire wraping should be done by a qualified person. Mistakes may cause damage to the wire wrap pin or printed circuit board.

4.6 The DLV11-E can be installed in any slot of the LSI-11 Backplane, except the first 4 slots that are reserved for the LSI-11 processor modules. When installing the DLV11-E, do not leave any open slots between the process modules and the DLV11-E. Note that priority for each option is determined by how close that option is installed to the processor modules. The closer to the processor you get, the higher priority the option has. A picture of a typical configuration is shown below:





4.1.1 DLV11-E Jumper Locations



4.1.2 Jumper Definitions

I = Jumper inserted = program bit cleared

R = Jumper removed = program bit set

NOTE: Jumpers are inserted to enable the function they control except for those jumpers that indicate negation (such as "-B") Negated jumpers are removed to enable the functions they control.

Jumper	Jumpers Installed when ship'd from Vol. Mfg.	Function
A3-A12		These jumpers correspond to bits 3-12 of the address word. When inserted, they will cause the bus interface to check for a True condition on the corresponding address bit.
A3	I	Jumpers A3 through A12 implement device address 17561X for the DLV11-E. The least significant octal digit is hard-wired on the module to address the four device registers as follows: X = 0 RCSR X = 2 RBUF X = 4 XCSR X = 6 XBUF
A4	R	
A5	R	
A6	R	
A7	I	
A8	I	
A9	I	
A10	R	
A11	I	
A12	I	
V3-V8		Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector address bit on the LSI-11 bus.
V3	R	This jumper selection implements interrupt vector address 300₈ for receiver interrupts and 304₈ for transmitter interrupts on the DLV11-E.
V4	R	
V5	R	
V6	I	
V7	I	
V8	R	

Jumper	Jumpers installed when ship'd from Vol. Mfg.	Function
R0 R1 R2 R3	I R I I	The module is configured to receive at 110 baud. Receiver and transmitter baud rate select jumpers, during common speed operation. See table 4.1.3
T0 T1 T2 T3	I R R R	The transmitter is configured for 9600 baud if split speed operation is used. Transmitter baud rate select jumpers during split spped operation. See table 4.1.3
BG	I	Jumper is inserted to enable Break generation.
P	R	Jumper is inserted for operation with parity.
E	R	Removed for even parity; inserted for odd parity. Receiver checks for appropriate parity and transmitter inserts appropriate parity.
1,2	R,R	These jumpers select the desired number of data bits (see Table 4.1.4)
PB	R	Jumper is inserted to enable the programmable baud rate capability.
C,C1	I,I	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted)
S,S1	R,R	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	R	This jumper is inserted to assert BHALT L when a framing error is received. This places the LSI-11 in the halt mode.

Jumper	Jumpers installed when ship'd	Function
B	R	Jumper B is inserted to negate BDCOK H when a BREAK signal or framing error is received. This causes the LSI-11 to reload the bootstrap. (Jumper -B must be removed when B is inserted.)
-B	I	
-FD	I	Jumper is removed to free DATA TERMINAL READY signal on.
-FR	I	Jumper is removed to force REQUEST TO SEND signal on.
RS	I	This jumper is inserted to enable normal transmission of the REQUEST TO SEND signal.
FB	R	Inserted to enable transmi ion of the FORCE BUSY signal (for Bell model 103E data sets)
M,M1	R,R	These are test jumpers used during the manufacture of the module. They are not defined for field use.

Table 4.1.3

Baud Rate Selections

	Bit	Bit	Bit	Bit	Bit	
Program Control	15	14	13	12	11*	
Receive Jumpers	R3	R2	R1	R0		Baud
Transmit Jumpers	T3	T2	T1	T0		Rate
	I	I	I	I		50
	I	I	I	R		75
	I	I	R	I		110
	I	I	R	R		134.5
	I	R	I	I		150
	I	R	I	R		300
	I	R	R	I		600
	I	R	R	R		1200
	R	I	I	I		1800
	R	I	I	R		2000
	R	I	R	I		2400
	R	I	R	R		3600
	R	R	I	I		4800
	R	R	I	R		7200
	R	R	R	I		9600

I = Jumper Inserted = Program Bit Cleared.

R = Jumper Removed = Program Bit Set.

*Bit 11 of the XCSR (Write Only Bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

Table 4.1.4

Data Bit Selections

Jumpers		Number of Data Bits
2	1	
I	I	5
I	R	6
R	I	7
R	R	8

5.0 TEST SET UP

5.1 No special test set up is required.

6.0 POWER CHECKS

6.1 Power requirements:

+5V ± 5% @ 1.0A (5.0 w)
+12V ± 5% @ 150 MA (1.8w)

NOTE: -12V is generated internally on the M8017 from the +12V supply.

6.2 Bus Loading

Each DLV11-E places one (1) bus load on the Q Bus as defined by the LSI-11 Q Bus Spec. (DEC STD 100).

7.0 DIAGNOSTIC TEST PROCEDURE

7.1 The DLV11-E can be tested in two (2) different turnaround configurations.

7.1.1 The first configuration for testing would be to plug a turnaround test connector directly into the DLV11-E. See Diagram 7.1 for view. This method should be used when it is impratical to work with the long modem cables or when the volume of DLV11-E's requires many cables. See Diagram 7.3 for information to make test connector.

NOTE: This test connector has no part # and cannot be ordered.

7.1.2 The second configuration for testing would be to plug a modem cable into the DLV11-E and plug the H315 turnaround connector; that is supplied, into the other end of the cable. See Diagram 7.2. The modem cable is not supplied on the DLV11-E. A cable may be supplied to the customer. If there is a cable going to the customer, use that one. If a cable is not going to be supplied, use a BC01V-X or BC05C-X.

7.2 Diagnostic Test

7.2.1 After configuring the DLV11-E to Section 7.1.1 or 7.1.2, load CVDVA through appropriate load media.

7.2.2 Starting program

7.2.2.1 Load address 200.

7.2.2.2 Start;check Section 7.2.3 for available switch settings.

7.2.3 Available test switch settings

7.2.3.1 Bit 15 - Halt on error
14 - Loop on test
13 - Inhibit error typeouts
12 - (unused)
11 - Inhibit iterations
10 - Bell on error
9 - Loop on error
8 - Loop on test in SWR 7:Ø
7 - Test number to loop on (used with Bit 8)

7.2.4 End of Pass is indicated by a type out

DIAGRAM 7.1

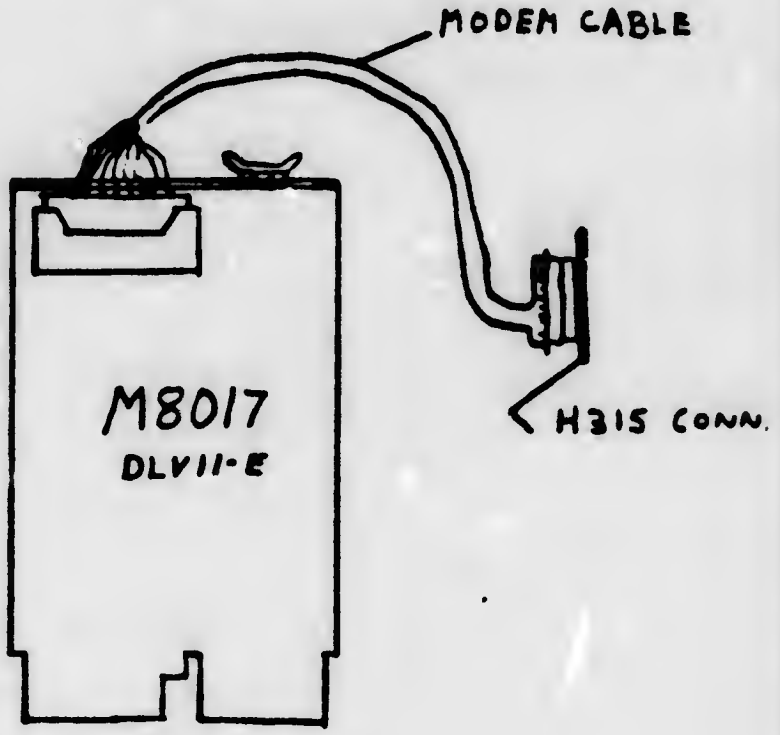


DIAGRAM 7.2

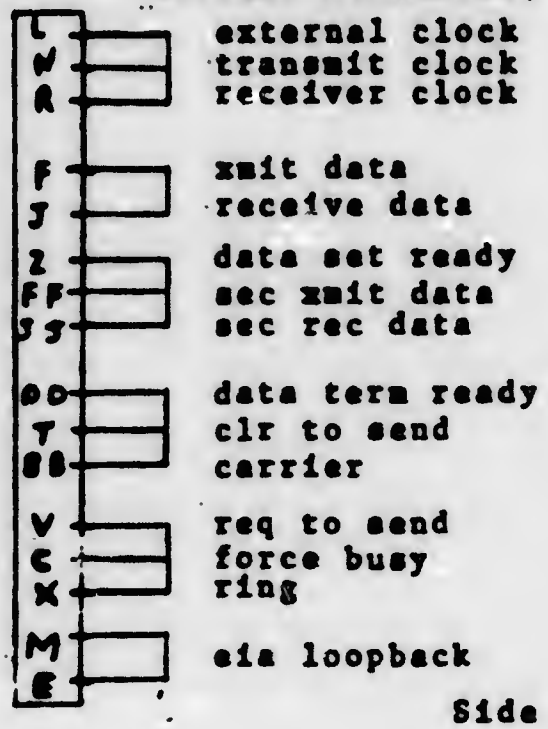
M8017 Test Connector

Diagram 7.3

Parts List

Part #	Description	Qty	Item #
12-10918-15	Conn, 44 Pos, HSG	1	1
12-10089-06	Socket, Crimp	16	2
91-07636-00	Wire, #26 Awg, Black	see notes	3
12-11166-00	Strain relief	1	4
36-11567-00	Label (this side up)	1	5

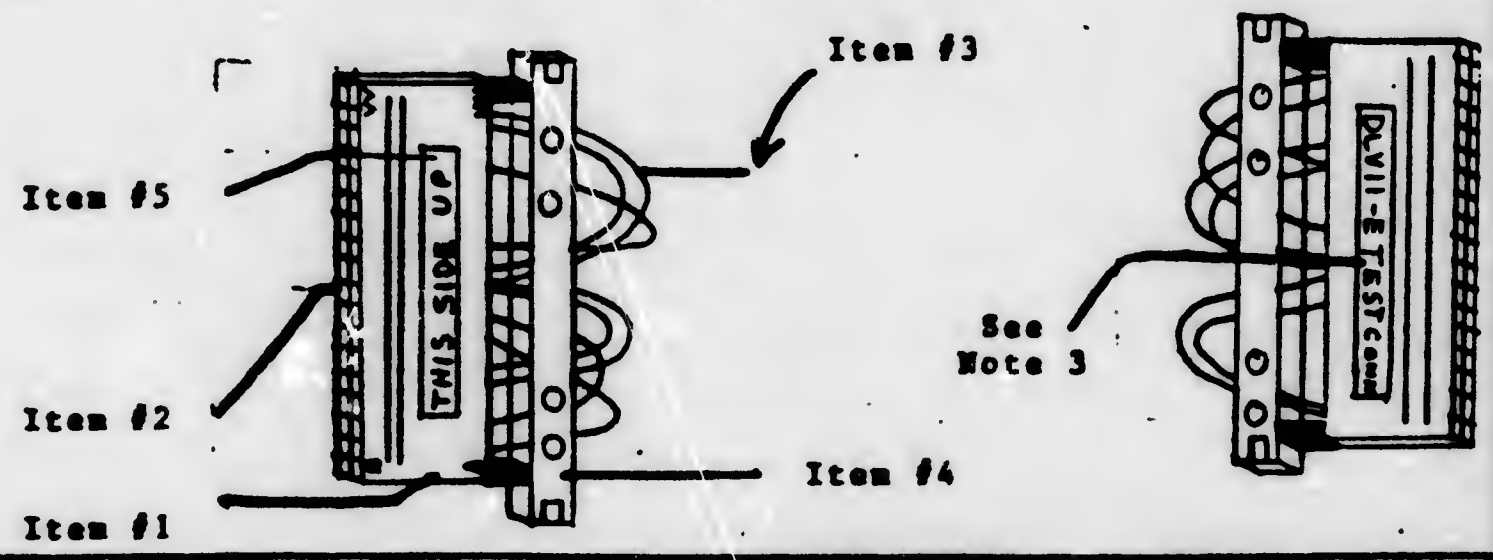
Circuit Schematic, Wire List



NOTES:

1. Suggested length of jumpers is ≈ 4 inches.
2. Actual jumper count is
   4 - double jumpers
   2 - single jumpers
3. On side 2 of Berg connector, attach label with identification "DLV11-E Test Conn". (no part # available for label)

Unit Assembly



	SIZE	CODE	NUMBER	REV
	A	SP	MAA5321-0-0	A


A53Z

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DLV11-F ASYNCHRONOUS SINGLE SERIAL LINE INTERFACE WITH 20ma

REVISIONS APPENDIX A

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5322					

ENG	APPD	SIZE	CODE	NUMBER	REV
Brent MacAloney		A	SP	MAA5322-0-0	A

DLV11-F ASYNCHRONOUS SINGLE SERIAL LINE INTERFACE WITH 20ma

INTRODUCTION

This procedure establishes the minimum test standards that a DLV11-F must meet to be considered acceptable for customer shipment.

DESCRIPTION

The DLV11-F is an asynchronous line interface module that interfaces the LSI-11 bus to a serial communications line. The DLV11-F receives serial data from a peripheral device and assembles it into parallel data for the LSI-11 bus. In turn, the parallel data from the LSI-11 bus is converted into serial data and is transmitted to a peripheral device. The DLV11-F is unique from the DLV11-E in that it supports 20ma current loop operation.

Option	Qty/contents	Description
DLV11-F	1 - M8028	module

1.0 REFERENCE DOCUMENTATION

1.1 Print Set MP00461

1.2 Technical Manual EK-DLV11-TM- (rev)

1.3 Users Guide EK-DLV11-OP-(rev)

1.4 Lib Kit ZJ-253-RB

1.5 Ship List A-PL-DLV11-F

1.6 Packaging Inst. A-SP-370029?-40-0

2.0 REQUIRED TEST EQUIPMENT

2.1 PDP11/03 with a minimum of 4K of memory and one available slot.

2.2 Scope: 465 or equivalent.

2.3 For power requirements, refer to Section 6.0.

2.4 Wire Wrap Gun (ok speed wrap model #BW-515BF) or equivalent.

2.5 Unwraping tool - hand type, unwraping tool.

3.0 AVAILABLE DIAGNOSTICS

3.1 LIB Kit # ZJ-253-RB
CVDVC - DLV11-F off line tests (paper tape and document)

3.2 DECX11 - DXDLA-H DLV11 Exerciser (Rev H or higher only)

4.0 INSTALLATION INSTRUCTIONS

4.1 If the DLV11-F is being tested as an option add-on, it is not necessary to change configuration jumpers. See Tables 4.1.1 and 4.1.2 for configuration shipped from Volume Manufacturing.

4.2 When being installed in a customer system, it may be necessary to change the jumpers as they are shipped. When configuring, refer to Tables 4.1.1 and 4.1.2 for proper installation.

4.3 CAUTION #1:

When changing wire wrapings, always use equipment designed for that purpose and calibrated. Note sections 2.4 and 2.5 for type of equipment.

4.4 CAUTION #2:

All wire wrapings must be done to Digital's workmanship standard; DEC STD 116. Reference should be made to Section 3 in that text.

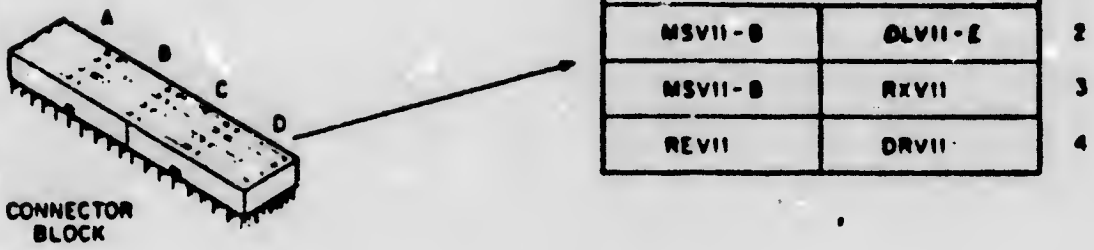
4.5 The DLV11-F can be installed in any slot of the LSI-11 Backplane, except those occupied by the processor modules. When installing the DLV11-F, do not leave any open slots between the processor modules and the DLV11-F. An open slot would break the interrupt acknowledge daisy chain. Note: the priority for each option is determined by how close that option is installed to the processor modules. The closer to the processor you get, the higher priority the option. A picture of a typical configuration is shown on Page 3 and 4.

TITLE MODULAR APPROACH TO SYSTEMS TEST - APPENDIX A

TYPICAL BACKPLANE CONFIGURATION

11/03

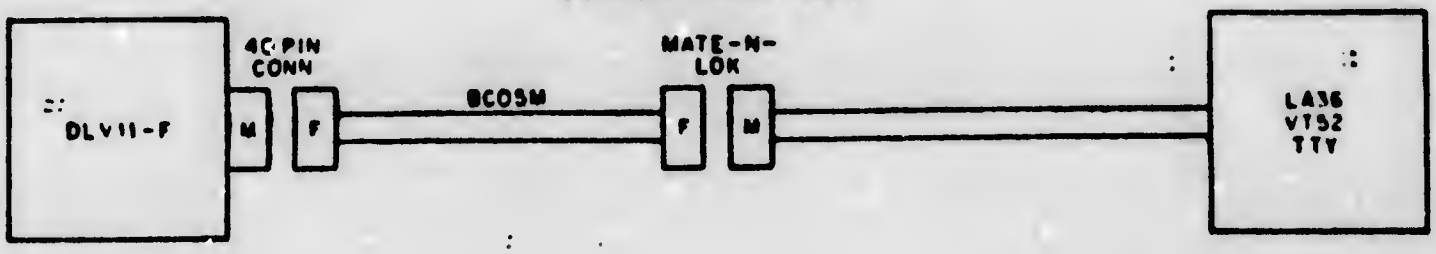
VIEW FROM MODULE SIDE OF BACKPLANE

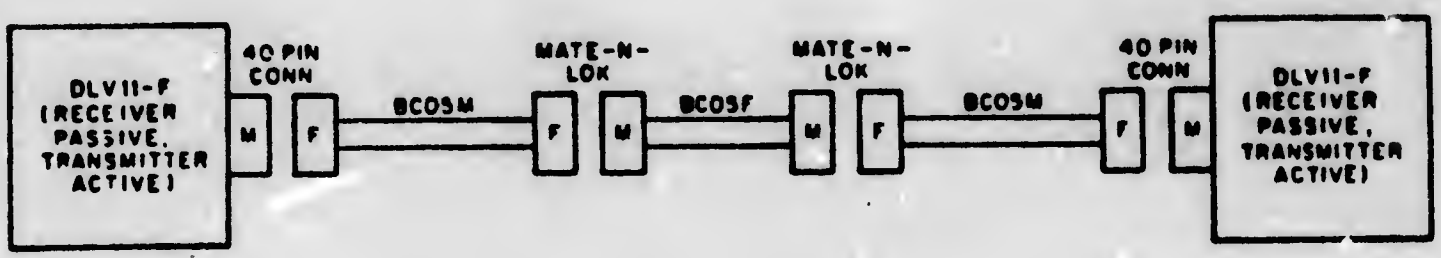


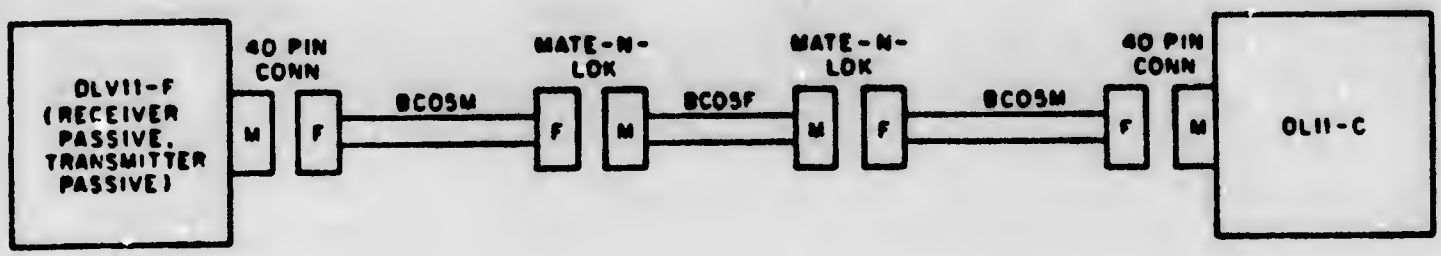
11/03

DLV11-F Cabling Examples

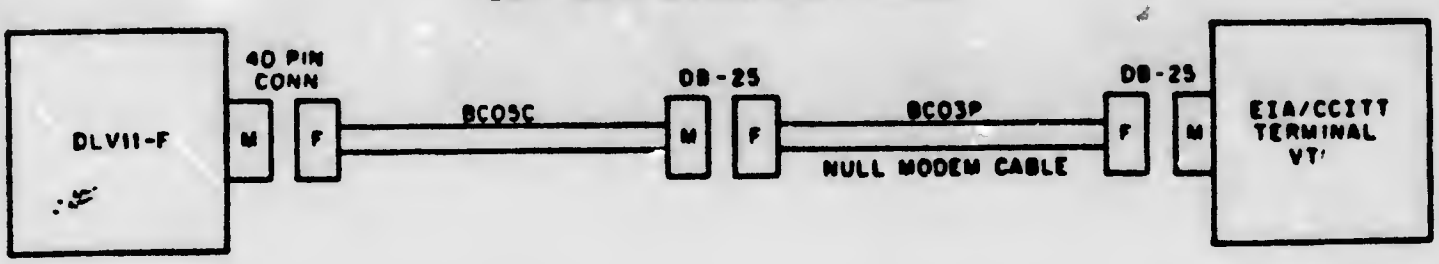
CURRENT LOOP MODE







EIA "DATA LEADS ONLY" MODE



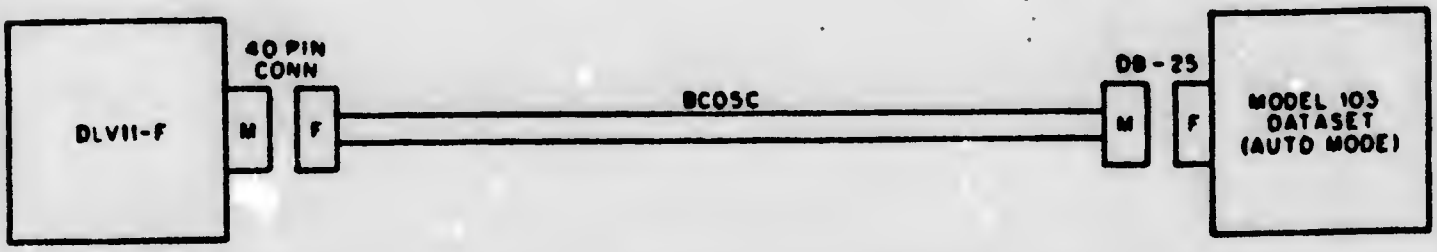


Table 4.1.1 DLV11-F JUMPER LOCATIONS

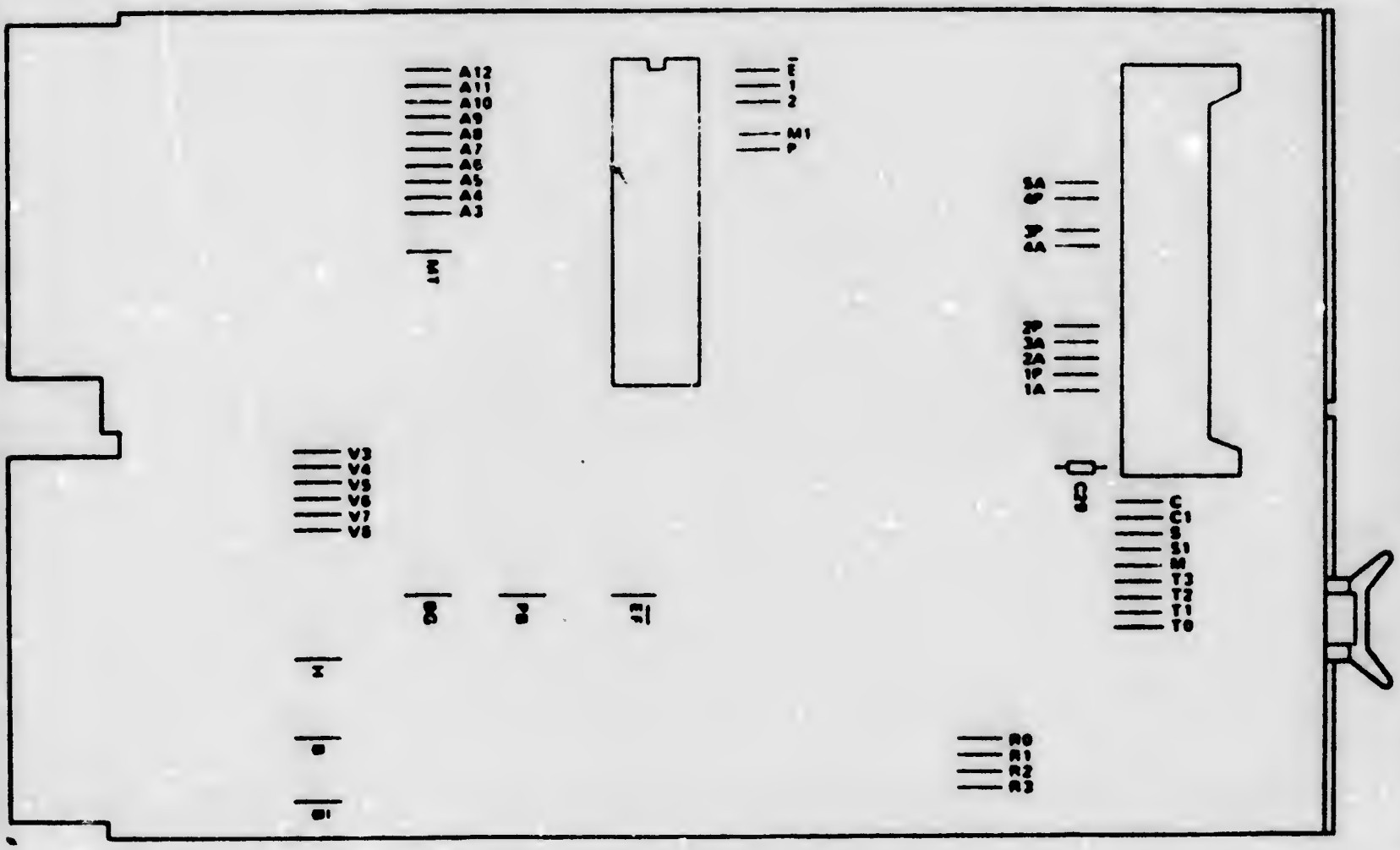


TABLE 4.1.2 JUMPER DEFINITIONS

I = Jumper inserted = program bit cleared

R = Jumper removed = program bit set

NOTE: Jumpers are inserted to enable the function they control except for those jumpers that indicate negation (such as "B") Negated jumpers are removed to enable the functions they control.

Jumper	Jumpers Installed when ship'd from Vol. Mfg.	Function
A3-A12		These jumpers correspond to bits 3-12 of the address word. When inserted, they will cause the bus interface to check for a True condition on the corresponding address bit.
A3	R	Jumpers A3 through A12 implement device address 17756X for the DLV11-F. The least significant octal digit is hard-wired on the module to address the four device registers as follows: (see table 4.1.4) X = 0 RCSR X = 2 RBUF X = 4 XCSR X = 6 XBUF
A4	I	
A5	I	
A6	I	
A7	R	
A8	I	
A9	I	
A10	I	
A11	I	
A12	I	
V3-V8		Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector address bit on the LSI-11 bus.
V3	R	This jumper selection implements interrupt vector address 60_8 for receiver interrupts and 64_8 for transmitter interrupts on the DLV11-F. See table 4.1.5.
V4	I	
V5	I	
V6	R	
V7	R	
V8	R	

Jumper	Jumpers installed when ship'd from Vol. Mfg.	Function
R0 R1 R2 R3	I R I I	The module is configured to receive at 110 baud. Receiver and transmitter baud rate select jumpers, during common speed operation. See table 4.1.3
T0 T1 T2 T3	I R R R	The transmitter is configured for 9600 baud if split speed operation is used. Transmitter baud rate select jumpers during split speed operation. See table 4.1.3
BG	I	Jumper is inserted to enable Break generation.
P	R	Jumper is inserted for operation with parity.
E	R	Removed for even parity; inserted for odd parity. Receiver checks for appropriate parity and transmitter inserts appropriate parity.
1,2	R,R	These jumpers select the desired number of data bits (see Table 4.1.4)
PB	R	Jumper is inserted to enable the programmable baud rate capability.
C,C1	I,I	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted)
S,S1	R,R	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	I	This jumper is inserted to assert BHALT L when a framing error is received. This places the LSI-11 in the halt mode.

Jumper	Jumpers Installed when Shipping from Vol. Manfg.	Function
B	R	Jumper B is inserted to negate BDCOK H when a BREAK signal framing error is received. This causes the LSI-11 to reload the bootstrap. (Jumper $\overline{B}$ must be removed when B is inserted.)
$\overline{B}$	I	
1A 2A 3A	I I I	These jumpers are inserted to make the 20MA current loop receiver active (jumpers 1P, 2P must be removed when 1A, 2A, and 3A are inserted).
1P 2P	R R	These are inserted to make the 20MA current loop receiver passive (jumpers 1A, 2A, and 3A must be removed when 1P and 2P are inserted).
4A 5A	I I	Inserted to make the 20MA current loop transmitter active (jumpers 3P and 4P must be removed when 4A and 5A are inserted).
3P 4P	R R	Inserted to make the 20MA current loop transmitter passive (jumpers 4A and 5A must be removed when 3P and 4P are inserted).
EF	I	Jumper is removed to enable the error flags to be read in the high byte of the receiver buffer.
MT	R	When inserted, enables maintenance bit.
M,M1	R,R	These are test jumpers used during the manufacture of the module. They are not defined for field use.

TABLE 4.1.3

Baud Rate Selections

	Bit	Bit	Bit	Bit	Bit	
Program Control	15	14	13	12	11*	
Receive Jumpers	R3	R2	R1	R0		Baud
Transmit Jumpers	T3	T2	T1	T0		Rate
	1	1	1	1		50
	1	1	1	R		75
	1	1	R	1		110
	1	1	R	R		134.5
	1	R	1	1		150
	1	R	1	R		300
	1	R	R	1		600
	1	R	R	R		1200
	R	1	1	1		1800
	R	1	1	R		2000
	R	1	R	1		2400
	R	1	R	R		3600
	R	R	1	1		4800
	R	R	1	R		7200
	R	R	R	1		9600

1 = Jumper Inserted = Program Bit Cleared.

R = Jumper Removed = Program Bit Set.

* Bit 11 of the XCSR (Write Only Bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

TABLE 4.1.4

Data Bit Selections

Jumpers		Number of Data Bits
2	1	
1	1	5
1	R	6
R	1	7
R	R	8

4.1.4 Address Selections

Jumpers: - inserted
R removed

Address	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
160000	-	-	-	-	-	-	-	-	-	-
160010	-	-	-	-	-	-	-	-	-	R
160020	-	-	-	-	-	-	-	-	R	-
160030	-	-	-	-	-	-	-	-	R	R
160040	-	-	-	-	-	-	-	R	-	-
160050	-	-	-	-	-	-	-	R	-	R
160060	-	-	-	-	-	-	-	R	R	-
160070	-	-	-	-	-	-	-	R	R	R
160100	-	-	-	-	-	-	R	-	-	-

4.1.5 Vector Selections

Jumpers: - inserted
R removed

Vector	V08	V07	V06	V05	V04	V03
300	-	R	R	-	-	-
310	-	R	R	-	-	R
320	-	R	R	-	R	-
330	-	R	R	-	R	R
340	-	R	R	R	-	-
350	-	R	R	R	-	R
360	-	R	R	R	R	-
370	-	R	R	R	R	R
400	R	-	-	-	-	-

5.0 TEST SET UP

5.1 No special test set up is required.

6.0 POWER CHECKS

6.1 Power Requirements

+5V ± 5% @ 1.0A (.0W)
+12V ± 5% @ 150 ma (5.0W)

NOTE: -12V is generated internally on the M8028 from +12V supply.

6.2 Bus Loading

Each DLV11-F places one (1) Bus load on the Q Bus as defined by the LSI-11 Q Bus spec. (DEC STD 160).

7.0 DIAGNOSTIC TEST PROCEDURE

7.1 The DLV11-F does not come with a turnaround connector as does the DLV11-E. Because of this, the DLV11-F will only be tested in the internal maintenance mode.

7.2 Diagnostic Test

7.2.1 After the DLV11-F has been checked for proper jumper configuration load CVDVC through appropriate load media.

7.2.2 Starting program

7.2.2.1 After checki ng available switch settings (7.2.3), start the program.

7.2.2.2 200G

7.2.3 Available switch settings

Bit 15 - Halt on error
14 - Loop on test
13 - Inhibit error
12 - (unused)
11 - Inhibit iterations
10 - Bell on error
9 - Loop on error
8 - Loop on test in SW (7:0)
7-0 - Test number to loop on (used with Bit 8)

7.2.4 End of pass is indicated by a type out.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 9/4/79

TITLE M.A.S.T. DLV11-J Four Line Serial Interface

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	Added Appendix A (pp. 15-16) to include the H3171 Distribution Panel ECO CHANGE	MA-MA0000 ML006	T. JELENIEWSKI	9-79	Tom Jeleniewski (Test)	10-1-80

4

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Ayotte	Tom Jeleniewski	A	SP	MA-A5324-0-0	C

DLV11-J FOUR LINE SERIAL INTERFACE

1.0 INTRODUCTION

This procedure establishes the minimum test requirements that a DLV11-J must meet to be considered acceptable for customer shipments from Systems Manufacturing.

1.1 Description

The DLV11-J is an asynchronous line interface module that interfaces the LSI-11 Bus to 4 serial communications lines. The DLV11-J is a dual-height module with E.I.A. operation 20MA operation is available when the DLV11-KA is used in conjunction with the DLV11-J. Although each line can be configured to operate at different baud rates, no split baud rates are possible.

Option	Qty/Contents	Description
DLV11-J	1-M8043	Module

2.0 REFERENCE DOCUMENTATION

2.1 Print Set MP00586

2.2 Users Guide EK-DLV1J-UG-???

2.3 Lib Kit ZJ-269-RB

2.4 Ship List - Reference should be made to System Manufacturing Ship List, not Engineering Ship List.

2.5 Packaging - A - PS-9905622-0-0

3.0 REQUIRED TEST EQUIPMENT

3.1 PDP 11/03 with a minimum of 4K of memory and one available slot.

3.2 Scope: 465 or equivalent

3.3 For power requirements, refer to Section 7.0 D.V.M. with 3 digits

3.4 Wire wrap gun (OK speed wrap model #BW-515BF) or equivalent.

3.5 Unwrapping tool - hand type, unwrapping tool

3.6 H3270-A (turnaround connectors) are needed for device testing. (See Section 6.1)

4.0 AVAILABLE DIAGNOSTIC PROGRAMS

4.1 Kit # ZJ269-RB CVDLA - DLV11-J Test, paper tape and listing

5.0 SPECIAL INSTRUCTIONS

5.1 Caution #1 - When changing wire wrappings, always use equipment designed for that purpose, and that is calibrated. Note Section 2.4 and 2.5 for type of equipment

5.2 Caution #2 - All wire wrapping must be done to Digital's workmanship standard; DEC Std 116. Reference should be made to Section 3. in that text.

6.0 INSTALLATION INSTRUCTIONS

6.1 Option Add-On

The DLV11-J may not require changes to the jumpers as it was configured from Volume Manufacturing. (Refer to Diagram 6.1.1 for jumper configuration). The DLV11-J Line 3 is configured for console device addresses 177560 - 177566 and vectors 60 and 64. For jumper definitions, refer to Table 6.1.2. DLV11-J is capable of being tested with Channel 3 in console mode. No changes will be required to the module when Channel 3 is console. This requires an EIA terminal or a DLV11-KA (EIA-20ma) option/20ma terminal to be used. This configuration will require the turn-around connectors mentioned in Section 3.6 to be used in Channels 0, 1, 2. Refer to Section 6.6 for addition of 2-DLV11-J.

If the above terminal equipment is not available, the DLV11-J is to be run with all 4 lines turned around using the turn around connectors mentioned in Section 3.6. This will require the DLV11-J be configured so all lines will be consecutively addressed and no console selected. Refer to Diagram 6.1.1. Table 6.1.2. and Section 8 for proper diagnostic setup when in this configuration. The following is a list of changes required to the DLV11-J so it may be run with 4 lines wrap-around:

V5 = Removed

C1 = X to 0

C2 = X to 0

X to H = K to C

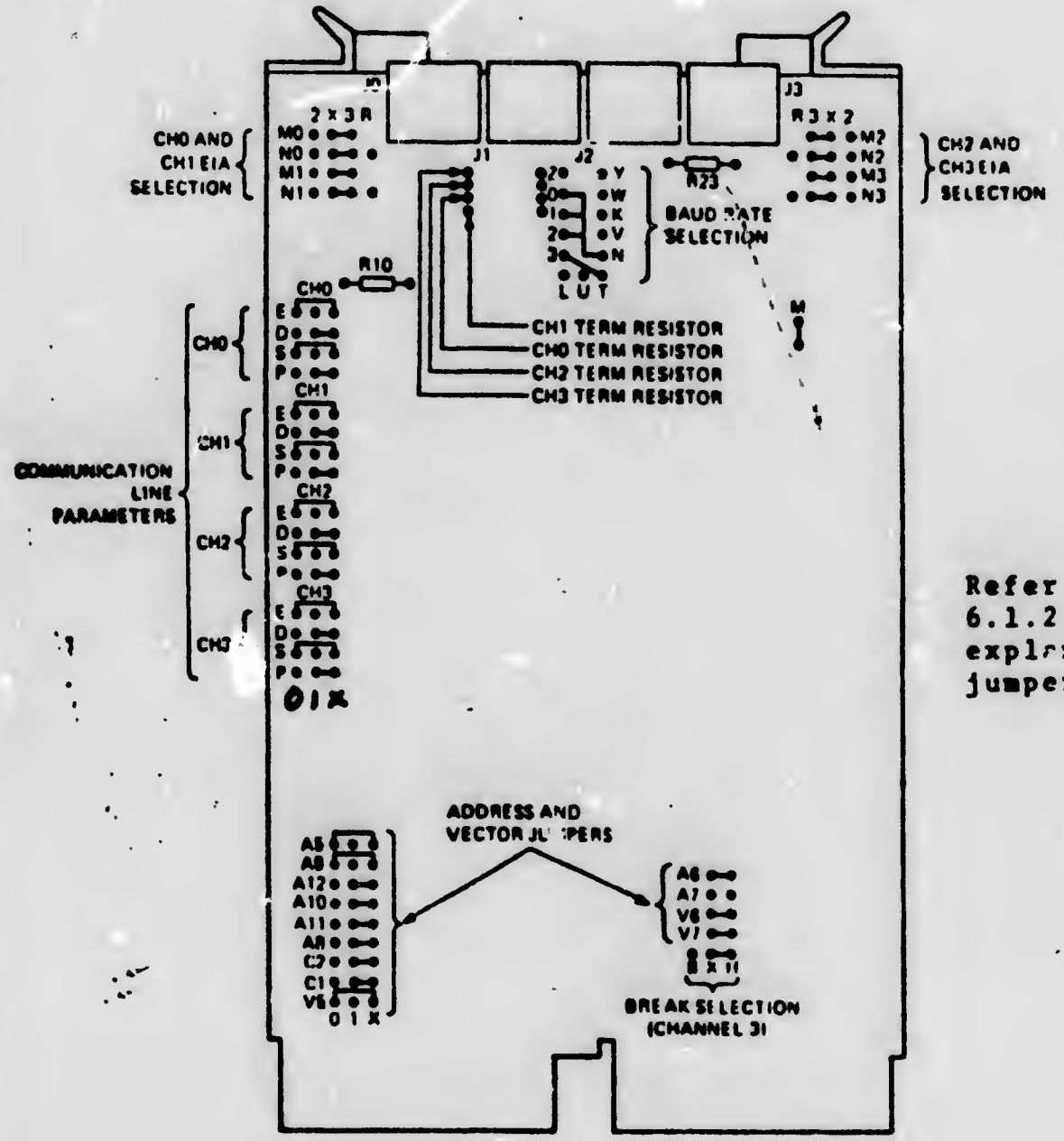
Diagnostic location 1220 must be 21 as defined in Section 8.2.4.2.

TITLE MODULAR APPROACH TO SYSTEMS TEST - APPENDIX A

X - Base Pin for function

0 - Logical 0 Pin

1 - Logical 1 Pin



Refer to Table 6.1.2 for pin explanations & jumper definitions.

Diagram 6.1.1
DLV11-J Jumper Configuration
When Supplied By Volume Manufacturing

	SIZE	CODE	NUMBER	REV
	A	SP	MAA5324-0-0	C

6.1.2 Jumper Definitions

R = Removed

I = Inserted

JUMPER	CONF. SHIP'D FROM VOL MFG.	FUNCTION
		Address
A5-A12		These jumpers correspond to Bits 5-12 of the address word for Channel 0. The least significant digit is decoded on the module during operation to address one of four serial line units device registers as follows: X = 0 RCSR X = 2 RBUF X = 4 XCSR X = 6 XBUF
A12	X to 1	This arrangement of jumpers implements the octal base device address 176500 for Channel 0 from which Channels 1 and 2 are automatically determined on the module.
A11	X to 1	
A10	X to 1	
A9	X to 0	
A8	X to 1	
A7	R	
A6	I	
A5	X to 0	
		Console Address Selection
C1 and C2		These jumpers allow the configuration of the last four addresses used on Channel 3 to be assigned to the console addresses 177560-177566. The preceding addresses of Channels 0, 1, and 2 are not affected.
C1	X to 1	C1 and C2 set to enable Channel 3 for console operation. The base address must be 176500, 176540, or 177500. If not set, Channel 3 will default to next consecutive address from Channel 2. (X to 0)
C2	X to 1	

6.1.2 Jumper Definitions cont.

JUMPER	CONF. SHIP'D FROM VOL MFG.	FUNCTION
Break		This can enable the use of a break response while Channel 3 is in console mode, or for bootstrap response.
Halt	X to H	Jumper set to enable break generation.
Boot	B to X	Jumper has to be disabled when break is set. Remove jumpers when Channel 3 is not console.
		<u>Vectors</u>
V5 - V7		Used to generate the vector during an interrupt transaction. V6 and V7 designate the base vector address and V5 determines the console vector for Channel 3.
V7	I	This arrangement implements the octal base vector of 300 and Channel 3 at 60 and 64. With V5 removed, the vector addresses for Channel 3 will be 330 and 334.
V6	I	
V5	X to 0	
		<u>Parity, Data Bits, Stop Bits, Odd/Even Parity</u>
P,D,E,S		Each channel (communication line) is capable of being set for individual line operation. D enables 7 or 8 data bits, E allows even or odd parity, P allows parity generation or no parity generation, S enables one or 2 stop bits.
D	X to 1	This allows 8 data bits to be used. For 7 data bits, insert Jumper X to 1.
S	X to 0	Jumper inserted for 1 stop bit. For 2 stop bits, insert Jumper X to 1.
P	X to 1	With this jumper inserted, parity generation and detection is disabled. For parity operation, insert jumper X to 0.

6.1.2 Jumper Definitions cont.

JUMPER	CONF. SHIP'D FROM VOL MFG.	FUNCTION
E	X to 0	Selects odd parity or even parity. Insert Jumper X to 1. NOTE: P Jumper must be X to 0 for selection of odd/even parity, and E must always be in odd or even state; never removed.
0,1,2,3		**Baud Rates** One baud rate wire wrap pin is provided for each channel. These numbers correspond to the respective lines. Both transmitter and receiver operate at the selected speed. To determine the baud rate for a channel, connect the jumper to the channel desired, and the other end to the desired baud rate pin (reference list below). Wire Wrap Pin Label / Baud Rate Bits/Sec. U 150 T 300 V 600 W 1200 Y 2400 L 4800 N 9600 K 19200 Z 38400 NOTE: If more than one channel requires the same baud rate, wire wrap jumpers may be daisy chained. Effective / Actual 0 — 0 to N — Configured for 9.6K baud — 0 to 1 1 — 1 to N — Configured for 9.6K baud — 2 to N 2 — 2 to N — Configured for 9.6K baud — 1 to 2 3 — 3 to T — Configured for 300 baud

6.1.2 Jumper Definitions cont.

JUMPER	CONF. SHIP'D FROM VOL MFG.	FUNCTION
M	I	Maintenance Bit (not for Systems Manufacturing usage)
NO-N3 MO-M3		These jumpers determine if EIA (RS-422, RS-423/RS232C]) or 20ma operation will be used.
NO-N3 MO-M3	X to 3 X to 3	These jumpers are inserted so the DLV11-J will be compatible for both EIA RS-423 and RS-232C simultaneously. For other configurations, see below: NOTE: When EIA RS-423 and RS-232C configuration is used, no termination resistors are to be installed. R10 and R23 must be installed. EIA RS-422 Operation 1) NO-N3 connect X to 2 2) MO-M3 connect X to 3 3) R10 and R23 are not required. 4) Terminating resistors R33 (CH3), R32 (CH2), R30 (CH0), R31 (CH1) are required to be 100 OHM ¼ watt, non-wire wound fusible resistors. P/N 13-00229-00 20MA Current Loop (Requires operation with DLV11-KA option) 1) NO-N3 connect X to R.(for program controlled paper tape reader) 2) MO-M3 Connect X to 3. 3) No termination resistors required. 4) R10 and R23 must be installed.

6.1.2 Jumper Definitions cont.

JUMPER	CONF SHIP'D FROM VOL MFG	FUNCTION
R10,R23		The value of Resistor R10 determines the slew rate of both channels 0 and 1, which are simultaneously set to the same value. Similarly, R23 controls the slew (settling) rate of both channels 2 and 3. These resistors are not required for operation in EIA RS-422.
R10	22K OHM	Channels 0 and 1
R23	22K OHM	Channels 2 and 3
		For selecting the correct value ¼" non-wire wound resistor. For R10 and R23, use list below:

Resistor	P/N	Baud Rate
22K	13-01808-00	38.4K
59K	13-00525-00	19.2K
120K	13-00539-00	9.6K
200K	13-14516-00	4.8K
430K	13-14649-00	2.4K
820K	12-03187-00	1.2K
1 MEG. OHM	13-09595-00	600 300 150 110

NOTE: If channels 0 and 1 are split baud rates the resistor value defalts to the higher baud rate. This holds true for channels 2 and 3.

6.2 System Installation

When the DLV11-J is being installed in a customer system, it may be necessary to change the jumpers as they were shipped from Volume Manufacturing. When configuring, refer to Diagram 6.1.1 and Table 6.1.2 to assure proper installation. Reference 6.1 for proper test set up.

6.3 The DLV11-J has many possible cabling configurations. Diagram 6.3.1 is an example of EIA interfacing and Diagram 6.3.2 is an example of 20MA interfacing.

NOTE: Remember that these are only examples, and are not necessarily all the possible combinations.

6.4 When installing the DLV11-J, do not leave any open slots between the processor module or memory and the DLV11-J. The priority for each option is determined by how close that option is installed to the processor modules. The closer to the processor you get, the higher priority the option has.

6.5 20MA Operation

The DLV11-J is capable of interfacing with 20MA when used with a DLV11-KA option.

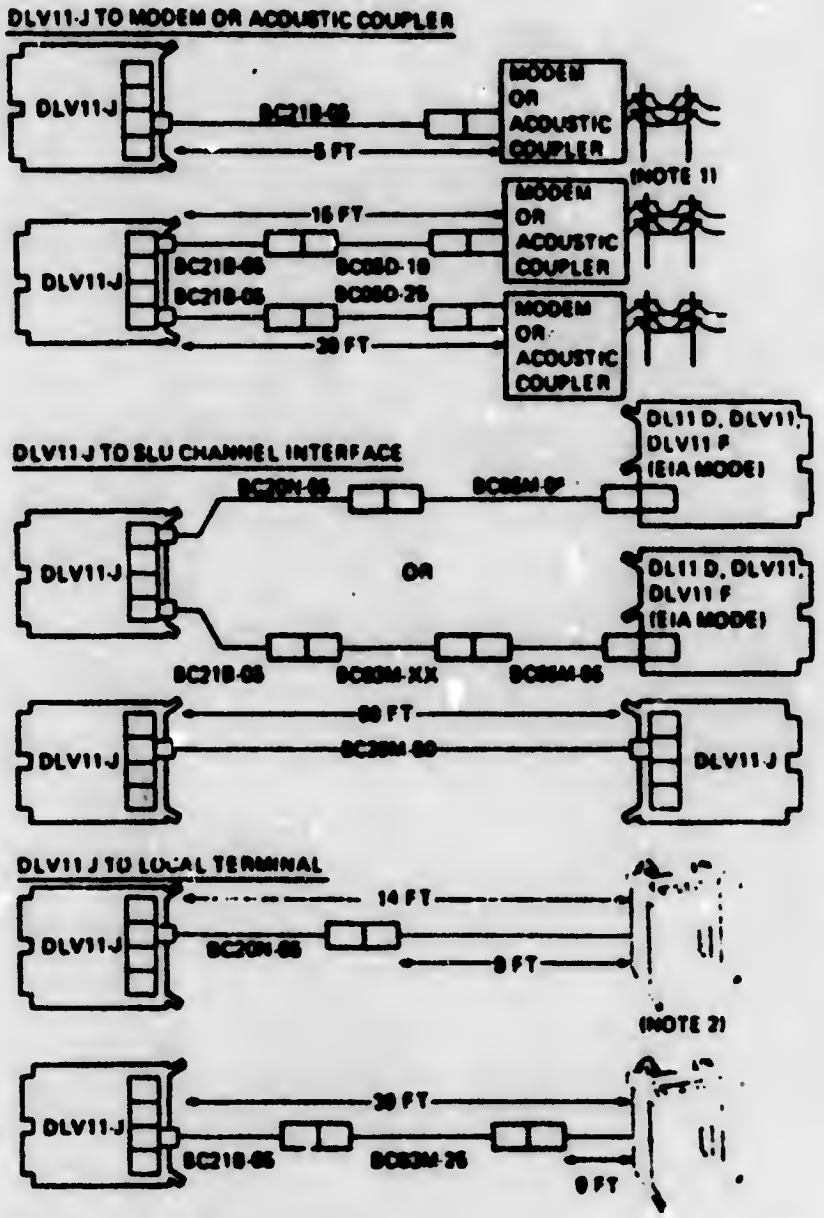
Option	Qty/Contents	Description
DLV11-KA	1-BC21A-03	Cable
	1-DLV11-KB	EIA to 20MA converter
DLV11-KB	1-EIA to 20MA Converter	

Configure the DLV11-J for 20MA operation as described in Section 6, using Diagrams 6.1.1, 6.1.2, and 6.3.2.

A 110 baud rate clock generator circuit is contained on the optional DLV11-KA 20 MA option. When 110 baud operation is desired, do not connect the baud rate jumper on the DLV11-J module for that particular channel. The 110 baud clock will be supplied by the DLV11-KA option through the interface connector.

6.6 Additional DLV11-J
When the first DLV11-J is used as console and another DLV11-J is to be used as 4-additional lines the starting address is the Base Address of the first module plus 30 and the Vector is the Base Address of the first module plus 30.

TITLE MODULAR APPROACH TO SYSTEMS TEST - APPENDIX A



NOTES:
1. MODEM USED IS A "MANUAL TYPE" SUCH AS BELL 103A WITH 8040.
2. DEC EIA RS-232C TERMINALS (VT52, LA36, LS120, ETC.) COME EQUIPPED WITH A 8 FT CABLE. NON-DEC EIA RS 232C TERMINALS ARE CONNECTED SIMILARLY EXCEPT 8 FT OF LENGTH MUST BE DEDUCTED FROM THE TOTAL CABLE LENGTH.

Diagram
6,3,1

	SIZE	CODE	NUMBER	REV
	A	SP	MAA5324-0-0	C

TITLE MODULAR APPROACH TO SYSTEMS TEST - APPENDIX A

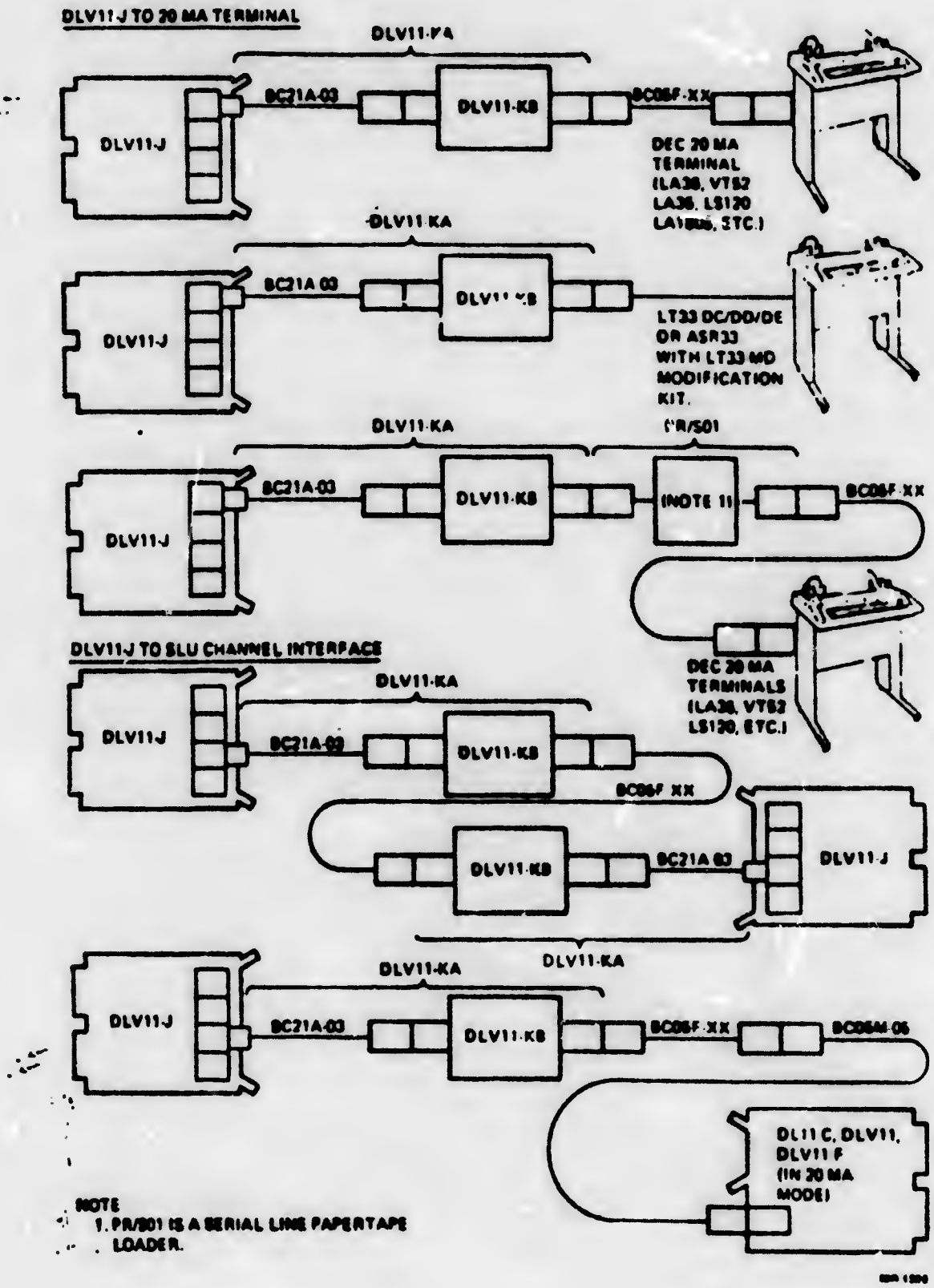


Diagram
6.3.2

	SIZE	CODE	NUMBER	REV
	A	SP	MAA5324-0-0	C

7.0 POWER CHECKS

7.1 Power Requirements

+5V ± .25V@ 1.0A typ. (1.25A max.)

+12V ± .36V@ 0.15A typ. (0.2A max.)

7.2 +12V is present on Pin 10 of each channel. This line is provided for the DLV11-KA option operation.

7.3 Bus Loading

Each DLV11-J places (1) AC and (1) DC Bus load on the Q Bus as defined by the LSI-11 Q Bus Spec. (DEC Std 160).

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 The DLV11-J can be tested 3 different ways as specified in Section 6.1. Reference should be made to that section for proper installation and configuration before diagnostics are run.

NOTE: If the DLV11-J is configured for 4 additional lines, the diagnostic must be loaded with another device as console. Diagnostic progr, must be modified at Loc 1220 ($USWR).

8.2 Starting Program

8.2.1 Load (CVDLA) diagnostic through appropriate load media. When running under APT loc 1220 ($USWR) must be 31 as defined in Section 8.2.4.2

8.2.2 Start: Refer to Section 8.2.4.1 for available switch register settings. Refer to Section 8.2.4.2 for configuration options program changes.

8.2.3 Initial system type 200 G.

8.2.4.1 Software Switch Register Options

Bit 15 set = 100000 = Halt on Error
14 set = 40000 = Loop on test (when testing in process)
13 set = 20000 = Inhibit error type outs
12 set = 10000 = Enable performance reports
11 set = 4000 = Inhibit iterations
10 set = 2000 = Bell on error
9 set = 1000 = Loop on error
8 set = 400 = Loop on test in SWR <7:0>
7:0 = Number of test to loop on (used with bit 8). All tests previous to the selected test are executed first with one iteration only.

8.2.4.2 Options
$USWR is at location 1220 in the program.
Location $USWR contains all the user selectable options. The values in this word must conform to the actual board configuration.

BIT POSITION	DEFINITION	$USWR DEFAULT VALUE
0	# of data bits transmitted 0 - 7 bits, 1 = 8 bits	1 = 8 Bits
1	Parity enabled	0 = NO
2	Even odd parity	0 = ODD
3	Break generation enabled	1 = YES
4	Run data wrap around tests	1 = YES
<11:9>	Console Device	1 = YES = console on module 1 Channel 3
<11:9> = 0	= No console selected	
<11:9> = 1	= Console on Module 1	
<11:9> = 2	= Console on Module 2	

IMPORTANT NOTE: For diagnostic purposes, all channels must be configured the same, either 7 or 8 bits.

8.3 End of Pass is indicated by a type out with no errors.

APPENDIX A

H3171 DISTRIBUTION PANEL

The H3171 Distrbution panel relinquishes the need to use four separate BC21B cables with the DLV11-J. It occupies 1.75 inches of panel space in a standard 19 inch rack. The H3171 incorporates an H7004 static filter to improve the R.F. integrity of the system. There are two mechanical configurations available. They are as follows:

A) H3171-A (Separate Filter)
This configuration is used in conjunction with CPU boxes that have a mounting bracket for static filters built directly into them. In this case the H3171 distribution panel itself contains no filter. The filter is located on the CPU bracket.

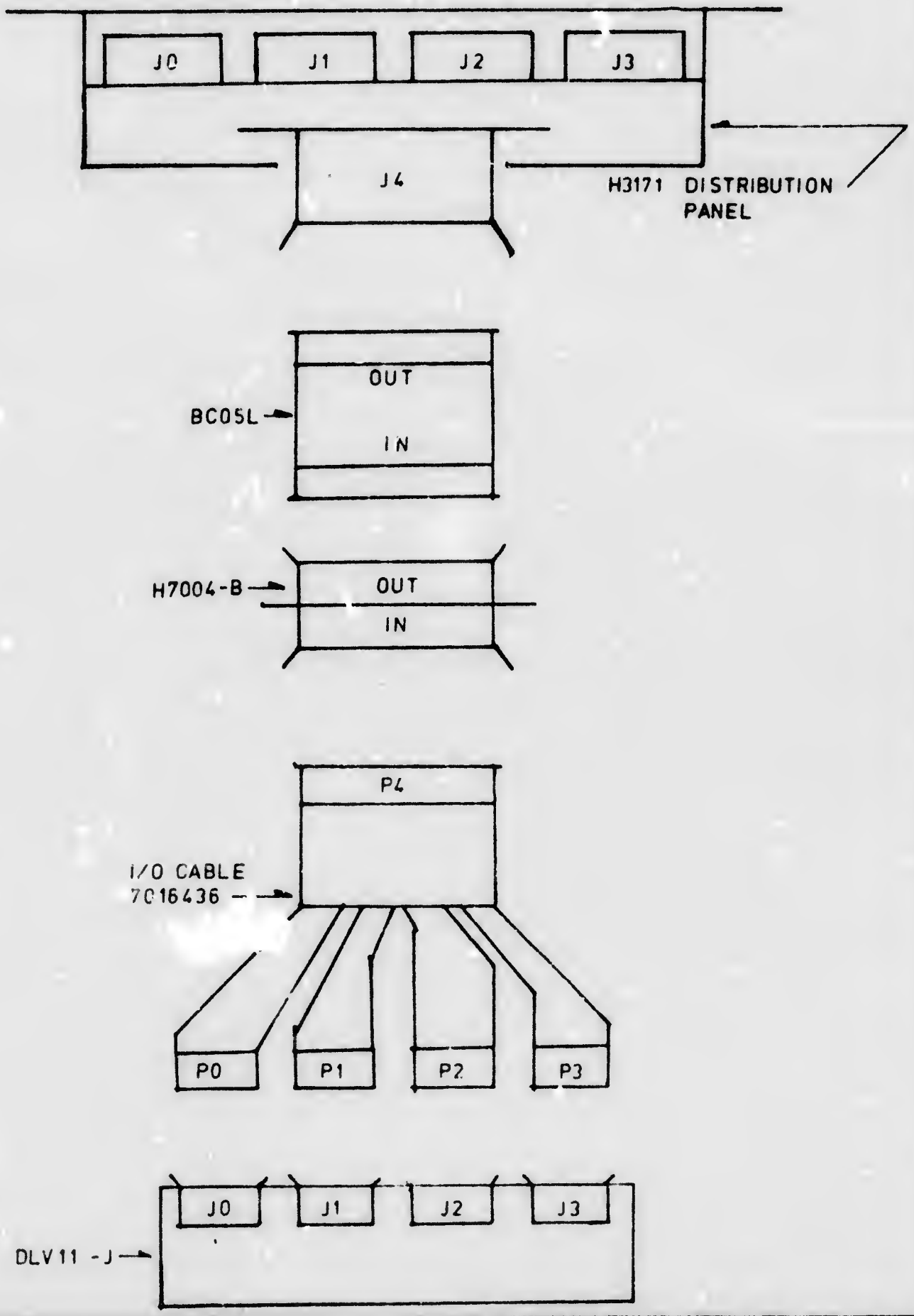
B) H3171-B (Integral Filter)
This configuration is used in conjunction with CPU boxes that do not contain a bracket for static filters. In this case the H3171 chassis is elongated to accept the static filter directly onto the distibution panel.

Each H3171 consists of 4 major assemblies. (See figure 1 in Appendix A)

1) Distribution Panel / Chassis (includes output connectors)
2) BC05L Cable
3) H7004-B Filter
4) I/O Cable (7016436)

TITLE M.A.S.T.

FIG. 1



	SIZE	CODE	NUMBER	REV
	A	SP	MA-A5324-0-0	C

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 3/10/80

TITLE M.A.S.T. DL11-W

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	Update old Back-up	MA-A0000-ML009	L.ELCLERC	8-80	S. ESTES	8-80

3

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Ayotte	Susan Estes	A	SP	MA-A5330-0-0	B

DL11-W

1.0 INTRODUCTION

The DL11-W is a single line asynchronous communication interface to the PDP11 Unibus. The DL11-W contains the functionality of the DL11-A, -B, -C, and -D options. The DL11-W also contains a line frequency real time clock (RTC) used for timed interrupts and software timekeeping.

The serial line unit (SLU) portion of the DL11-W has such features as split speed, odd/even/no parity select, active/passive 20 ma. interface, EIA RS232C (data only) interface, and a 5 to 8 bit character length. These parameters and features are switch selectable.

2.0 REFERENCE DOCUMENTATION

2.1 Manuals & Engineering Specifications

2.1.1 DL11-W SLU/RTC Maint. Manual EK-DL11W-MM

2.2 Prints & Schematics

2.2.1 Field Maintenance Print Set MP00106

3.0 REQUIRED TEST EQUIPMENT

3.1 Hardware and Media

3.1.1 PDP11 system with 8K of memory
3.1.2 Quad SPC slot
3.1.3 DVM accurate to .01V at 15VDC
3.1.4 EIA or 20 ma. terminal

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 FLOAT PROGRAM ..... DZFLA
4.2 DL11-W DIAGNOSTIC ..... CZDLD

5.0 SPECIAL INSTRUCTIONS

The DL11-W is comprised of a quad height module (M7856), which plugs into a PDP11 SPC slot. The four option variations are listed below:

OPTION	DESCRIPTION
DL11-W	M7856 SLU/RTC Module
DL11-WA	DL11-W, 70-08360-01 20 ma. Cable
DL11-WB	DL11-W, BC05C-25 EIA Cable
DL11-WC	DL11-W, BC03L-10 filtered panel mount EIA Cable.

6.0 INSTALLATION AND TEST SET-UP INSTRUCTIONS

The M7856 Module has many features and several operating modes which must be configured via the 5 switch packs prior to installation. Refer to FIGURE 1 for switch location.

6.1 FLOAT PROGRAM

6.1.1 Run the FLOAT program (DZFLA) to determine the correct address and vector settings for the DL11-W(s). Note that this only applies to DL11-W's that are not used for consoles.

6.2 MODE & ADDRESS SELECTION

6.2.1 The M7856 Module may be run in one of 3 modes:

MODE 1 - As a console interface with the RTC enabled. The SLU address is 777560 and the RTC address is 777546.

MODE 2 - As a SLU ONLY with the RTC DISABLED. The SLU address range is 774000 to 777770.

MODE 3 - As a RTC ONLY with the SLU DISABLED. The RTC address is 777546.

*** NOTE ***

For DL11-W's which will NOT use the RTC logic, remove R63. See FIGURE 1 for location.

Refer to TABLE 1 for switch selection of ADDRESS and MODE.

6.3 VECTOR ADDRESS SELECTION

6.3.1 Vector address selection is accomplished by setting the switch pack S2. The DL11-W uses three vectors: one for the receiver, one for the X-mitter, and one for the real time clock. The X-mitter vector (XX4) is automatically selected when the receiver vector (XXØ) is set. If the DL11-W is being used as a console, the receiver vector should be set to 6Ø. The vector for the RTC is fixed at 1ØØ. Refer to TABLE 2 for switch settings.

6.4 BAUD RATE SELECTION

6.4.1 Split speed on the M7856 may be attained by setting the transmit and receive speed select switches to their desired values. If split speed is not desired, set the transmit and receive select switches to the same speed settings. Refer to TABLE4 for the switch settings.

6.5 2Ø ma. ACTIVE/PASSIVE OPERATION

6.5.1 If the DL11-W is to be used as a 2Ø ma. interface, the X-mitter, receiver, and paper tape reader enable functions must be set as either ACTIVE or PASSIVE. The normal setting is for active transmitter, active receiver, and active paper tape reader enable. Refer to TABLE 5 for these switch settings.

6.6 MISCELLANEOUS SWITCH FUNCTIONS

6.6.1 The BREAK ENABLE function is selected by setting SW4-1 ON. The normal setting is OFF.

6.6.2 ODD PARITY is selected by setting SW4-2 ON. (See 6.6.5) The normal setting is ON.

6.6.3 CHARACTER LENGTH is selected by SW4-3 and -4 (Refer to TABLE 3). The normal settings are OFF.

6.6.4 STOP BITS are selected by SW4-5. ON=1 stop bit, OFF=2 stop bits. (1.5 stop bits if 5 bits per character) The normal setting is OFF.

6.6.5 PARITY is enabled if SW4-6 is ON. The normal setting is ON.

6.7 Install the M7856 Module in a Quad SPC slot and connect the cable to the berg connector on the module.

6.8 Connect an appropriate terminal (EIA or 20 ma.) to the DL11-W.

7.0 POWER CHECKS

7.1 Verify the presence of the following voltages at the module pins indicated:

VOLTAGE	MODULE PIN
+5VDC +/- .25V	CA2
+15VDC +/- .75V	CU1

8.0 DIAGNOSTIC TEST PROCEDURE

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria, e.g.: Pass Counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the "CHECKLIST".

The DL11-W diagnostic contains three separate tests which are to be run on the serial line unit. Testing of the real time clock is done in the DATA TEST.

8.1 DL11-W DATA TESTS ..... CZDLD

8.1.1 The DATA TEST is capable of testing the console interface and up to 15 consecutively addressed and vectored SLU's. The diagnostic assumes the following parameters: the console address is 777560 and the vector is 60. The first of any additional SLU's is addressed at 776500 and vectored at 300. The diagnostic will autosize any DL11-W's which fall within this range.

8.1.2 Start the DATA TESTS at address 200 and set the switch register for the desired functions.

SWITCH	FUNCTION
15	Set to halt on error
14	Set for scope loop
13	Set to inhibit error typeout
12	Unused
11	Unused
10	Set to enable error flag tests
9	Set to loop on error
8	Set to enable break function tests
7	Set to enable data tests with turnaround (H315)
6	Set to inhibit RTC tests (console only)
5	Set to set-up device map (inhibit auto-size)
4	Set to inhibit SLU tests

8.1.3 The console will report the number of units being tested and an END-OF-PASS message will be printed after all units have been tested.

8.2 DL11-W ECHO TEST ..... CZDLD

8.2.1 To run the ECHO TEST on the console terminal, start at address 204. An asterisk (*) will be printed at the terminal to indicate that the test has started. Type a few printable characters at the terminal and verify that they are echoed back to the terminal correctly.

8.2.2 If the unit under test is not the console interface, it will be necessary to modify the following program locations to reflect the parameters of the unit under test. Make sure a terminal is connected to the DL11-W.

NAME	LOCATION	CONTENTS
CRCSR	2654 *	Address of receiver status register
CRBUF	2656	Address of receiver buffer register
CTCSR	2660	Address of transmitter status register
CTBUF	2662	Address of transmitter buffer register
CRVECT	2664	Receiver vector
CRPSW	2666	Receiver vector plus 2 (PSW)
CTVECT	2670	Transmitter vector
CTPSW	2672	Transmitter vector plus 2 (PSW)

* - CZDLD REV D

8.2.3 Run the ECHO TEST as described in step 8.2.1. Repeat step 8.2.2 for every DL11-W to be tested.

8.3 CHARACTER TEST ..... CZDLD

8.3.1 To run the CHARACTER TEST on the console terminal, start at address 210. The terminal will print 32 characters per line and will repeat every third line. Typing any character at the terminal will halt the test. A typical pattern is shown below:

```
!"#$%&'()*+,->/0123456789:;<=>?
@ABCDEFGHIJKLMNOPQRSTUVWXYZ(\)^_
'abcdefghijklmnopqrstuvwxyz(!)-~
```

8.3.2 If the unit under test is not the console interface, it will be necessary to modify the following program locations to reflect the parameters of the unit under test. Make sure a terminal is connected to the DL11-W.

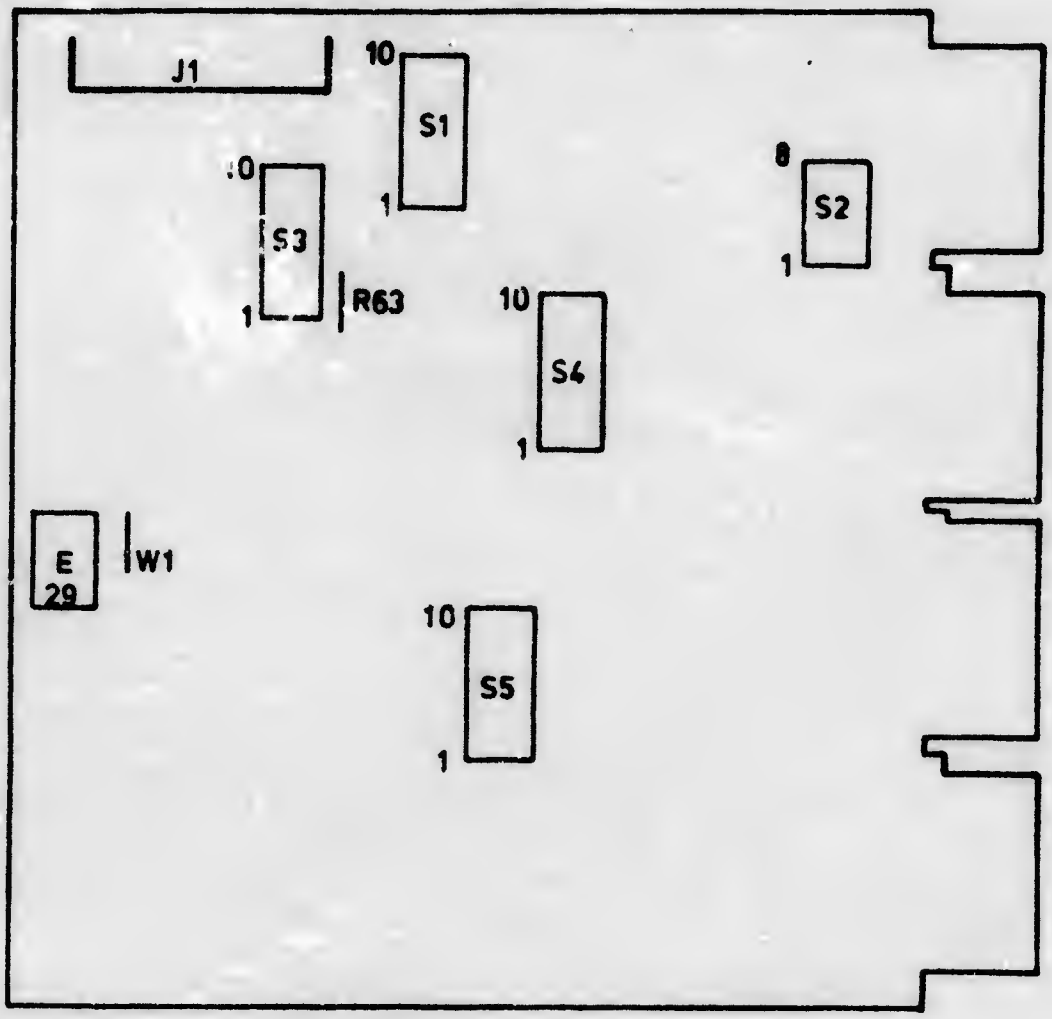
NAME	LOCATION	CONTENTS
CRCSR...	2654 *	Address of receiver status register
CRBUF...	2656	Address of receiver buffer register
CTCSR...	2660	Address of transmitter status register
CTBUF...	2662	Address of transmitter buffer register
CRVECT..	2664	Receiver vector
CRPSW...	2666	Receiver vector plus 2 (PSW)
CTVECT..	2670	Transmitter vector
CTPSW...	2672	Transmitter vector plus 2 (PSW)

* - CZDLD REV D

8.3.3 Run the CHARACTER TEST as described in step 8.3.1. Repeat step 8.3.2 for every DL11-W to be tested.

FIGURE 1

M7856 MODULE LAYOUT



NOTES -

R63 must be removed if the RTC is disabled.

The Berg connector, J1, contains a 70-0860 cable for the DL11-WA option; a BC05C-25 for the DL11-WB option and a BC03L-10 for the DL11-WC option.

Jumper W1 must always be installed.

TABLE 1

ADDRESS AND MODE SELECTION TABLE

ADRS BIT	A10	A09	A08	A07	A06	A05	A04	A03	LTC	LTC
SW S5	-3	-2	-1	-4	-5	-6	-8	-7	-9	-10
MODE 1	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
MODE 2	--	--	--	--	--	--	--	--	ON	OFF
MODE 3	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON

NOTES - A switch set to ON equals a logical 0 and a switch set to OF is equal to a logical 1.

The switch settings for mode 1 selector an address of 777560 (console) and the RTC (or LTC) address is 777546.

The address switch settings for mode 2 are user defined to select any address from 774000 to 777770. The RTC is disabled.

The switch settings for mode 3 select the RTC (or LTC) address as 777546 and the SLU is disabled.

T

VECTOR ADDR[illegible]ECTION TABLE

SWITCH	IS	TO SELECT VECT BIT
S2-4	ON	3
S2-6	ON	4
S2-3	ON	5
S2-5	ON	6
S2-7	ON	7
S2-8	ON	8

TABLE 3

CHARACTER LENGTH TABLE

LENGTH	S4-4	S4-3
5 BITS	ON	ON
6 BITS	ON	OFF
7 BITS	OFF	ON
8 BITS	OFF	OFF

TABLE 4

SPEED SELECTION TABLE

BAUD	RECEIVER			TRANSMITTER		
	S3-2	S3-3	S3-5	S4-10	S3-1	S3-4
110	OFF	OFF	OFF	ON	ON	ON
150	ON	OFF	OFF	OFF	ON	ON
300	OFF	ON	ON	ON	OFF	OFF
600	OFF	ON	OFF	ON	OFF	ON
1200	OFF	OFF	ON	ON	ON	OFF
2400	ON	ON	ON	OFF	OFF	OFF
4800	ON	ON	OFF	OFF	OFF	ON
9600	ON	OFF	ON	OFF	ON	OFF

TABLE 5

20 MA. ACTIVE/PASSIVE SELECTION TABLE

TRANSMIT	S1-1	S1-2	S1-3	S1-6	S1-7
ACTIVE	ON	ON	OFF	OFF	ON
PASSIVE	OFF	OFF	ON	ON	OFF

RECEIVE	S3-6	S3-7	S3-8	S3-9	S3-10
ACTIVE	ON	OFF	ON	OFF	ON
PASSIVE	OFF	ON	OFF	ON	OFF

PT RDR ENA	S1-4	S1-5	S1-8	S1-9	S1-10
ACTIVE	ON	OFF	ON	OFF	ON
PASSIVE	OFF	ON	OFF	ON	OFF

NOTE - Normal operation is to select active transmit, active receive, and active paper tape reader enable.


A55T10

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KW11-L - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5510					

ENG	APPD	SIZE	CODE	NUMBER	REV
Ion Jelenievski		A	SP	MAA5510-0-0	A

KW11-L

Line Frequency Clock Test

ABSTRACT

This program tests the KW11L line frequency clock. It validates proper operation under both interrupt and non-interrupt modes. It requires the operator to monitor its operation with a clock capable of measuring time in seconds.

REQUIREMENTS

PDP-11 with KW11L

STORAGE 0 - 2000

[redacted] lute Loader

EXECUTION TIME 1 minute

STARTING PROCEDURE 200 = 60 HZ, Line Frequency
202 = 50 HZ, Line Frequency
Load appropriate address to switch register and depress start switch

PRINTOUTS Yes

SWITCH REGISTER OPTIONS No

REFERENCE DOCUMENTS

Printset KW11-L Drawing Directory
Manual DEC-11-HKWB-D
MainDEC-11-DZKWA-A-D
MainDEC-11-DZKWA-A-PB

The device address is 777546 and vector address is 100. It's on bus request level 6. It is also rated at one (1) bus load.

To be mounted in an 11/35 or 11/40

The module location is slot F-3. Remove wrie F3R2 to F3V2.

To be mounted in an 11/45 or 11/50

The module location is slot C1. Remove write C1R2 to C1V2.

End of pass

This test rings the teletype bell at the completion of several different time intervals over a period of one minute. From the time this test beigns, the bell will ring at the end of 1,2,3,4,5,10,20,30,40,50, and 60 seconds, it will then repeat this sequence as long as desired. For veri ication of this option the test should 15 minutes.

A5520

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KW11P - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5520					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jeleniewski		A	SP	MAA5520-0-0	A

KW11P

ABSTRACT

This program tests the KW11-P Real Time Clock. It contains a series of incremented routines that test the control and status register, count set buffer, counter, and interrupt vector address using 100KHZ, 10KHZ, and 60 or 50EZ using the external input with a temporary jumper on the backplane to the LTCL pin (50 or 60HZ). There is also a provision for running two KW11P's simultaneously (one a "COW" or Known Good) and comparing the two.

REQUIREMENTS

PDP-11
KW11-P

STORAGE

This program occupies memory from 0 to 4664.

LOADING

Absolute Loader

EXECUTION TIME

Basic test requires 15 sec. per pass.

STARTING PROCEDURE

200 Basic Test
204 Restart Address Primarily Used by XOR Tester
210 Timing Test
214 Double or Single Real Time Clock Test 100KHZ
220 Double or Single Real Time Clock Test 10KHZ
224 Double or Single Real Time Clock Test 60HZ
230 Double or Single Real Time Clock Test 50HZ

PRINT OUTS

With switches 12 thru 15 equal to "0" (Down) the program will print on errors and continue in test. Bell will ring at completion of a pass.

SWITCH REGISTER OPTIONS

SW15 = 1 or UP ... Halt on Error
SW14 = 1 or UP ... Scope Loop
SW13 = 1 or UP ... Inhibit Printout
SW02 = 1 or UP ... Clock 2 (cow) Present - execute repeatability tests (T25 + T26)
SW00 = 1 or UP ... Suppress Tests using external frequency

DOUBLE REAL TIME CLOCK TESTING

Using the same diagnostic as before, double real time clock testing may be accomplished. One clock is the one under test and the other is a "Known Good" or COW board.

To convert a standard P clock to a "COW" Module:

1. Remove jumper A4
   CSR = 772560
   CSB = 772562
   CTR = 772564

2. Add jumper V8
   Vector Location is 504
   PSW Location is 506

NOTE: This vector is in floating vector space, caution is advised with respect to allowing vector conflicts with other devices on the system.

PROCEDURE FOR DUAL CLOCK REAL TIME CLOCK TEST

1. Load address 214, depress start (100KHZ Test).

2. Enter the time via the TTY keyboard.

3. Set the switches in the switch register to 000005. The TTY will print the time at 5 second intervals.

4. Consecutive printout will be written 5.00 plus or minus .01 seconds of each other. Allow the test to run for at least 10 printouts. If the tolerance is exceeded, the clock under test is defective.

5. Load address 220, depress start (10KHZ Test).

6. Repeat steps 2-4.

7. Load address 224, if 60HZ; or 230 if 50HZ; depress start (line frequency test).

8. Repeat steps 2 and 3.

9. Consecutive printouts will be within 5.00 plus or minus .04 seconds of each other. Typically, and 5.00 plus or minus .2 seconds worst case due to possible AC line frequency variations allow the test to run for at least 10 printouts. If the tolerance is exceeded the clock "Under Test" is defective.

A553-530

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KW11W ACCEPTANCE PROCEDURE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5530					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekerkewski	Tom	A	SP	MAA5530-0-0	A

KW11W ACCEPTANCE PROCEDURE

I. TEST EQUIPMENT REQUIRED

1. PDP-11 Computer
2. 453 Tektronix Scope or Equivalent
3. KW11-W Option & Print Set
4. M7823 (Watchdog timer)
5. M105 (Address selector)
6. M7821 (vector address selector)
7. TTY

II. MAINDECS REQUIRED

1. DZKWC-C-PB/D

III. EQUIPMENT SET-UP

1. To exercise the KW11-W option, all jumpers mu . be installed on M7823. The test connector 7009463 must be used on KW11-W logic test.

IV. OPERATOR ACTION

1. Load MAINDEC-11-DZKWG-C into PDP11 using absolute loader. Refer to program write-up, MAINDEC-11 DZKWC-C-D.

2. Load and start 200. The TTY will respond as follows:
   First device address:
   The operator responds by inputting 6 characters plus a carriage return on the keyboard.
   Example: First device address 772400 CR

   2.1 The TTY responds as follows:
   First Int. Vector =
   The operator must respond by inputting 3 characters plus a carriage return on the keyboard.
   Example: First int. Vector = 350 CR

   2.2 The TTY will respond as follows:
   Priority int. Level =
   The operator responds by inputting 1 character & CR (using Floating Vector, refer to system configuration, should be between DQ11 & DU11.)
   Example: Priority int. Level = 7 CR

IV. OPERATOR ACTION (Continued)

3. Running the Logic Test:
The TTY will respond with the following:
Logic Test (1), Delay Test (2)*, Dynamic (3)
The operator responds by inputting on the keyboard "1" with a carriage return for Logic test,
The TTY will respond:
1
Logic Test
This test, upon completion, will type out "pass" this test should run for a minimum of 5 minutes.

* Delay test (2) is part of adjustment procedure.

Note: To run the Logic test, the supplied test plug must be connected to the module connector. The T 3 delay must exceed T 2 by 50 microseconds. The adjustment of T 1 must be set to a minimum. For details on other adjustments see KW11-W adjustment procedure - A-SP-KW11-W-3.

4. Running the Dynamic Test
Put bit 00 in the switch register to get back into the monitor or halt machine and load and start 240. If the operator has gone back into the monitor, a keyboard input must be used. Type in "3", carriage return (CR). Dynamic test begins.

On every 100 completions of Dynamic Test, the TTY will type "pass". This test should run for a minimum of 15 minutes.

Acceptable Errors

1. None

5. Procedure for Restart After Error or Fix
1. If an incorrect character is typed while inputting on the TTY, the operator may type a run out and repeat the entire line.

2. Starting address 1000 - direct start or restart of Logic test.

3. Starting address 220 - direct start or restart of delay adjustment test.

A55540

DIGITAL EQUIPMENT CORPORATION
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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KW11-K DUAL PROGRAMMABLE REAL TIME CLOCK - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5540					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Seligman	for Dick	A	SP	MA5540-0-0	A

MANUFACTURING SPECIFICATION

TITLE MODULAR APPROACH TO SYSTEMS TEST - APPENDIX A

KW11-K DUAL PROGRAMMABLE REAL TIME CLOCK

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic write-up for purposes of expediency. All instructions contained in this procedure are brief and direct for reasons of simplification, so not to confuse the operator when performing diagnostic testing. For more in-depth testing information, it will be necessary to refer to the diagnostic write-up.

2.0 REFERENCE DOCUMENTS

The documents listed below are for reference only.

2.1 Workmanship Manual

2.2 KW11-K User's Manual EK-KW11-K-OP-001 or later revision

2.3 KW11-K Printset B-TC-KW11-K-1

2.4 KW11-K System Checkout and Acceptance Procedure A-SP-KW11-K-2

3.0 REQUIRED TEST EQUIPMENT

3.1 PDP-11 CPU

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC-11-DZKWK KW11-K Diagnostic and Write-up.

4.2 MAINDEC-11-DZKWK DEC-X11 KW11-K Exerciser and Write-up.

5.0 SPECIAL INSPECTION AND CHECKS

5.1 None

6.0 TEST SET-UP

6.1 Set-up address and vector

7.0 SYSTEM INTEGRATION TEST PROCEDURE

7.1 Load diagnostic into system under test using low or high speed tape reader, XXDP, or ACT-11.

	SIZE	CODE	NUMBER	REV
	A	SP	MAA5540-0-0	A

7.2 Program Start-Up

7.2.1 Load Address 200.

7.2.2 Start SR = 000000 (Standard Default Condition)

7.3 Switch Register Settings

7.3.1 SR15 = Halt on Error

7.3.2 SR14 - Loop on Test

7.3.3 SR13 - Inhibit Error Printout

7.3.4 SR12 - Inhibit Special Test Typeout

7.3.5 SR11 = Inhibit Iterations

7.3.6 SR10 = Bell on Error

7.3.7 SR9 = Loop on Error

7.3.8 SR8 = Loop on Test in SR 0-7

7.4 Operator Action

The operator should observe non-erroring passes per appropriate checklists. Each pass takes approximately 4 minutes.

7.5 Acceptable Errors

There are no acceptable errors.

7.6 Procedure # Restart After Repair

7.6.1 Repeat steps 7.2 thru 7.5.

7.7 DEC-X11 and AD11-K Installed

7.7.1 Refer to AD11-K Mfg. and Field System Acceptance Procedure A-SP-AD11-K-5 Section 7 for interactive testing.

A5550

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KWV11-A REAL TIME CLOCK (11/03) - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	Prev. 7668001-0-5550					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jeberiewicz	Tom	A	SP	MAA5550-0-0	B

KWV11-A REAL TIME CLOCK (11/Ø3)

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeup for the purpose of expediency. The procedure has been kept brief, and to the point, to keep from confusing the user. For additional information, it will be necessary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD 116)

2.2 A-SP-KWV11-A-2 Engineering Specification

2.3 EK-ADV11-OP-ØØ1 ADV11-A, KWV11-A, AAV11-A, DRV11 Users Manual

2.4 11LO3 Manufacturing Specifications

2.5 Microcomputer Handbook EB-07948

3.0 REQUIRED TEST EQUIPMENT

3.1 LSI11 Standard Computer

3.2 KWV11-A Module

3.3 Output terminal/DLV11

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC-11 - DVKWA KWV11-A Diagnostic and Writeup

4.2 MAINDEC-11 - DXKWF DEC/X11 Exerciser and Writeup

5.0 SPECIAL INSTRUCTIONS AND CHECKS

5.1 If the system contains an H322 signal distribution panel, connect the KWV11-A by means of a BCØ8R cable, J1 of module to J5 of the H322. (all 11LØ3 systems)

5.2 When an ADV11-A and a KWV11-A are both present in the system, module jumpers (DEC 7010771) are installed from the KW output tab (CLK) to the A/D clock overflow tab (C) and from the KW tab (STI) to the AD tab(s).

6.0 TEST SET UP

6.1 Insure switch packs S1 and S3 are set for a device address of 170420 and a vector address of 440 respectively.

6.2 Insure all switches of switch pack S2 are turned off.

6.3 Install module in CPU slots A thru DØ2 of all 11LØ3 systems.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 KWV11-A Test Diagnostic (DVKWA)

7.1.1 Load program through appropriate load media.

7.1.2 Program starting addresses.

	7.1.2.1	200 - Start of logic tests
	7.1.2.2	204 - Restart address for logic tests
*	7.1.2.3	210 - IO signal test #1
*	7.1.2.4	214 - IO signal test #2
*	7.1.2.5	220 - IO signal test #3
	7.1.2.6	230 - Production starting address
	7.1.2.7	240 - Tester starting address

* For Field use only.

7.1.3 Alternate software SR settings (176)

7.1.3.1	SWR15 = 1	Halt on error
7.1.3.2	SWR14 = 1	Loop on test
7.1.3.3	SWR13 = 1	Inhibit error typeout
7.1.3.4	SWR12 = 1	Enable line frequency rate testing
7.1.3.5	SWR11 = 1	Inhibit iterations (short pass)
7.1.3.6	SWR10 = 1	Bell on error
7.1.3.7	SWR 9 = 1	Loop on error
7.1.3.8	SWR 8 = 1	Loop on test in SWR <7:0>

NOTE: The software switch register may be changed at any time by typing Control C. If you wish to keep the current value, type <CR>. If you wish to change the value, type the new value followed by a <CR>.

7.1.4 Operator Action

7.1.4.1 Set all SWR bits as desired (default 000000)

7.1.4.2 Type 200G.

7.1.5 Evidence of End of Pass and Run Time at End of Pass typeout will resemble the following example:

"END PASS 1 - Total errors 0 - Good units 00000000 00000001" First Pass runs without iterations and takes 30 seconds, subsequent passes run with iterations and take 2.5 minutes.

7.1.6 Acceptable errors: None

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AA11 DIGITAL/ANALOG CONVERTER - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6110					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jeleniewski		A	SP	MAA6110-0-0	A

AA11 DIGITAL/ANALOG CONVERTER

1.0 AA11 SET-UP AND CALIBRATION

Refer to document A-SP-AA11-D-7

1.1 Diagnostic Package

(A) Calibration Test MainDEC-11-D6BA

(B) Scope Options Test MainDEC-11-D6CA

1.2 Other Related Documents

(A) AA11-D D/A Sub-System Manual DEC-11-HAAC-D


A61715

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AAV11-A 4 CHANNEL 12 BIT D/A FOR PDP-11/03 - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6115					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekowski	Tom	A	SP	MAA6115-0-0	A

AAV11-A 4 CHANNEL 12 BIT D/A FOR PDP-11/03

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeup. For the purpose of expediency, the procedure has been kept brief and to the point, to keep from confusing the user. For additional information, it will be necessary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD 116)

2.2 Engineering Specification A-SP-AAV11-A-3

2.3 User's Manual EK-ADV11-OP-001

2.4 AAV1 rint Set

3.0 REQUIRED T..T EQUIPMENT

3.1 LSI-11 Standard Computer

3.2 Oscilloscope 453 or equivalent

3.3 DVM - 5 digits or accurate null meter

3.4 AAV11-A module

3.5 Output terminal/DLV11

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC 11 - DVAAA AAV11-A Test Diagnostic and Write up

4.2 MAINDEC 11 - DXAAC DEC/X11 Exerciser and Write up

5.0 SPECIAL INSTRUCTIONS AND CHECKS

5.1 RF Shield provided with AAV11-A must be installed over Side 1 (component) of module.

5.2 If an H322 Distribution Panel is present, then connect AAV11-A by means of a BC08-06 cable from J1 of module to J10 of the H322 (all H and J variations of 11L03)

6.0 TEST SET UP

6.1 Insure switch pack S1 set up for a device address of 170440. No vector is set up since the AAV11-A is not capable of interrupting.

6.2 Install module in Expander Box (BA11-M) slot A thru D03 of all H and J variations of 11L03's.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 AAV11-A Test (DVAAA)

7.1.1 Load program through appropriate load media.

7.1.2 Available tests and their starting addresses:

ST. ADD	TEST
200	Manual Logic Test
204	Manual Ramp Test
210	Manual Static Calibration
214	Manual Dynamic Calibration

7.1.3 Alternate Software SR settings (loc 176)

7.1.3.1 SWR15 = 1 Halt on error
7.1.3.2 SWR14 = 1 Loop on test
7.1.3.3 SWR13 = 1 Inhibit error typeouts
7.1.3.4 SWR11 = 1 Inhibit iterations
7.1.3.5 SWR10 = 1 Bell on error
7.1.3.6 SWR 9 = 1 Loop on error
7.1.3.7 SWR 8 = 1 Loop on test in SWR<7:0>

7.1.4 Operator Action

7.1.4.1 Set SWR bits as desired
7.1.4.2 Type 200G (for logic test)

NOTE: For detailed information on manual ramp test, manual static calibration test, and manual dynamic calibration test, refer to engineering specifications SP-AAV11A-3

7.1.5 Evidence of End of Pass and Run Time

"END PASS #XXXXX" is typed in 5 seconds with no iterations and in 20 seconds with iterations.

7.1.6 Acceptable Errors: None

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE ADO1-D A/D CONVERTER - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6120					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM JELENIEWSKI		A	SP	MAA6120-0-0	A

AD01-D A/D CONVERTER

1.0 AD01-D SET-UP AND CALIBRATION

Refer to document DEC-11-HADDA-C-D

1.1 AD01-D Acceptance Procedure

Refer to document A-SP-AD01-D-12

1.2 Diagnostic Package

(A) AD01-D Logic and Calibration Test
MainDEC-11-D6AB

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE LPA11-K LABORATORY PERIPHERAL ACCELERATOR - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6124					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelonkiewicz		A	SP	MAA6124-0-0	A

LPA11-K LABORATORY PERIPHERAL ACCELERATOR

INTRODUCTION

This LPA11-K procedure establishes minimum checkout specifications for FA&T, along with configuration requirements.

1.0 TEST EQUIPMENT

1.1 Oscilloscope (100 MHz bandwidth min.)

1.2 Quad Extender Module (W984)

1.3 Hex Multilayer Extender Module (W9048)

1.4 Tektronix Model 7D01 Logic Analyzer with DFI Display Formatter (or equivalent) is recommended but not required.

2.0 TEST SOFTWARE

2.1 MP00479 LPA11-K Field Maintenance Print Set

2.2 MP00161 AA11-K Field Maintenance Print Set

2.3 MP00047 AD11-K Field Maintenance Print Set

2.4 MP00090 AM11-K Field Maintenance Print Set

2.5 B-DD-DR11-K DR11-K Customer Print Set

2.6 MP00048 KW11-K Field Maintenance Print Set

2.7 B-DD-AR11-0 AR11 Customer Print Set

2.8 B-DD-LPS11-S LPS11 Customer Print Set

2.9 EK-LPA11-SM-001 LPA11-K Installation and Maintenance Manual

2.10 EK-KMC11-OP-001 KMC11-A Maintenance Manual

2.11 ZJ252-RB LPA11-K Diagnostic Package

2.12 ZJ234-RB KMC11-A Diagnostic Package

2.13 MAINDEC-11-DXLPF DEC-X-11 Multiuser Mode Micro Code Loader

2.14 MAINDEC-11-DXLPG DEC-X-11 Dedicated Mode Micro Code Loader

2.15 MAINDEC-11-DXLPH DEC-X-11 LPA11-K Exerciser

2.16 A-SP-LPS11-14 LPS11 Acceptance Procedure

3.0 CHECKOUT OF AN LPA11-K WITH "K" OPTIONS

There are many possible configurations for the LPA11-K. Therefore, configuration of the system cannot be specifically given for all cases. The LPA11-K must be configured according to the guidelines given in the LPA11-K Installation and Maintenance Manual. Checkout of the LPA11-K can proceed as soon as configuration has been completed. Checkout of an LPA11-K with "K" options is as follows:

3.1 Make sure all device addresses, vector addresses and priority levels of the Basic LPA11-K and any additional options on the LPA11-K's I/O Bus are set according to Appendix A of this document.

3.2 Make sure that Switch 7 of E76 on the M8200-YC is set to the "OFF" position.

3.3 Make sure that Jumper W1 is installed on the M8254.

3.4 Make sure that the I/O Bus has at least an AD11-K and a KW11-K on it.

3.5 Load MAINDEC-11-DRLPA (LPA11-K System Test). Follow operating instructions contained in the write up for this diagnostic. Do not patch locations "SR1:" and "SR2:". Allow the program to run in its default condition (1 AD11-K and 1 KW11-K). This will be a quick check to see that the Basic LPA11-K is functioning properly. Allow at least four (4) non-erroring passes. If there is an error, refer to the trouble-shooting flowchart in Appendix B.

3.6 The following checkout instructions will assume a maximum LPA11 System (5 DR11-K's, 1 KW11-K, 2 AD11-K's, and 1 AA11-K). Omit the sections pertaining to any options that are not included in the configuration that is being tested.

3.7 Load MAINDEC-11-DRLPF (LPA/DR11-K Digital I/O Test). Follow operating instructions contained in the writeup for this diagnostic. All DR11-K's on the LPA11-K's I/O Bus will be checked by this diagnostic. If an error occurs, fix or replace the failing DR11-K. The diagnostic must be allowed to make at least four (4) non-erroring passes.

3.8 Load MAINDEC-11-DRLPG (LPA11/KW11-K Diagnostic). Follow operating instructions contained in the writeup for this diagnostic. Interrupt logic is not checked by this diagnostic. If an error occurs, fix or replace the failing KW11-K. The diagnostic must be allowed to make at least four (4) non-erroring passes.

3.9 Load MAINDEC-11DRLPK (LPA11/AD11-K Diagnostic). Follow operating instructions contained in the writeup for this diagnostic. Check and calibrate the AD11-K (s) according to A-SP-AD11-K-5 which is included in the AD11-K Field Maintenance Print Set. Use of this diagnostic appears to the user the same as if the DZADL diagnostic was being run on an AD11-K on the Unibus. Interrupt logic on the AD11-K is not checked by MD-11-DRLPK.

NOTE: Allow a 15 minute warmup for the AD11-K(s) before calibration. Allow the diagnostic to make at least two (2) non-erroring passes of "Auto Test" after calibration is completed. Make sure the G5036 wraparound module is in place and that the switch is in the "0" position.

If an AM11-K (Multiple Gain Multiplexer) is to be installed on the system, do so at this time. Refer to A-SP-AM11-K-5 (AM11-K Manufacturing and Field Acceptance Procedure) for installation and checkout. Use MAINDEC-11-DRLPB instead of MAINDEC-11-DZADL. Omit reference to MD-11-DXKBA (DEC/X11 Module).

3.10 Load MAINDEC-11-DRLPB (LPA11/AA11-K diagnostic). Follow operating instructions contained in the writeup for this diagnostic. Checkout and calibrate the AA11-K according to A-SP-AA11-K-5 (AA11-K Manufacturing and Field Acceptance Procedure). MD-11-DRLPB will appear to the user the same as if MD-11-DZAAC were being run on an AA11-K on the Unibus. However, the interrupt logic on the AA11-K will not be checked and the settling test square wave will not be generated. Omit references to running MD-11-DXAAB (DEC/X11 Module).

3.11 Load MAINDEC-11-DRLPA. Follow operating instructions contained in the writeup for this diagnostic. The address of locations "SR1:" and "SR2:" may be found in the symbol table at the back of the listing. Load location "SR1:" with the appropriate bits to inform the diagnostic as to which options are on the LPA11-K's I/O Bus. Load location "SR2:" with the appropriate bits to inform the diagnostic as to how the options are set up for test. The FA&T area will have G5036 wraparound modules on all AD11-K's present. Set the switches on the G5036's to the "0" position. G5036 wraparound modules are optional in the field. All DR11-K's will have the one foot BC08R wraparound cable installed; if an AA11-K is present, it will have one of the display scopes connected (as described in A-SP-AA11-K-5).

Allow MAINDEC-11-DRLPA to make a minimum of six (6) non-erroring passes. If an error does occur, refer to the troubleshooting charts in Appendix B.

4.0 CHECKOUT OF AN LPA11-K WITH AN AR11

4.1 Configure the LPA11-K with an AR11 analog realtime subsystem that has previously been checked out and accepted according to the AR11 System Installation and Checkout Procedure (A-SP-AR11-0-4). Follow configuration guidelines given in the LPA11-K Installation and Maintenance Manual (EK-LPA11-SM-001).

4.2 Set the Device Address of the AR11 to 770400. Set the Vector Address to 340.

4.3 Set the Device Address, Vector Address and Priority Level of the Basic LPA11-K according to Appendix A of this document.

4.4 Make sure that Switch 7 of E76 on the M8200-YC is set to the "OFF" position.

4.5 Make sure that Jumper W1 is installed on the M8254.

4.6 Make sure a G5036 wraparound module is connected to the AR11 in the FA&T area. Set the switch to the "0" position. The G5036 wraparound module is optional in the field.

4.7 Load MAINDEC-11-DRLPA (LPA11-K System Test). Follow operating instructions contained in the writeup for this diagnostic. Patch location "SR1:" to 002000. Patch location "SR2:" to 002000 if the G5036 is present. Allow the diagnostic to make at least six (6) non-erroring passes. If an error does occur, refer to the troubleshooting flowcharts in Appendix B.

5.0 CHECKOUT OF AN LPA11-K WITH AN LPS11

5.1 Configure the LPA11-K with an LPS11 Laboratory Peripheral System that has previously been checked out and accepted according to the LPS11 Acceptance Procedure (A-SP-LPS11-S-14). Follow configuration guidelines given in the LPA11-K Installation and Maintenance Manual (EK-LPA11-SM-001).

5.2 Set the Base Device Address of the LPS11 to 770400. Set the Vector Address to 340.

5.3 Set the Device Address, Vector Address, and Priority Level of the Basic LPA11-K according to Appendix A of this document.

5.4 Make sure that Switch 7 of E76 on the M8200-YC is set to the "OFF" position.

5.5 Make sure that Jumper W1 is installed on the M8254.

5.6 Make sure that all A/D Channel inputs are shorted to ground.

5.7 If the LPS11 has the LPSDRA Option, it must have the Digital I/O Test Cable (7009192) connected. This is optional in the field, but mandatory in the FA&T area.

5.8 If the LPS11 has the LPSVC Option, a scope must be connected to the scope control output on the rear of the LPS11 chassis. Refer to paragraph 14.0 of A-SP-LPS11-S-14 (LPS11 Acceptance Procedure) for selection of the proper scope and its installation. This is optional in the field, but mandatory in the FA&T area.

5.9 Load MAINDEC-11-DRLPA (LPA11-K System Test). Follow operating instructions contained in the writeup for this diagnostic. The address of locations "SR1:" and "SR2:" may be found in the Symbol Table at the back of the listing. Load location "SR1:" with the appropriate bits to inform the diagnostic that there is a LPS11 on the LPA11-K's I/O Bus, and to inform it as to which options are in the LPS11. Load location "SR2:" with the appropriate bits to inform the diagnostic as to how the LPS11 options are set up for test.

Allow MAINDEC-11-DRLPA to make at least six (6) non-erroring passes. If an error does occur, refer to the troubleshooting charts in Appendix B.

6.0 LPA11-K OPTION ACCEPTANCE

6.1 Perform the option test given in Section 3.0 of this document if the LPA11-K has "K" options on the I/O Bus.

6.2 Perform the option test given in Section 4.0 of this document if the LPA11-K has an AR11 on the I/O Bus.

6.3 Perform the option test given in Section 5.0 of this document if the LPA11-K has an LPS11 on the I/O Bus.

6.4 Configure DEC/X11 for the system that the LPA11-K is on. DEC/X11 for the LPA11-K must include MAINDEC-11-DXLPF, MAINDEC-11-DXLPG and MAINDEC-11-DXLPH. When running DECX/11 in the FA&T area, run MD-11-DXLPG and MD-11-DXLPH. They must be selected in that order. Do not select MD-11-DXLPF and MD-11-DXLPH if a problem seemed to exist with the system when the customer was using multiuser mode. MD-11-DXLPF and MD-11-DXLPG are both loaders that are used to load the microcode that is run by the MD-11-DXLPH exerciser. MD-11-DXLPF is the microcode loader for the multiuser mode. MD-11-DXLPG is the microcode loader for the dedicated mode. If all three LPA11-K DEC/X11 modules were selected, whichever of the two loaders was the last one selected, would be the one whose microcode would be exercised by MD-11-DXLPH.

6.4 cont

Patch locations "SR1:" and "SR2:" of MAINDEC-11-DRLPE according to the instructions contained in the writeup for this DEC/X11 module. Run DEC/X11 for a minimum of four (4) hours.

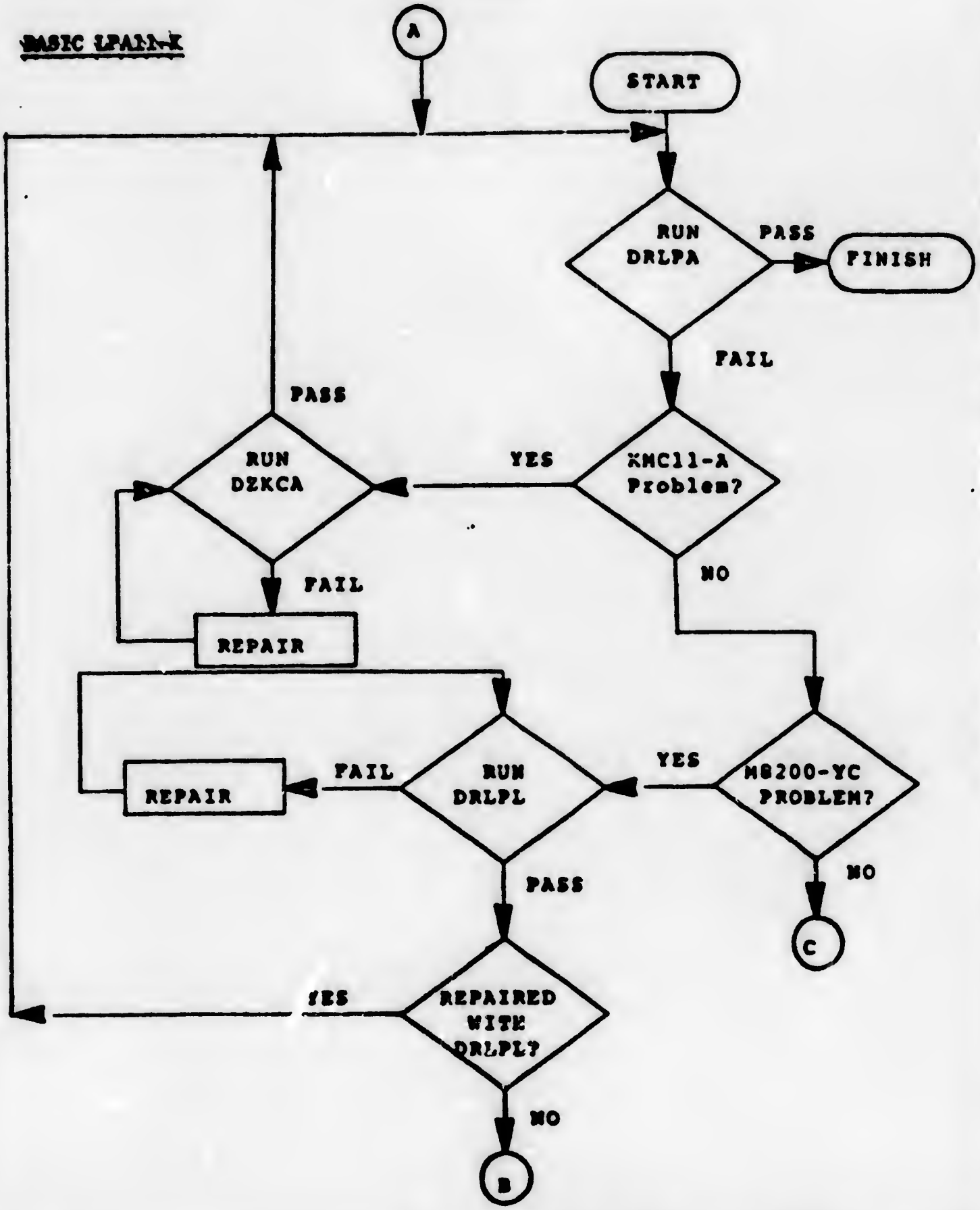
APPENDIX A

DEVICE	DEVICE ADDRESS	VECTOR ADDRESS	PRIORITY LEVEL
KMC11-A	770460	*300	5
M8200-YC	770470	420	5
AA11-K	770416	360	4
AD11-K #1	770400	340	6
AD11-K #2	770440	400	6
AR11	770400	340	Fixed
DR11-K #1	767770	310	4
DR11-K #2	767760	320	4
DR11-K #3	767750	330	4
DR11-K #4	767740	350	4
DR11-K #5	767730	370	4
KW11-K	770404	344	6
LPS11	770400	340	Fixed

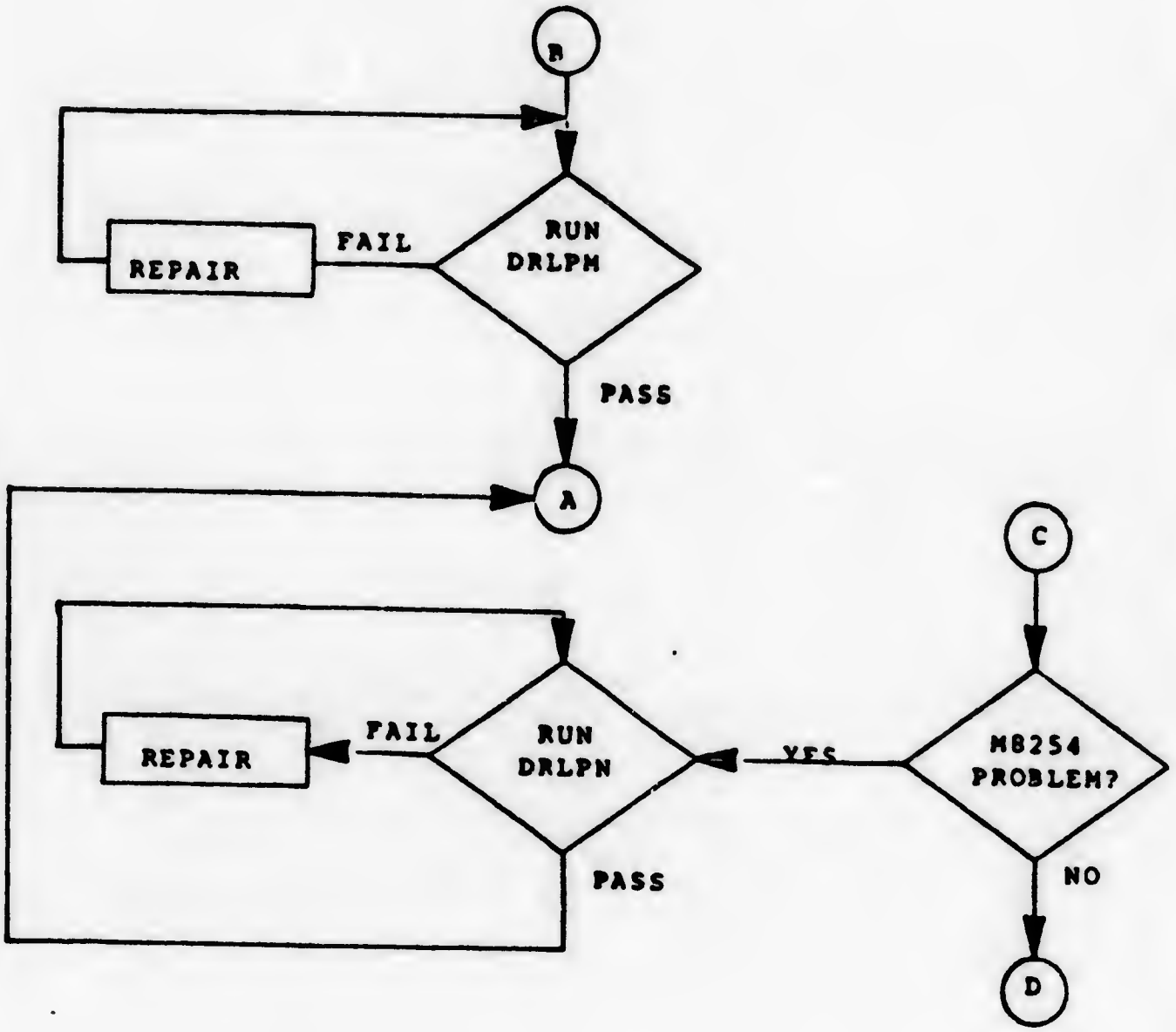
* Preferred Floating Vector Address

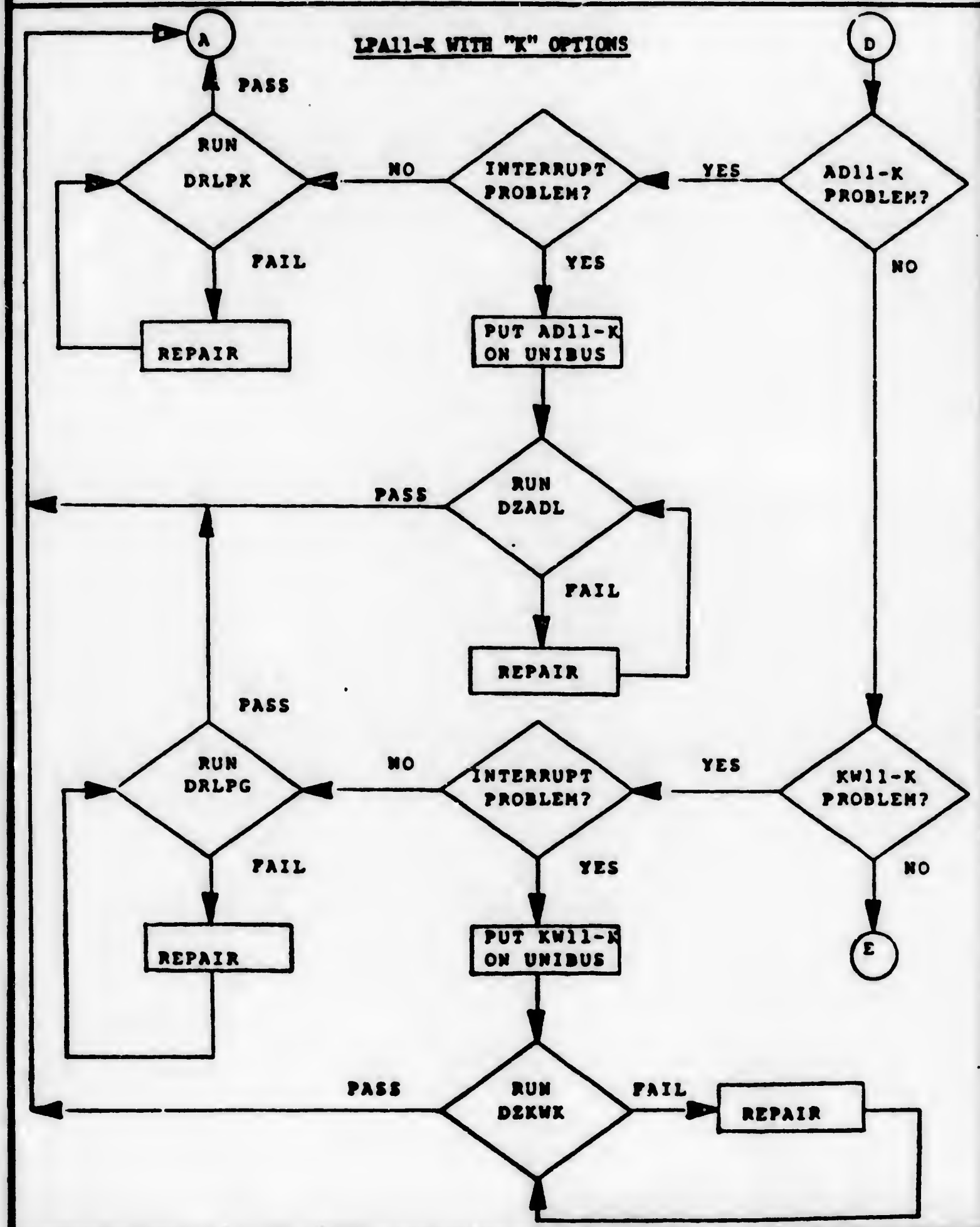
APPENDIX B

BASIC LPA11-K

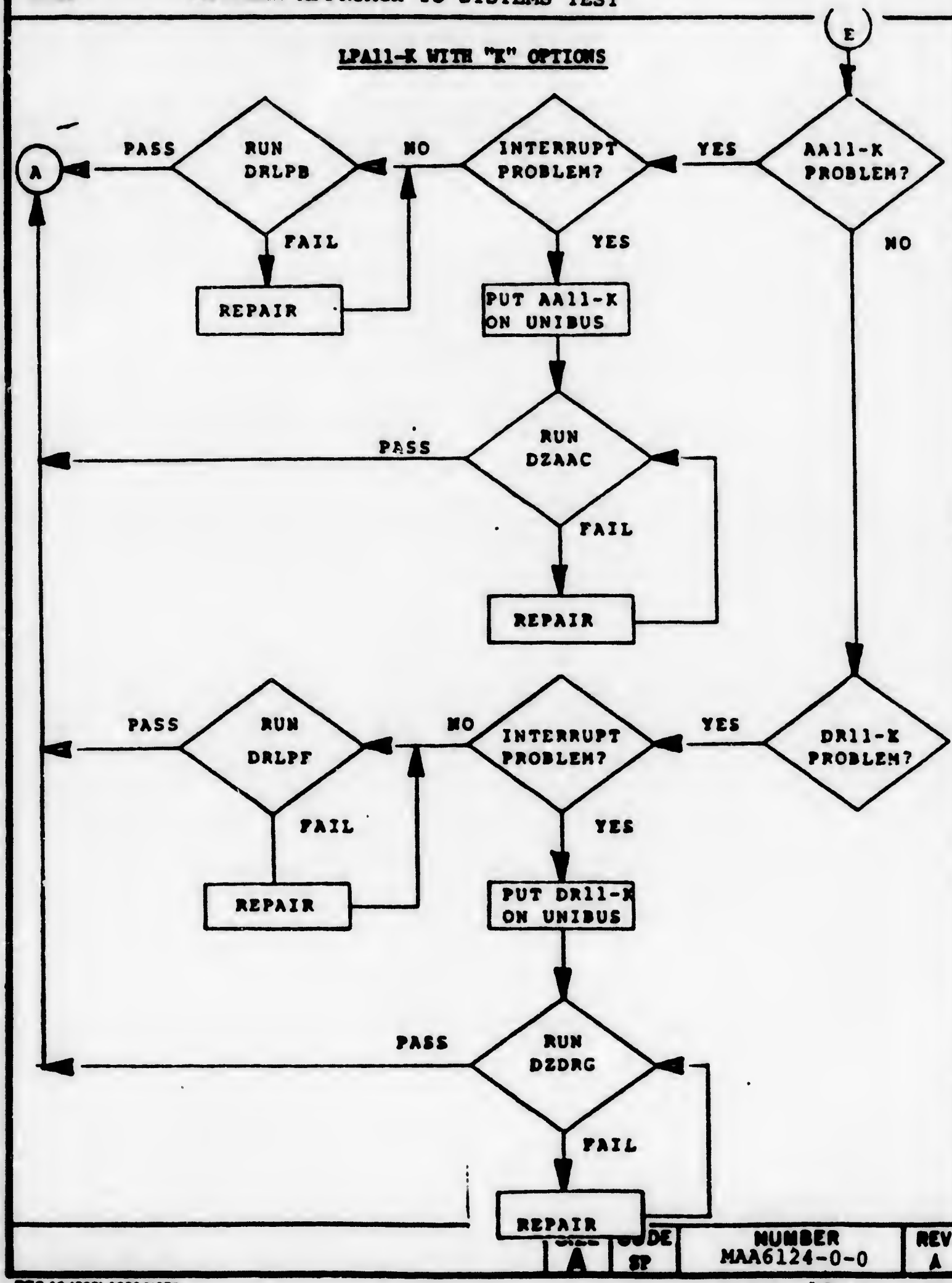


BASIC LPA11-K

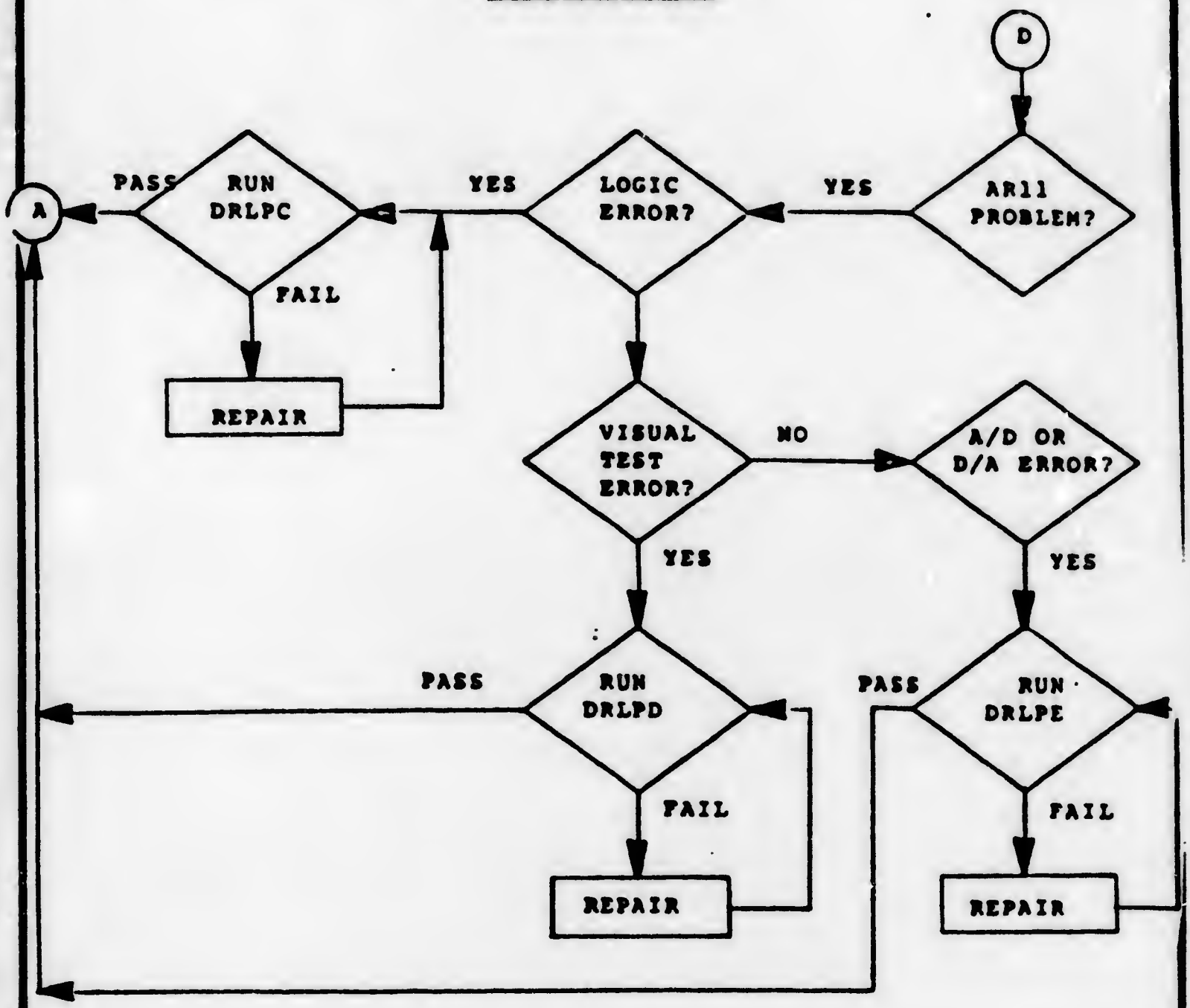



A
LPA11-K WITH "K" OPTIONS
D
PASS
RUN DRLPK
NO
INTERRUPT PROBLEM?
YES
AD11-K PROBLEM?
FAIL
YES
NO
REPAIR
PUT AD11-K ON UNIBUS
PASS
RUN DZADL
FAIL
REPAIR
PASS
RUN DRLPG
NO
INTERRUPT PROBLEM?
YES
KW11-K PROBLEM?
FAIL
YES
NO
REPAIR
PUT KW11-K ON UNIBUS
E
PASS
RUN DZKWK
FAIL
REPAIR

LPA11-K WITH "K" OPTIONS

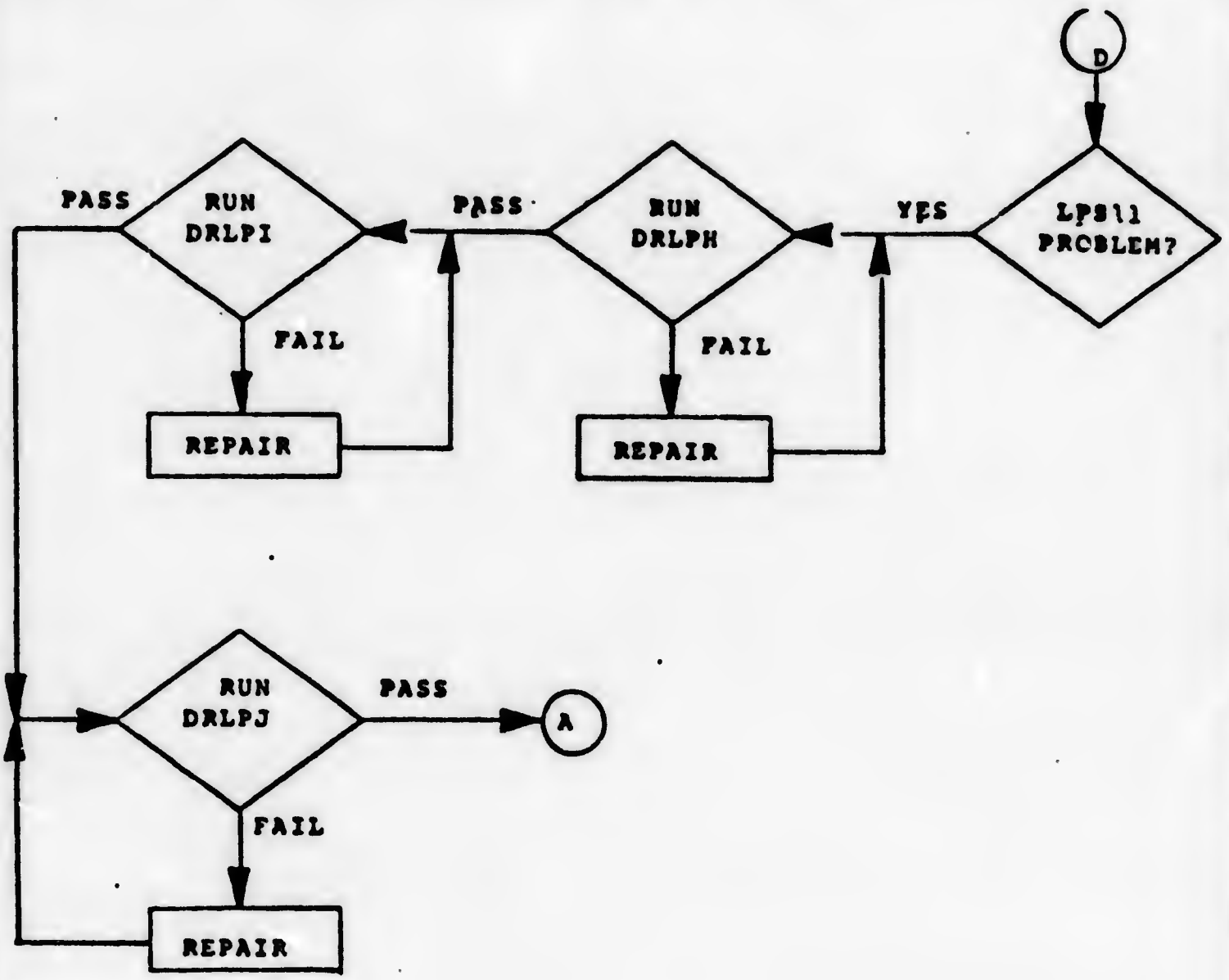


LPA11-K WITH AR11



- NOTE: If DRLPA reports an error and it cannot be found by running DRLPC, DRLPD or DRLPE; then you must connect the Unibus to the LPA11's I/O Bus. Remove the M8254 module and replace it with a G727 grant card. Run MD-11-DZARA, MD-11-DZARB and MD-11-DZARC to solve the problem. Make sure you do not exceed the Unibus Load Spec's.

TITLE MODULAR APPROACH TO SYSTEMS TEST



NOTE: If DRLPA reports an error, and it cannot be found by running MD-11-DRLPH, MD-11-DRLPI or MD-11-DRLPJ; then you must connect the Unibus to the LPA11-K's I/O Bus. Remove the M8254 module and replace it with a G727 grant card. Run MD-11-DZLPC, MD-11-DZLPD or MD-11-DZLPI to solve the problem. Make sure you do not exceed the Unibus Load Specs.

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MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AD11-K BACKUP REFERENCE DOCUMENTATION - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6125					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Sobieniewski		A	SP	MAA6125-0-0	A

AD11-K BACKUP REFERENCE DOCUMENTATION

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic write-up for the purpose of expediency. All instructions contained in this procedure are brief and direct for reasons of simplification, so not to confuse the operator when performing diagnostic testing. For more in-depth information, it will be necessary to refer to the diagnostic write-up.

2.0 REFERENCE DOCUMENTS

The documents listed below are for reference only.

2.1 Workmanship Manual

2.2 AD11-K User's Manual EK-AD11-K-OP-001

2.3 AD11-K Print Set B-TC-AD11-K-1

2.4 AD11-K Manufacturing and Field System Acceptance Procedure A-SP-AD11-K-5.

3.0 REQUIRED TEST EQUIPMENT

3.1 BG5036 Maintenance Kit (consists of a G5036 wrap-around module and a BC08R-1 cable).

3.2 Calibrated DC voltage source (EDC model MV116 or equivalent). Two are needed if a wrap-around module is not available.

3.3 PDP-11 CPU.

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC-11-DZADL AD11-K Diagnostic and Write-Up.

4.2 MAINDEC-11-DXADB DEC-X11 AD11-K Exerciser and Write-Up.

5.0 SPECIAL INSPECTION AND CHECKS

5.1 Assure the A/D converter package is securely fastened to the AAV0 module.

6.0 TEST SET-UP

6.1 Set up address and vector switches per AD11-K Mfg. and Field System Acceptance Procedure A-SP-AD11-K-5 section 2.2 - 2.3.

6.2 Install G5036 wrap-around test card per AD11-K Mfg. and Field System Acceptance Procedure A-SP-AD11-K-5 section 6.1 if wrap-around module is available. If the wrap-around module is not available, refer to AD11-K Mfg. and Field System Acceptance Procedure A-SP-AD11-K-5 section 6.2.

7.0 SYSTEM INTEGRATION TEST PROCEDURE

7.1 Load diagnostic into system under test using low or high speed tape reader, XXDP, or ACT-11.

7.2 Program Start-Up

7.2.1 Load Address 200

7.2.2 Start SR = 000000 (Standard Default Condition)

7.3 Switch Register Settings

7.3.1 SW15 = 1 or Up Halt on Error

7.3.2 SW14 = 1 or Up Loop on Test

7.3.3 SW13 = 1 or Up Inhibit Error Typeouts

7.3.4 SW12 = 1 or Up for VT55 Display

7.3.5 SW11 = 1 or Up Inhibit Iterations

7.3.6 SW10 = 1 or Up Bell on Error

7.3.7 SW9 = 1 or Up Loop on Error

7.3.8 SW8 = 1 or Up Loop on Test in SR <0:7>

7.4 Operator Action

After the diagnostic has been started, this statement is printed out: "Type the letter and carriage return of the desired test." The Auto Test (A) should be selected since it operates all diagnostic portions of the AD11-K test.

The operator should observe 2 non-erroring passes. Running the Auto test on the first pass should take 18 minutes, successive passes should take 36 minutes each.

7.5 Acceptable Errors

There are no acceptable errors.

7.6 Procedure ∮ Restart After Repair

7.6.1 Repeat steps 7.2 thru 7.5.

7.7 DEC-X11 With KW11-K Installed

7.7.1 Refer to AD11-K Mfg. and Field System Acceptance Procedure A-SP-AD11-K-5 Section 7 for interactive testing.

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MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AA11-K DIGITAL TO ANALOG CONVERTER - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6126					

ENG	APPD	SIZE	CODE	NUMBER	REV
Ron Jekanowski		A	SP	MAA6126-0-0	A

AA11-K DIGITAL TO ANALOG CONVERTER

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeup for the purpose of expediency. All instructions in this procedure are brief and direct for reasons of simplification, so not to confuse the operator when performing diagnostic testing. For more in-depth information, it will be necessary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

The documents listed below are for reference only.

2.1 Workmanship Manual

2.2 AA11-K user's Manual EK-AA11K-TM-001

2.3 AA11-K Print Set

2.4 AA11-K Manufacturing and Field System Acceptance Procedure A-SP-AA11-K-5

3.0 REQUIRED TEST EQUIPMENT

3.1 Calibrated DC Volt Meter

3.2 VR14 or VT01 Scope or Equivalent

3.3 Oscilloscope Tektronix 453 or Equivalent

3.4 PDP-11 CPU with 1 Quad SPC Slot

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC-11-DZAAC-A DIAGNOSTIC AND WRITEUP FOR AA11-K

4.2 MAINDEC-11-DXAAB-A AA11-K DEC-X-11 Exerciser and Writeup

5.0 SPECIAL INSPECTIONS AND CHECKS

NONE

6.0 TEST SETUP

6.1 Set up address and vector switches per AA11-K Mfg. and Field System Acceptance Procedure A-SP-AA11-K-5 Sections 3.4 - 3.6.

6.2 Connect scope cable to AA11-K berg connector J1 per AA11-K Mfg. and Field System Acceptance Procedure A-SP-AA11-K-5 Section 4.2.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 Load program through the appropriate load media.

7.2 Program starting address

7.2.1 Load address 200

7.2.2 Start 000000 (SR) standard switch settings

7.3 Alternate switch settings

7.3.1 SW15=1 Halt on Error

7.3.2 SW14=1 Loop on current test

7.3.3 SW13=1 Inhibit error typeout

7.3.4 SW12=1 Storage Scope connected

7.3.5 SW11=1 Inhibit test iterations

7.3.6 SW10=1 External delay connected

7.3.7 SW09=1 Two's compliment mode

7.3.8 SW08=1 Loop on test in SR 7:0

7.4 Operator Action

A message will be typed designating a 2 letter code for sub test selection. The auto logic test "AL" should be selected first to verify proper logic operation. Then "AD" should be typed to run the visual display portion.

NOTE: If scope display is not available, refer to the AA11-K Mfg. and Field Acceptance Procedure, A-SP-AA11-K-5 for alternative testing.

7.5 Evidence of End of Pass, or Estimated Run Time

7.5.1 Subtest "AL" takes approx. 30 sec.

7.5.2 Subtest "AD" takes approx. 60 sec.

7.5.3 Subtest "AL" is operator dependent.

7.5.4 Subtest "ML" is a non-ending loop.

7.5.5 Subtest "MD" is a non-ending loop.

7.6 Acceptable Errors

NONE

7.7 Procedure #Restart After Repair

7.7.1 Repeat steps 7.2 through 7.6.

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MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AM11-K MULTIPLEXER EXPANDER - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6127					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tony Sekniewski	Tom	A	SP	MAA6127-0-0	A

AM11-K MULTIPLEXER EXPANDER

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic write-up for the purpose of expediency. All instructions contained in this procedure are direct and brief for reasons of simplification, so as not to confuse the operator when performing the diagnostic testing. For more in-depth information, it will be necessary to refer to the diagnostic write-up.

2.0 REFERENCE DOCUMENTATION

The documents listed below are for reference only.

2.1 Workmanship Manual

2.2 AM11-K User's Manual EK-Am11K-TM-001

2.3 AM11-K Print Set

2.4 AM11-K Manufacturing and Field System Acceptance Procedure A-SP-AM11-K-5.

3.0 REQUIRED TEST EQUIPMENT

3.1 Oscilloscope Tektronix 453 or equivalent.

3.2 BG5036 Maintenance Kit (G5036 Wraparound Module and a BC08R-01 Cable)

3.3 Calibrated DC voltage source (EDC Model MV100 or equivalent).

3.4 BC08R-08 cable

3.5 AD11-K Analog Module

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC-11-DZADB-B AD11-K diagnostic used for checkout and debug of the AM11-K.

4.2 MAINDEC-11-DXADB-A AD11-K DEC-X-11 exerciser.

5.0 SPECIAL INSPECTIONS AND CHECKS

NONE

6.0 TEST SETUP

6.1 Connect a BC11-T cable from AD11-K J2 to AM11-K J1.

6.2 Connect the BC08R-08 cable from AD11-K J1 to AM11-K J3.

6.3 Connect G5036 test module to J2, J4 or J5 depending on which bank of channels on the AM11-K are to be tested; i.e., J2 - CH20 - 37, J4 - CH40-57, J5 - CH60-77.

NOTE: G5036 module connects to the AM11-K via a BC08R-01. This cable should be installed upside down, i.e., A-VV instead of A-A.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 Load program through the appropriate load media.

7.2 Program start address

7.2.1 Load address 200

7.2.2 Start 000000 (SR) standard switch settings

7.3 Alternate Switch Settings

7.3.1 SW15 = 1 Halt on error

7.3.2 SW14 = 1 Loop on test

7.3.3 SW13 = 1 Inhibit error typeouts

7.3.4 SW12 = 1 Halt for VT55 display

7.3.5 SW11 = 1 Inhibit iterations

7.3.6 SW10 = 1 Bell on error

7.3.7 SW09 = 1 Loop on error

7.3.8 SW08 = 1 Loop on test in SWR 7:0

7.4 Operator Action

A message is printed with a list of subtests that the user may select. For acceptance verification, the only test to be selected is test "A", the auto test. Before running the test, a 1 location patch is necessary to select one of three base addresses of the channels to be tested. Refer to Section 6.3 for channel selection. The location "base CH" should be patched for 20 (channels 20-37 to be tested), 40 (channels 40-57 to be tested) or 60 (channels 60-77 to be tested).

NOTE: If BG5036 wraparound test board is not available, refer to the AM11-K Mfg. & Field Acceptance Procedure A-SP-AM11-K-5 Section 7.2 for alternative testing.

7.5 Evidence of End Pass or Estimated Run Time

When running the auto test "END PASS" will be typed. Each pass of the auto test takes approximately 10 minutes.

7.6 Acceptable Errors

NONE

7.7 Procedure to Restart After Repair

Repeat steps 7.2 through 7.6.

NOTE: If analog section of the option is repaired, recalibration may be necessary. Refer to AM11-K calibration procedure for further instructions.

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE LSP-11 SYSTEM CHECKOUT & ACCEPTANCE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6130					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekerawski	Tom Sekerawski	A	SP	MAA6130-0-0	A

LPS-11 SYSTEM CHECKOUT & ACCEPTANCE

1.0 LPS-11 Setup and Calibration

Refer to Document DEC-11-HLPMA-B-D

1.1 LPS-11 Acceptance Procedure

Refer to Document A-SP-LPS11-S-14

1.2 Diagnostic Package

A) LPS-11 Test I MAINDEC-11-DZLPC
B) LPS-11 Test II MAINDEC-11-DZLPD
C) M7023 Digital I/O Test MAINDEC-11-DZLPI-A

Other Related Documents

LPS-11 System Users Guide DEC-11-HLPMA-B-D


A613

DIGITAL EQUIPMENT CORPORATION

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE 16 CHANNEL 12 BIT A/D FOR PDP-11/03 - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6135					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jeteniewski	Tom	A	SP	MAA6135-0-0	A

EN-01003-16-N672-(392)

16 CHANNEL 12 BIT A/D FOR PDP-11/03

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeup. For the purpose of expediency, the procedure has been kept brief, and to the point, to keep from confusing the user. For additional information, it will be necessary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD 116)

2.2 Engineering Specifications SP-ADV11-A-3

2.3 ADV11-A Print Set

2.4 EK-ADV11-OP-001 ADV11-A, KWV11-A, AAV11-A, DRV11 Users Manual

2.5 11L03 Manufacturing Specifications

3.0 REQUIRED TEST EQUIPMENT

3.1 LSI11 Standard Computer with 8K of memory

3.2 Test connecter 70-12894

3.3 Precision voltage source: Electronic Development Corp. (EDC) VS-11N or equivalent.

3.4 ADV11-A module

3.5 Output terminal/DLV11

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC 11 - DVADA ADV11-A Performance Test Diagnostic and writeup.

4.2 MAINDEC 11 - DXADC DEC/X11 Exerciser and writeup.

5.0 SPECIAL INSTRUCTIONS AND CHECKS

5.1 If an H322 distribution panel is present, then connect ADV11-A by means of a BC08R-06 cable from J1 of module to J10 of the H322 (all C and D variations of 11L03)

5.2 When an ADV11-A and a KWV11-A are both present in the system module, jumpers (DEC 7010771) are installed from the KW output tab (CLK) to the A/D clock overflow tab (C) and from the KW tab (ST1) to the A/D tab(s).

5.3 Two RF shields are provided with each ADV11-A. They are installed on each side of the module.

5.4 If the ADV11-A is hooked up to an H322, then SEL signal must be grounded on the H322 so that the A/D is shipped to the customer in single ended mode. To accomplish this, connect a wire between J8 top screw terminal (SE signal) to J7 top screw terminal (logic GRD) on the H322.

6.0 TEST SET UP

6.1 Insure switch packs S2 and S1 are set up for a device address of 17Ø4ØØ, and a vector of 400 respectively.

6.2 Install module in slots A thru DØ3 of CPU box C and D variations of 11LØ3.

6.3 Install test connecter 7Ø-12894 in Berg Connecter J1 of module.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 ADV11-A Performance Test (DVADA)

7.1.1 Load program through appropriate load media

7.1.2 Summary of available tests and character typed to execute.

Character Typed	Test
W	Wrap around test
C	Calibration test
P	Print values test
L	Logic tests
A	Wraparound and logic tests

* NOTE 1: Wraparound test requires Berg Test Connecter to run.

NOTE 2: Program will give instructions on calibrating upon typing C.

7.1.3 Program starting addresses

7.1.3.1 200 - For normal test
7.1.3.2 204 - Restart
7.1.3.3 210 - Option area burn-in

7.1.4 Alternate Software SR settings (176)

7.1.4.1 SWR15 = 1 Halt on error
7.1.4.2 SWR14 = 1 Loop on test
7.1.4.3 SWR13 = 1 Inhibit error typeouts
7.1.4.4 SWR12 = 1 Halt for VT55 Display
7.1.4.5 SWR11 = 1 Inhibit iterations
7.1.4.6 SWR10 = 1 Bell on error
7.1.4.7 SWR 9 = 1 Loop on error
7.1.4.8 SWR 8 = 1 Loop on test in SWR <7:0>

7.1.5 Operator Action

7.1.5.1 Set SWR bits as desired.
7.1.5.2 Type 200G
7.1.5.3 Type character to run desired test.

7.1.6 Evidence of End of Pass

At end of pass, the following typeout will occur:

"END PASS GOOD UNITS $$$$$$$$$$$$$11"
This indicates that units 1 and 2 have run without failure.

7.1.7 Execution time for each test is:

Calibration:	5 conversions/min. @110 baud
Print Valves:	8 conversions/8 seconds @ 110 baud
Wraparound:	7 minutes first pass;32 minutes for successive passes
Logic:	1 minute
Auto:	8 minutes first pass; 33 minutes for successive passes

7.1.8 Acceptable Errors: None

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MANUFACTURING SPECIFICATION

DATE 5/7/81

TITLE M.A.S.T. IB11

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	New Release	ML013		6/2/81		6/2/81

ENG	APPD	SIZE	CODE	NUMBER	REV
Art Richard	Bob Beck	A	SP	MA-A6154-0-0	A

IB11

1.0 INTRODUCTION:

1.1 The IB11 option is a hardware/software package that allows test and measurement instruments that are IEEE bus compatible to be interfaced with the PDP-11 Unibus. The IB11 consist of a DW11 Unibus to Q-bus Interface, DDV11 Backplane, and IBV11 IEEE Instrument Bus Interface.

2.0 REFERENCE DOCUMENTATION:

2.1 Manuals & Engineering Specification:

2.1.1	IB11 Unibus to IEEE Instrument Bus Interface Installation Manual	EK-IB11A-IN
2.1.2	DW11 Unibus to LSI-11 Bus Installation Manual	EP-DW11A-IN
2.1.3	IBV11-A LSI-11 Bus to Instrument Bus Interface User's Manual	EP-IBV11-UG

2.2 Prints and Schematics:

2.2.1	IB11 Field Maint. Print Set	MP00620
2.2.2	DW11 Unibus to Q-bus Print Set	MP00459
2.2.3	IBV11-A LSI/IB Interface Print Set	MP00274

3.0 REQUIRED TEST EQUIPMENT:

3.1 PDP-11 with 16K words of memory.

3.2 Console terminal such as an LA36, LA120 or equivalent.

3.3 Appropriate load media.

3.4 Digital Volt Meter (DVM), accurate to .1V @ 15 volts.

4.0 REQUIRED DIAGNOSTIC PROGRAMS:

4.1 CVIBB?? IBV11-A Diagnostic

5.0 SPECIAL INSTRUCTIONS:

5.1 When installing the M8217 module into an available Unibus backplane SPC slot, the NPG in/NPG out jumper CA1 to CB1 must be removed.

6.0 INSTALLATION & TEST SET-UP INSTRUCTIONS:

6.1 Visual Inspection:

6.1.1 Check for any structural damage to modules such as broken components, cut etches, etc.

6.2 Module Switch Configuration:

6.2.1 The first M7954 module switches are configured as follows:

Reference Figures 1, 2, and 3.

For Bus address 160150:

S2 - switches 7, 8, & 10 on.
switches 1, 2, 3, 4, 5, 6, & 9 off.

For vector address 420:

S1 - switches 1, 5, & 8 on.
switches 2, 3, 4, 6, & 7 off.

6.2.2 Other M7954 modules to be added to the system will use floating address and vector assignments.

6.3 Module Cabling:

6.3.1 Two BC05L-06 cables connect from the M8217 to the M9401 module. See Figure 4. The red stripe on the cables must be adjacent to connectors pins VV/UU on both modules.

6.4 Module Placement:

Refer to Figures 5 and 6.

6.4.1 The M8217 is placed in a available Unibus backplane SPC slot.

6.4.2 The M9401 module is placed in slot A/B01 of the DDV11-C LSI-11 Bus backplane.

6.4.3 The M7954 Instrument Bus module is normaly placed into slot C/D01 of the DDV11-C LSI-11 Bus backplane. If more M7954 modules are to be added, install into slots noting device priority. See Figure 6.

6.4.4 The M9400-YB Terminator module is placed into the slot just after the last M7954. Normaly C/D02 of the DDV11-C.

7.0 POWER CHECKS:

The following voltage should be present on the respective backplane pins:

VOLTAGE	TOLERANCE	BACKPLANE LOC.
+5 V.D.C.	4.75V to 5.25V	AA2, BA2, or CA2

8.0 DIAGNOSTIC TEST PROCEDURE:

Note: For the specific sequence of diagnostics to be run in any particular situation, and for current MAST minimum test criteria (e.g. pass-counts, etc.), refer to the appropriate MAST CHECKLIST. The following is a list of step-by-step instructions for executing each individual diagnostic contained in the CHECKLIST.

8.1 CVIBB?? IBV11-A Diagnostic

8.1.1 Starting instructions:

Starting address is 200.

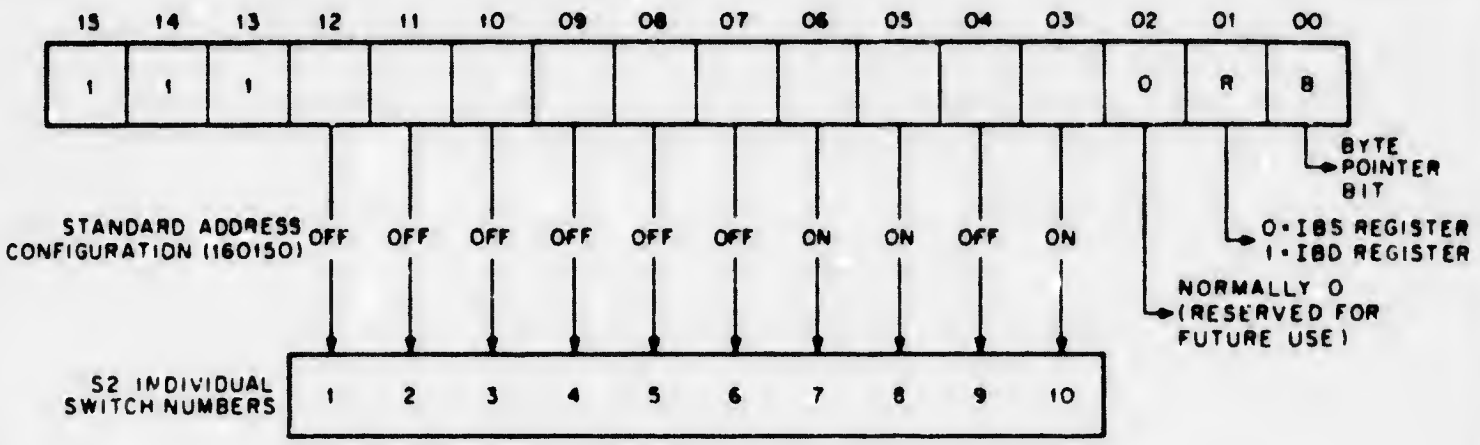
CVIBBA IBV11A DIAGNOSTIC

SWR = 000000 NEW = <CR>

END PASS# 1

END PASS# 2

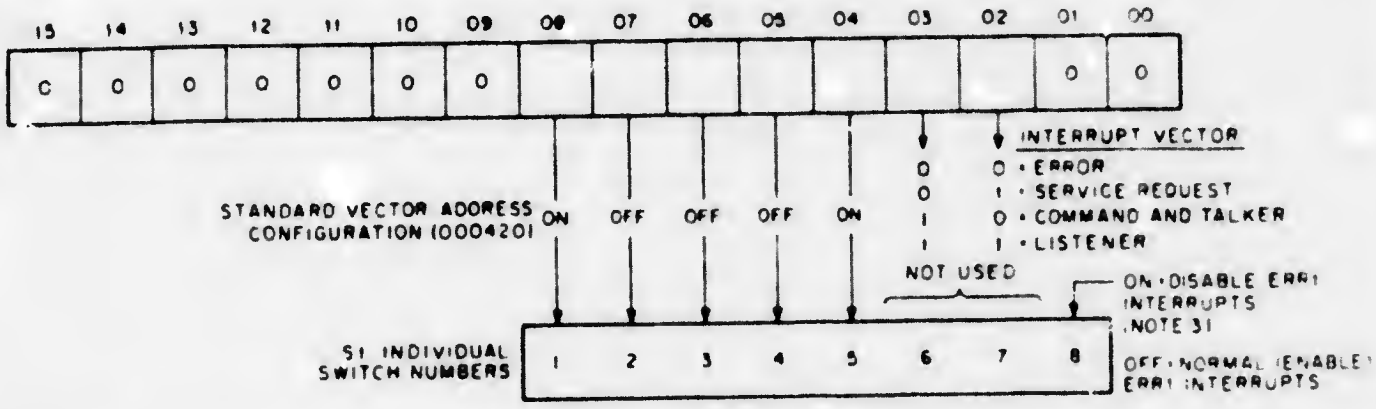
8.1.2 No errors are allowed.



NOTES:

1. OFF • Logical 0; ON • Logical 1
2. Only the IBS REGISTER ADDRESS is configured via S2. The IBD REGISTER ADDRESS always equals the IBS REGISTER ADDRESS +2.

Figure 1 M7954 Device Address Selection



NOTES:

1. OFF • Logical 0, ON • Logical 1
2. Only the VECTOR ADDRESS bits (8,4) are configured via S1. Bits 3 and 2 are IBV11-A hardware-selected for the functions shown.
3. S1-8 OFF • IBV11 is the only system controller connected to the instrument bus.
   S1-8 ON • Another system controller is connected to the instrument bus.

Figure 2 M7954 Interrupt Vector Address Selection

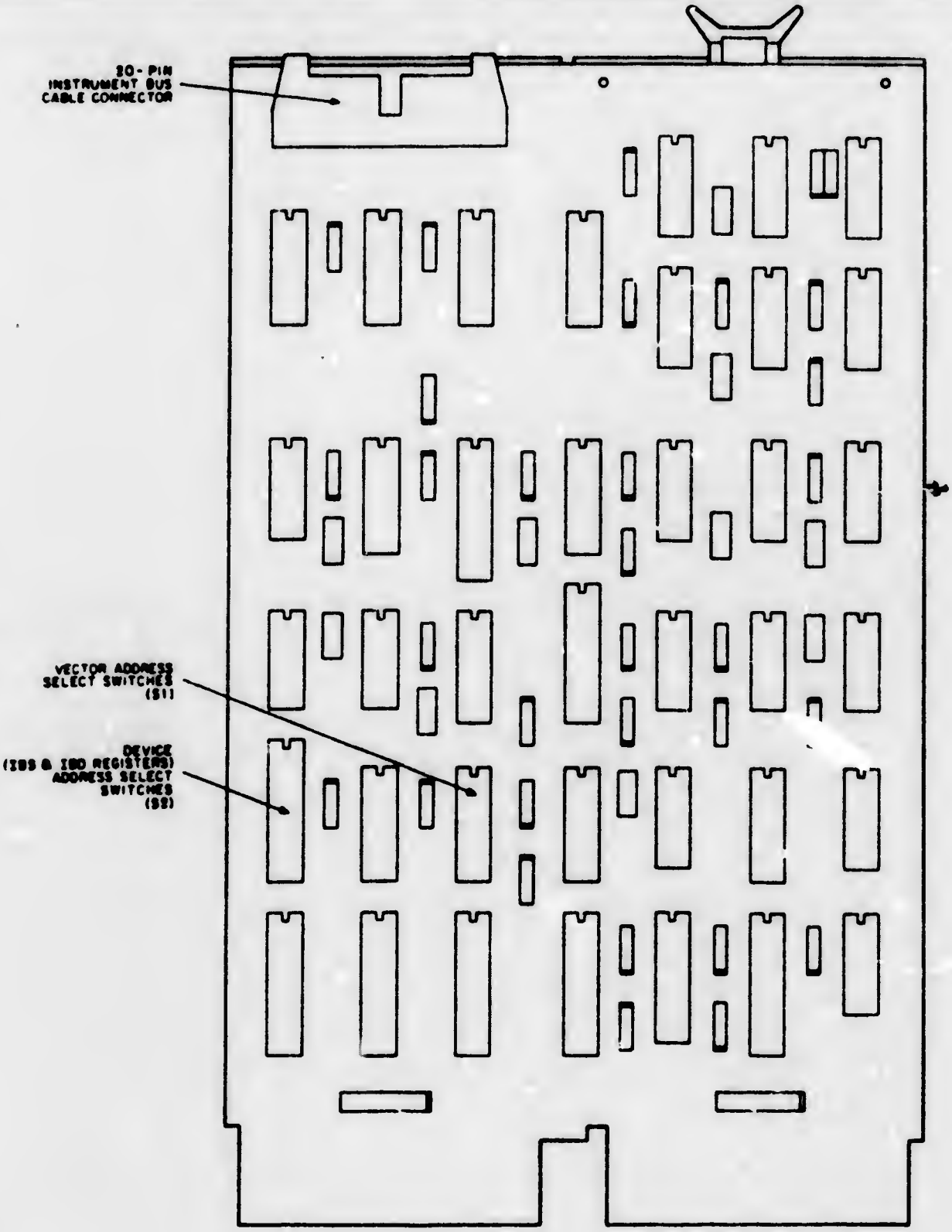
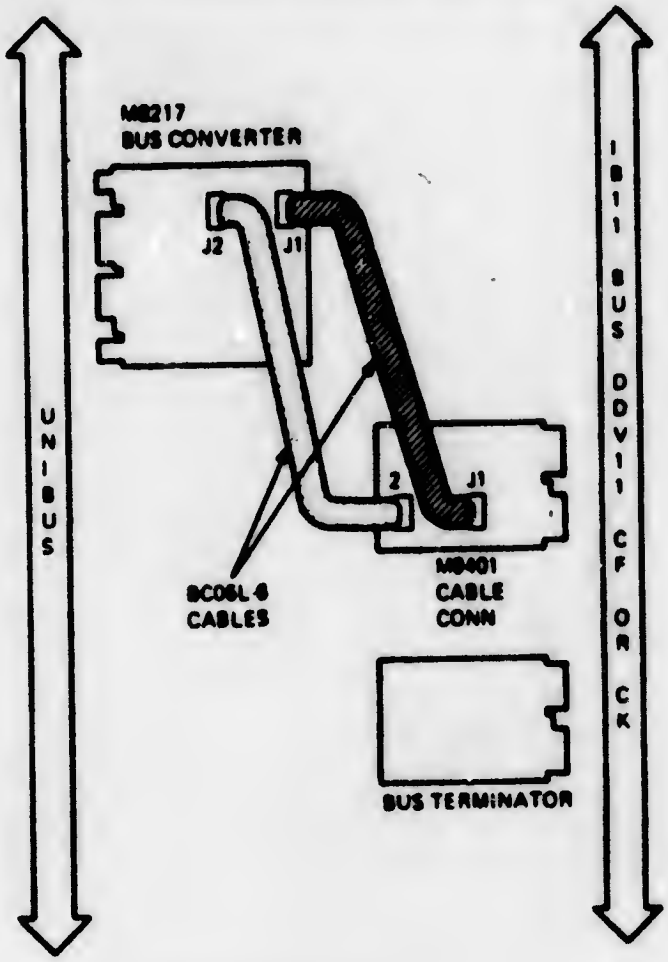


Figure 3 M7954 Module Switch Locations



IB11 Interconnecting Diagram

Figure 4

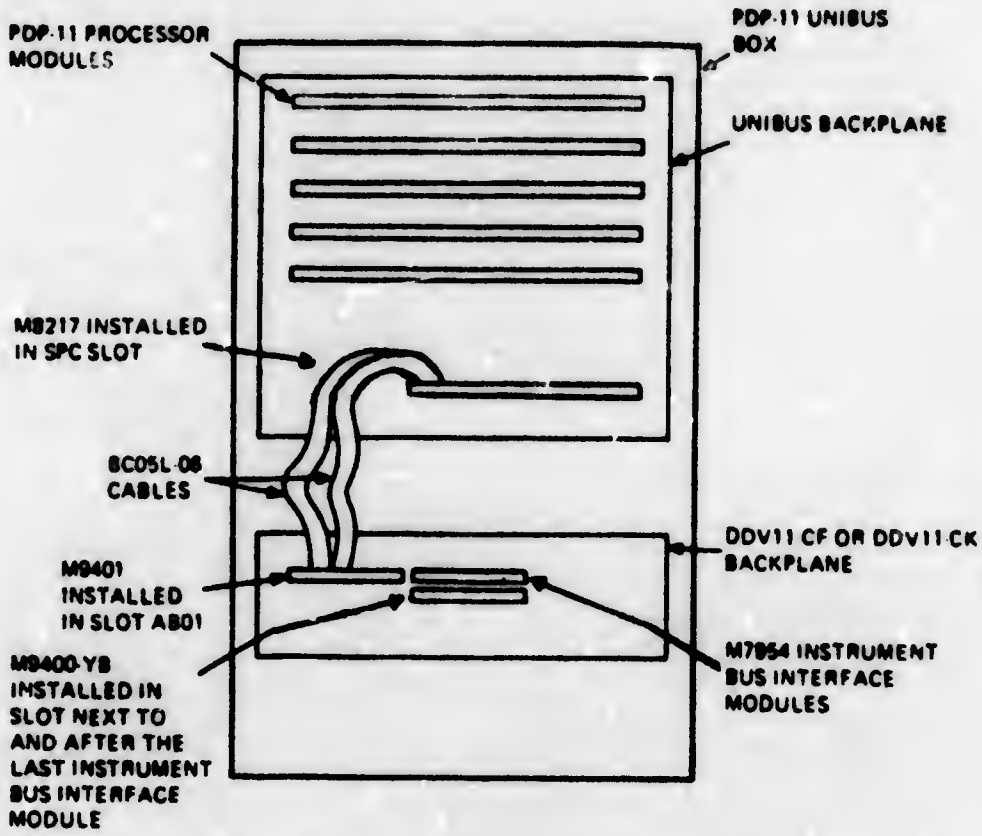


Figure 5 IB11 Option in a PDP-11 Processor Box

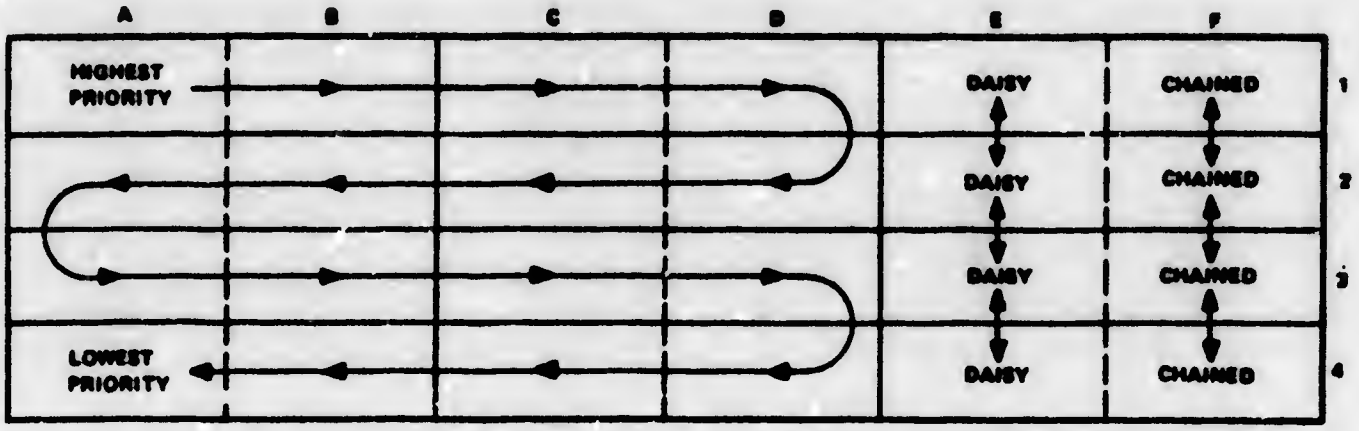


Figure 6 DDV11-C Backplane Priority Assignments

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE ICS-11 INDUSTRIAL SUB-SYSTEM PROCEDURE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	Prev. 7668001-0-6160					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekerinski		A	SP	MAA6160-0-0	C

ICS-11 INDUSTRIAL SUB-SYSTEM PROCEDURE

1.0 SPECIAL INSTRUCTIONS

1.1 No slots may be empty between A005 and A007 modules.

1.2 W7440 modules must never be installed in ICS file slot #9.

1.3 A907 must be installed between A005/A007 and the M8030/ M8050 module (s), when the latter is located within four (4) slots of the A005/A007 module (s).

1.4 ICS-J continuity Jumper Card must be installed in the "F" connector block of all open slots between the first and last interrupting module of a file.

1.5 Mercury wetted relay modules (A005, A007, M8030, M8050) must reside in a vertical plane for a period of at least one (1) minute, to prevent module damage resulting from a shorted relay.

1.6 Interrupting modules closest t. the control module has highest priority within the file, and that file closest to the processor has highest priority within the ICS11.

1.7 Options IAC-IA, IAC-IB, IAC-OA, and IAC-OB shall be system tested as IDC-ID, IDC-IE, IDC-OA, and IDC-OB respectively.

Modules used in these configurations must have jumper W1 installed, only after completion of all system testing.

1.8 The A005-YA is a computer Special System's variant, that shall require program modifications to the in-house AUTOCAT diagnostic.

1.8.1 Reference Table 5 for diagnostic changes.

1.8.2 Reference A-SP-A005-0-8, Section 7, for A005-YA explanation.

1.8.3 Field Service shall reference Table 6 for calibration test parameters when using the ICS Field Test Program.

1.8.4 FA&T shall reference the ICS Field Test Program when performing re-calibration of the A005-YA.

2.0 REFERENCE DOCUMENTS

Manuals	EK-ICS11-MM
Checkout Procedures	A-SP-A6330-0-5 A-SP-7010596
Acceptance Procedures	A-SP-A6330-0-5 A-SP-7010596
F.S. Acceptance	A-SP-ICS11-M-5
Module Test Procedures	A-SP-7010327-0-1 A-SP-7011020-0-1 A-SP-14/30-0-5 A-SP-ICS11-M-6
Engineering Specifications	A-SP-H1601-0 A-SP-M6850-0 A-SP-M6870-0-8 A-SP-M8030-0-8 A-SP-M8050-0-8 A-SP-W7410-0-8 A-SP-W7411-0-8 A-SP-W7430-0-8 A-SP-W7431-0-8 A-SP-W7440-0-8 A-SP-ICS11-M-4 A-SP-A005-0-8 A-SP-A007-0-8 A-SP-A907-0-8 A-SP-6330-0-8 A-SP-H1501-0-1 A-SP-ICS11-M-6
Prints	B-DD-ICS11-M B-DD-H912-0 B-DD-IDA-0 B-DD-ICJ-I B-DD-ISH-I B-DD-IDC-0 B-DD-IDC-I B-DD-IAD-I B-DD-IMX-I B-DD-IRL-0 B-DD-7010596-0 B-DD-7010327-0

MainDec Listings

AUTOCAT-11-QZICA (FA&T only)
AUTOCAT-11-QZICB (Module Test only)
AUTOCAT-11-QZICC (Module Test only)
MD-11-DZICA (Field Serv. only)

3.0 REFERENCE TEST EQUIPMENT

3.1 7010596 System Tester (in-house).

3.2 Oscilloscope, tektronic 465 or equivalent.

3.3 A6330, DAC Tester.

3.4 "11" family processor, with 8K memory.

4.0 SPECIAL INSPECTION/CHECK

4.1 Ensure system components agree with ICS line items on the Customer Requisition form.

4.2 Ensure an electromagnetic shield is present between the M8090 and the first I/O module for each ICS File Box.

4.3 Verify each ICS File Box module (s) are installed according to the approved priority sequence table. See Table 1.

4.4 Verify File Box (s) are securely grounded to the mounting cabinet and that the latter is secured system power ground. (use ohm meter)

5.0 CONFIGURATION GUIDELINES

5.1 All ICS option modules are to be installed using the slot-priority sequence table. See Table 1.

5.2 H912 mounting terminals must not be installed in cabinets containing sensitive equipment, such as disks or tapes.

6.0 TEST SET-UP

Refer to test procedures A-SP-7010596-0-0 and A-SP-A6330-0-5.

Module Configuration; see Table 1 through 4.

7.0 SYSTEM INTEGRATION TEST PROCEDURE

7.1 Power up both the system tester and the system under test. Also, if the IDA-0A option tester is to be used at this time, it should also be turned on. Allow 30 minutes for this system and test gear to stabilize.

7.2 ICS11 Systems Test Program

NOTE: This diagnostic requires the use of a ICS system tester.

7.2.1 Load the ICS systems test program diagnostic AUTO-CAT-11-QZIRA using standard Digital Loading Procedures.

7.2.2 Set switch register to 200, load and start.

7.2.3 Enter the octal number of the file to be tested.

7.2.4 Enter the vector address of the same file. Addre: range 234-777.

7.2.5 Enter (self (cr)). This will automatically run a self test of the system tester to verify that all internal workings of the tester are operative. Should errors be encountered during this run, repairs should be instituted before proceding.

NOTE: System tester cables should be disconnected from the following option modules before attempting to run "self test". If not, false interrupts may be generated by the customer's file. IDC-IB, IDC-IC, IDC-IE and IAD-IA.

7.2.6 Enter (Z (cr)) to clear any previous job buffer entry.

7.2.7 Enter the I/O options mounted within the ICS file to be tested. This file may be 1 or 12 possible files on the system.

7.2.7.1 Should the file configuration include IDA-0A options, (A6330) do not enter them at this time.

NOTE: It is not necessary to remove this option while testing all other options, but do disconnect the DC input from the IDA-0A option tester. (ref. A-SP-A6330-0-0 option test procedure).

SAMPLE ENTRY

#EA005 (CR) - Enter one A005 in slot address 00 to real address 171000. Module connected to system testers analog cable.

#EA007,4 (CR) - Enter four A007's in slot addresses 02,04, 06 and 10 real addresses 171002 to 171010 modules connected to system testers analog cables.

#EW7411,5 (CR) Enter five W7411's in real addresses 171012 to 171023,modules connected to system tester DC cables 0-4

#S-30 (CR) Set slot address equal to 30. NOTE: We are not running A6330's at this time, so slot addresses 24 and 26 have been bypassed.

#EM6850,4 (CR) Enter four M6850's in slot address 30 thru 36. Real addresses 171030 thru 171036.

This completes the loading of the program job buffer to run all modules with the exception of both A6330's.

7.2.8 Type in (L (CR)) to obtain the module entry loaded into the program. This should be checked against your entry to verify that all entries were made correctly.

7.2.9 After entering the modules into the job buffer, type in (K (CR)). The program will respond with K ON. This will enable the program to run non stop.

7.2.10 Type in (R (CR)). This will initiate the test on the file box. NOTE: Should the program be halted during pass 2, it should not be restarted for 30 minutes, if IAD-IA options are within the filebox configuration. This is to allow for stabilization of flying caps mounted on this module.

7.2.11 Run the diagnostic for a minimum of (1) time specified, or (1) complete pass. Whichever is longer.

7.2.11.1 The current pass count can be obtained by typing "p" on the teletype. NOTE: If the ICS file has a maximum load of (16) analog modules (worst case diagnostic run time) a complete pass will take approximately 1½ hours.

7.2.11.2 Connect all I/O cables from the ICS to the H009 MTG panel (after tests have been run successfully in Acceptance), and have QC inspect the installation.

7.3 ICS11 Field Test Program

NOTE: This diagnostic requires the use of a field UDC/ICS tester.

7.3.1 Ref. Specification A-SP-ICS11-M-5 for indepth explanation.

7.4 ICS-11 Systems Test Program In Conjunction with A6330 DAC Tester.

7.4.1 Disconnect all I/O system tester cables from the files that were previously tested.

7.4.2 Five A6330's can be connected to the option tester at this time, but they will have to be scoped independantly of one another.

7.4.3 Enter (Z CR) on the teletype to clear all previously entered jobs.

7.4.4 Enter (K CR) on the teletype to check what state the "K" command is in. The K command for this test should be in the off mode.

7.4.5 Enter the slot address location for all the IDA-OA options within the file.
NOTE: only (5) five IDA-OA options can be connected to the tester. If others are present, they can be tested upon the completion of this test.

Example of loading technique to be used for IDA-OA options:

S - 24 cr Set slot address equal to 24
E A6330, 2 <cr> Enter A6330's in slot addresses 24 and 26 real addresses 171024 and 171026, Jobs 0 and 1 respectively.

7.4.6 Adjust all settings for the scope, and switch the option tester to the first option (card/cable output) Job 0. (reference A6330 option test procedure A-SP-A6330-0-5.)

7.4.7 Type in RJO<cr>. This will initiate pass 1 testing on the first IDA-OA option or Job 0 at slot address 171024. (see step 7.4.5) ramps will be outputed to the option for scope measurements.

7.0 SYSTEM INTEGRATION TEST PROCEDURE CONT.

7.4.8 Compare the scope waveform against the tolerences indicated within the option test procedure A-SP-A6330-0-5. If the option is found to be within tolerence, proceed to the next step. If not,repair adjust, or replace the option, and retest until acceptable.

7.4.8.1 To adjust the A6330, or IDA-0A Option, proceed as follows: (Ref. Figure 1)

A. First measure the cards reference voltage between "TP2" and "IPG". It should be +2 volts ± 2mv. If out of spec, use the "+2 v adj." pot to adjust it within tolerence.

B. Set the thumbwheel switch to the card under test.

C. Set the thumbwheel switch to channel 0 or the first voltege output.

D. Adjust the pot "D/A 0" gain adjust for channel 0. The output on the scope should be adjusted within the ± 20mv tolerence.

E. Set the thumbwheel switch to channel 2 or the second voltage output.

F. Repeat step D, but use pot marked "D/A 1" gain adjust.

G. Repeat steps C thru F for remaining two voltage channels 2 and 3 (thumbwheel settings 4 and 6 respectively).

H. Reset thumbwheel switch to channel 1. This is the first current output channel.

I. Adjust the current offset of channel 1 as close as possible to ground by using pot. "off 0".

7.0 SYSTEM INTEGRATION TEST PROCEDURE CONT.

J. Adjust the current gain of channel 1 to fall within the required ± 20 mv tolerance.

K. Reset the thumbwheel switch to channel 3 or the second current output.

L. Repeat steps I thru J and repeat these steps for the remaining current outputs channels 5 and 7.

7.4.9 Type "Control C" to terminate the test.

7.4.10 If other IDA-0A options have been entered, type in the next job to be run. Repeat steps 7.4.7 thru 7.4.9 until all jobs have been tested.

7.4.11 Turn "K" command on by typing "K" on the terminal.

7.4.12 Enter R <cr> and run all IDA-CA options entered in step 6.4.5 for (1) hour. With the "K" command on, pass 2 will only be run during this test. It is not necessary to scope the outputs for this test.

7.4.13 Type "Control C" to terminate the test.

7.4.14 Repeat steps 7.4.6 thru 7.4.10. Should any of the options fail, repair and repeat all tests.

7.4.15 If there are more than (5) five IDA-0A options within this file, it will be necessary to repeat steps 7.4.5 thru 7.4.14 to test the remaining.

7.5 Repeat all tests 7.0 thru 7.4.15 for all other files on the systems configuration.

TABLE 1

FILE BOX - MODULE PRIORITY TABLE

PRIORITY SEQUENCE	MODULE	OPTION	COMMENTS
1	A005	IAD-IA	
2	A007	IMX-IA	7 MAX
3	A005	IAD-IA	
4	A007	IMX-IA	7 MAX
5	A907	ISH-IA	
6	W7410	IDC-IA	
7	W7411	IAC-IA	H912, + BC40J
8	W7411	IDC-ID	
9	W7440	IDC-IC	
10	W7430	IDC-IB	
11	W7431	IAC-IB	H912, + BC40J
12	W7431	IDC-IE	
13	A6330	IDA-OA	12 MAX
14	M6870	IDC-OB	
15	M6870	IAC-OB	H912, + BC40J
16	M6850	IDC-OA	
17	M6850	IAC-OA	H912, +BC40J
18	M8030	IRL-OA	
19	M8050	IRL-OB	

TABLE 2

A005 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W108	OUT	INTERRUPT MODE
W111	IN	ICS-11

A007 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W21	OUT	SELECT MUX # 1
W22	OUT	SELECT MUX # 2
W23	OUT	SELECT MUX # 3
W24	OUT	SELECT MUX # 4
W25	OUT	SELECT MUX # 5
W26	OUT	SELECT MUX # 6
W27	OUT	SELECT MUX # 7

W7430 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W58	IN	INTERRUPT MODE
W59	OUT	ICS-11

W7431 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W 9	OUT	INTERRUPT MODE
W10	IN	ICS-11

TABLE 3

W7440 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W 2 W16	IN OUT	ICS-11 INTERRUPT MODE

M8090 STANDARD JUMPER CONFIGURATION

File No.	ICSR/ICAR JUMPERS									
	A12 W22	A11 W21	A10 W20	A9 W19	A8 W18	A7 W17	A6 W16	A5 W15	A4 W14	A3 W13
00	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT
01	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	IN
02	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	IN	OUT
03	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	IN	IN
04	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	OUT	OUT
05	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	OUT	IN
06	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	IN	OUT
07	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	IN	IN
08	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	OUT	OUT
09	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	OUT	IN
10	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	IN	OUT
11	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	IN	IN

Jumper OUT = Logic "1"
Jumper IN = Logic "0"

TABLE 4

M8090 STANDARD JUMPER CONFIGURATION

FILE JUMPERS

AD7 W12	AD6 W11	AD5 W10	AD4 W 9
IN	IN	IN	IN
IN	IN	IN	OUT
IN	IN	OUT	IN
IN	IN	OUT	OUT
IN	OUT	IN	IN
IN	OUT	IN	OUT
IN	OUT	OUT	IN
IN	OUT	OUT	OUT
OUT	IN	IN	IN
OUT	IN	IN	OUT
OUT	IN	OUT	IN
OUT	IN	OUT	OUT

Jumper OUT = Logical "1"
Jumper IN = Logical "0"

M8090 STANDARD JUMPER CONFIGURATION

File No.	Vector Address	VECTOR ADDRESS JUMPERS D8 W7	D7 W6	D6 W5	D5 W4	D4 W3	D3 W2	D2 W1
00*	234	IN	OUT	IN	IN	OUT	OUT	OUT
01**	300	IN	OUT	OUT	IN	IN	IN	IN
02	304	IN	OUT	OUT	IN	IN	IN	OUT
03	310	IN	OUT	OUT	IN	IN	OUT	IN
04	314	IN	OUT	OUT	IN	IN	OUT	OUT
05	320	IN	OUT	OUT	IN	OUT	IN	IN
06	324	IN	OUT	OUT	IN	OUT	IN,	OUT
07	330	IN	OUT	OUT	IN	OUT	OUT	IN
08	334	IN	OUT	OUT	IN	OUT	OUT	OUT
09	340	IN	OUT	OUT	OUT	IN	IN	IN
10	344	IN	OUT	OUT	OUT	IN,	IN	OUT
11	350	IN	OUT	OUT	OUT	IN	OUT	IN

Jumper OUT = Logic "1" Jumper IN = Logic "0"

TABLE 5

AUTOCAT DIAGNOSTIC "PATCHES"

ADDRESS TO BE CHANGED		
ICS11 AUTOCAT-11-QZICA	ICR11 AUTOCAT-11-QZICA	NEW CONTENTS
033210	033722	100020
033230	033312	100420
033250	033332	100066
033270	033352	100100
033310	033372	100500
033330	033412	100466
033346	033430	100000
033350	033432	101001
033370	033452	101004
033410	033472	101066
033530	033612	101466
033550	033632	101404
033566	033650	100000
033570	033652	101401

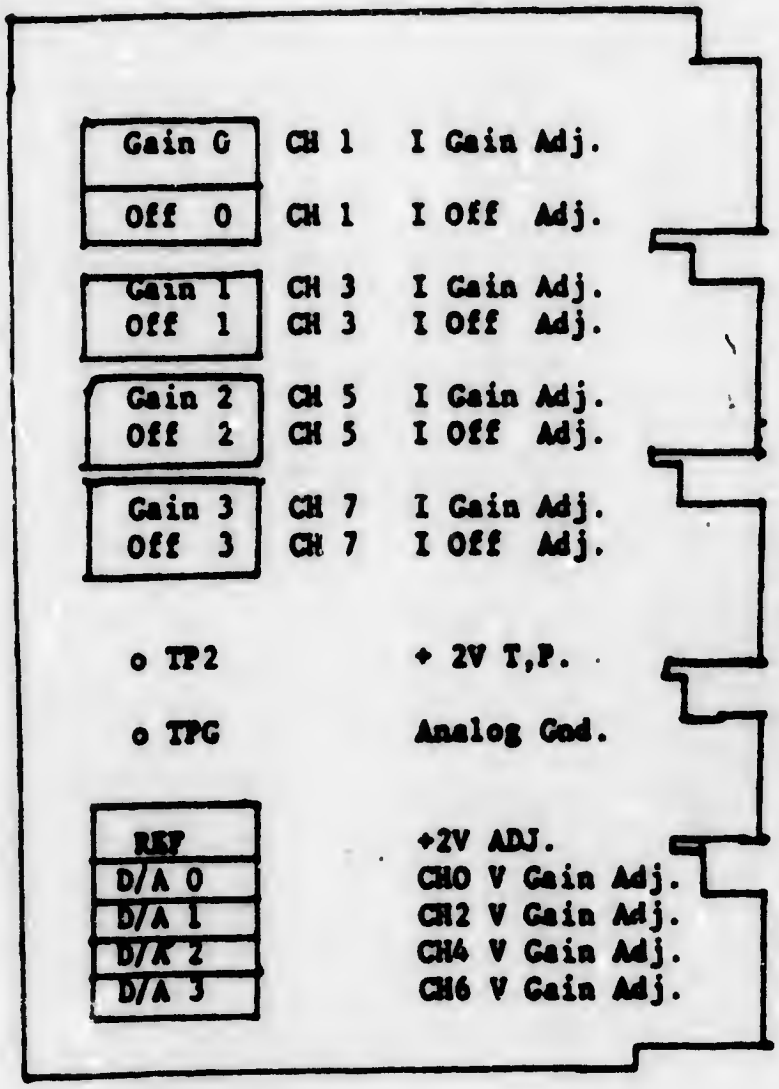
TABLE 6

CALIBRATION TABLE FOR A005-YA

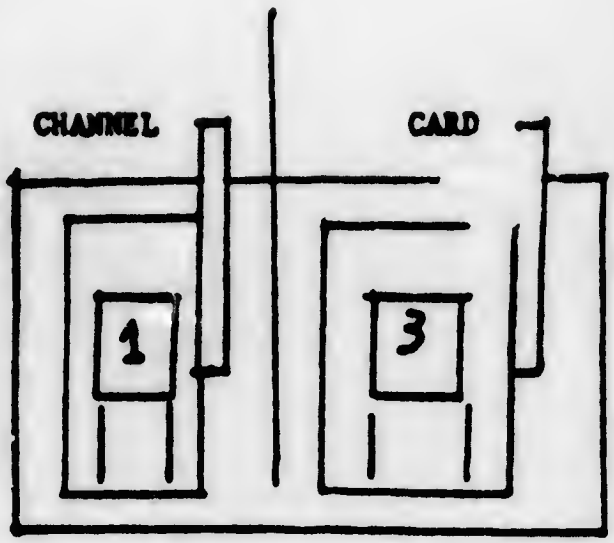
EDC Output			Channel		Average		Tolerance (LSB)	
Bipolar	Unipolar	Gain	A005-YA	A007	Bipolar	Unipolar	Bipolar	Unipolar
+0V	+0V	1000	10	*	0000	0000	+4	+6
+0V	+0V	500	10		0000	0000	∓2	∓3
+0V	+0V	250	10		0000	0000	∓2	∓3
+0V	+0V	125	10		0000	0000	∓2	∓3
+5MV	+5MV	1000	10	*	2000	4000	+5	+8
-5MV	----	1000	10		6000	----	∓5	--
+9MV	+9MV	1000	10		3463	7146	+5	+10
-9MV	----	1000	10		4315	----	∓5	--
+10MV	+10MV	500	10		2000	4000	∓3	+5
+36MV	+36MV	250	10		3463	7146	∓3	∓6
+40MV	+40MV	125	10		2000	4000	∓3	∓5
+0V	+0V	50	10		0000	0000	+2	+3
+0V	+0V	12.5	10		0000	0000	∓2	∓3
+0V	+0V	2.5	10		0000	0000	∓2	∓3
+0V	+0V	1	10		0000	0000	∓2	∓3
+180MV	+180MV	50	10		3463	7146	+2	+4
+400MV	+400MV	12.5	10		2000	4000	∓2	∓4
+3.6V	+3.6V	2.5	10		3463	7146	∓3	∓5
+5V	+5V	1	10		2000	4000	∓2	∓4
+9.9609V	+9.9609V	1	10	*	3770	7760	+3	+5
-9.9804V		1	10	*	4007	----	∓3	--
-5.0V		1	10		6000	----	∓2	--

* Channel to be used for each A007

A007 #	1	2	3	4	5	6	7
CHANNEL	21	42	63	84	105	126	147



A6330 DAC Module
Top View



V0 -	0		0
I0 -	1		1
V1 -	2		2
I1 -	3		3
V2 -	4		4
I2 -	5		5
V3 -	6		
I3 -	7		

THUMBWHEEL SWITCH
FRONT VIEW

FIGURE 1

A6765

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE ICR-11 INDUSTRIAL SUB-SYSTEM PROCEDURE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	Prev. 7668001-0-6165					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Sekemiewski		A	SP	MAA6165-0-0	B

ICR-11 INDUSTRIAL SUB-SYSTEM PROCEDURE

1.0 SPECIAL INSTRUCTIONS

1.1 No slots may be empty between A005 and A007 modules.

1.2 W7440 modules must never be installed in ICS file slot #9.

1.3 A907 must be installed between A005/A007 and the M8030/M8050 modules (s), when the latter is located within four (4) slots of the A005/A007 modules (s).

1.4 ICS-J continuity Jumper Card must be installed in the "F" connector block of all open slots between the first and last interruping module of a file.

1.5 Mercury wetted relay modules (A005, A007, M8030, M8050) must reside in a vertical plane for a period of at least one (1) minute, to prevent module damage resulting from a shorted relay.

1.6 Interrupting modules closest to the control module has highest priority within the file, and that file closest to the processor has highest priority within the ICR-11.

1.7 Options IAC-IA, IAC-IB, IAC-OA, and IAC-OB shall be system tested as IDC-ID, IDC-IE, IDC-OA and IDC-OB respectively.

Modules used in these configurations must have jumper W1 installed, only after completion of all system testing.

1.8 The A005-YA is a computer special system's variant, that shall require program modification to the in-house AUTOCAT diagnostic.

1.8.1 Ref. table 7 for diagnostic changes.

1.8.2 Ref. A-SP-A005-0-8, Section 7, for A005-YA explanation.

1.8.3 Field Service shall reference table 8 for calibration test parameters when using the ICR-11 Field Test Program.

1.8.4 Reference the ICR -11 Field Test Program when performing recalibration of the A005-YA.

2.0 REFERENCE DOCUMENTS

Manuals:	EK-ICR11-MM
Checkout Procedures:	A-SP-A6330-0-5 A-SP-7010596
Acceptance Procedures:	A-SP-A6330-0-5 A-SP-7010596
F.S. Acceptance:	A-SP-ICR11-A-5
Module Test Procedures:	A-SP-7010327-0-1 A-SP-7011020-0-1 A-SP-14/30-0-5 A-SP-ICR11-A-7
Engineering Specifications:	A-SP-H1601-0-1 A-SP-M6850-0-8 A-SP-M6870-0-8 A-SP-M8030-0-8 A-SP-M8050-0-8 A-SP-W7410-0-8 A-SP-W7411-0-8 A-SP-W7430-0-8 A-SP-W7431-0-8 A-SP-W7440-0-8 A-SP-H772-0-3 A-SP-A005-0-8 A-SP-A007-0-8 A-SP-A907-0-8 A-SP-6330-0-8 A-SP-H1501-0-1 A-SP-ICR11-A-1
Print:	B-DD-ICR11-A & C B-DD-H912-0 B-DD-IDA-0 B-DD-ICJ-I B-DD-ISH-I B-DD-IDC-0 B-DD-IDC-I B-DD-IAD-I B-DD-IMX-I B-DD-IRL-0 B-DD-7010596-0 B-DD-7010327-0

MainDec Listings: AUTOCAT-11-QZIRA (FA&T only)
AUTOCAT-11-QZIRB (HVM only)
MD-11-DZIRA
MD-11-DZIRB (Field Service only)

3.0 REFERENCE TEST EQUIPMENT

3.1 7010596 System Tester (in-house) w/ I/O Extender cables.

3.2 Oscilloscope, tektronic 465 or equivalent.

3.3 A6330, DAC Tester.

3.4 "11" family processor, with 8K memory.

4.0 SPECIAL INSPECTION/CHECK

4.1 Ensure System Components agree with ICR line items on the Customer Requisition Form.

4.2 Ensure an Electromagnetic Shield is present between the M8096 and the first I/O Module for each ICS File Box.

4.3 Verify each ICS File Box Module (s) are installed according to the approved priority sequence table. See Table 1.

4.4 Verify File Box (s) are securely grounded to the mounting cabinet and that the latter is secured System Power Ground. (use ohm meter)

5.0 CONFIGURATION GUIDELINES

5.1 All ICS option modules are to be installed using the slot-priority sequence table. See Table 1.

5.2 H912 mounting terminals must not be installed in cabinets containing sensitive equipment, such as disks or tapes.

5.3 ICR modules are to be installed per approved placement. See Figure 1.

6.0 TEST SET-UP

Refer to test procedure A-SP-7010596-0-0 and A-SP-A6330-0-5. Module configuration: see Table 1 thru 6.

6.1 Mechanical Checkout

6.1.1 There are two distinct mechanical variations to the ICR11: the ICR11-A, which is a cabinet mountable version; and the ICR11-C (NEMA), which is enclosed for use in harsh industrial environments. Both units are electronically identical with the exception of a heat circuit present only in the ICR11-C.

6.1.2 The ICR11-C version will be shipped to the FA&T line on an enclosed skid. Before proceeding, it will be necessary to remove the shipping container cover. This is accomplished by removing (8) bolts at the base of the cover.

6.1.3 Remove top rear module card guides to allow for insertion of system test cables.

6.1.4 ICR11-A - Connect the I/O test cables to all options mounted within the file, except IAD-0A (A0005), IMX-IA (A0007) or IDA-0A (A6330). Options IAD-IA and IMX-IA require special test gear hardware, IDA-0A option tester. (reference procedures ICS/ICR systems tester procedure A-SP-7010596-0-0 and IDA-0A (A6330) Checkout Procedure A-SP-A6330-0-5 for detailed information on configuring and connecting those testers).

NOTE: Do not attempt to run IDA-0A options with IAD-IA and IMX-IA options connected to the system tester.

6.1.5 ICR11-C - All conditions in step 6.1.4 hold true for the ICR11-C, but it will be necessary to add extendor cables to the I/O System Test Cables in order to make the necessary connections within the NEMA casting.

This can be best accomplished by opening the front door to the NEMA casting, and removing the four (4) file retaining screws. Slide the file forward about six (6) inches. Now open both side access doors to the NEMA. Connect the mating end of the extender cable to the I/O system test cable. Snake the remaining end up into the NEMA conduit hole located on the bottom of the casting. Work the cable up into the back of the casting until the connection can be made with the option mounted within the file.

6.1.6 It is best to connect options in the center of the file and work out to both ends. Each conduit hole is capable of excepting eight (8) cables, so if sixteen (16) options accompany the file, both conduit holes must be used. After all option cables are connected, slide the file back in, and close all three NEMA doors. All testing should be accomplished on the file in this manner.

6.1.7 Insert the Master Control and Interface Modules (M8094, and M8098) into the provided DD11B block or available SPC slots on the system. Be sure that all jumper locations are correct. (Ref.table 2-6)

6.1.8 Check the following hardware for proper installation against the ICR11 Engineering Print Set #B-DD-ICR11-A and C.

BC08 Cables (Master and Slave connections)-Teletype Jumper Connector #7011532 25 foot serial interface cable between master and slave M8098 modules #7011259.

NOTE: ICR11-C version only - disconnect the slave M8098 Digital cable from the inside bulkhead connection. This is necessary to facilitate mating of the serial interface test cable #7011259. Route the test cable up thru the bottom conduit hole before connecting to the pigtail.

6.1.9 Reference the ICS systems tester procedure #A-SP-7010596-0-0 for proper internal conversion and panel switch settings to be used on the system configuration to be tested.

NOTE: System Tester's BC11-A bus cable plugs into last unibus slot of the customer's system. DO NOT PLUG THIS CABLE INTO THE ICR FILEBOX UNDER TEST.

7.0 SYSTEMS TEST

7.1 Power up both the system tester and the system under test. Also, if the IDA-0A option tester is to be used at this time, it should also be turned on. Allow 30 minutes for this system and test gear to stabilize.

7.2 ICR-11 Controller Tests

NOTE: it is not necessary to have the ICS system tester connected to the system under test to perform this testing.

7.2.1 Load the "ICR Controller Diagnostic MAINDEC-11-DZIRA" using standard Digital Loading Procedures.

7.2.2 Set switch register to 224 and load address.
NOTE: This starting address includes power fail testing.

7.2.3 Reset the switch register to 1000 and press start.
NOTE: Reference diagnostic write up MAINDEC-11-DZIRA-D for additional information and switch settings if desired.

7.2.4 Check the system map against the system configuration to insure that all files reported on exist, and that all that exist, are reported.

7.2.5 Power fail test each remote filebox on the system, as instructed to do so by the program. .....

7.2.6 Upon completion of the Power Fail Test, run the diagnostic for time specified for every file on the system. Therefore, a two file system will have a diagnostic run time of doubled. When the prescribed run time has been reached, lower switch 09 to terminate the test and obtain the run summary typeout.

7.2.7 Acceptable error count for the run summary should be 0. Should errors or line errors be encountered, the system shall be considered unacceptable. Repairs shall be initiated and the program rerun for the specified time, until an error free pass is achieved.

7.3 ICR11 Systems Test Program

NOTE: This diagnostic requires the use of a ICS system tester.

7.3.1 Load the ICR systems test program diagnostic AUTOCAT-11-QZIRA using standard Digital Loading Procedures.

7.3.2 Set switch register to 200 load and start.

7.3.3 Enter the octal number of the file to be tested.

7.3.4 Enter the vector address of the same file. Address range 234-777.

7.3.5 Enter (self <cr>). This will automatically run a self test of the system tester to verify that all internal workings of the tester are operative. Should errors be encountered during this run, repairs should be instituted before proceding.

NOTE: System tester cables should be disconnected from the following option modules before attempting to run "self test". If not, false interupts will be generated by the customer's file. IDC-IB, IDC-IC, IDC-IE, and IAD-IA.

7.3.6 Enter (Z <cr>) to clear any previous job buffer entry.

7.3.7 Enter the I/O options mounted within the ICR file to be tested. This file maybe 1 of 12 possible files on the system. (See Figure 2)

7.3.7.1 Should the file configuration include IDA-OA options, (A6330) do not enter them at this time.

NOTE: It is not necessary to remove this option while testing all other options, but do disconnect the EDC input from the IDA-OA option tester. (ref. A-SP-A6330 option test procedure). Sample entry:

#EA005<CR>Enter one A005 in slot address 00 real address 171000. Module connected to system testers analog cable.

#EA007,4<CR>Enter four A007's in slot addresses 02,04, 06, and 10 real addresses 171002 to 171010 modules connected to system testers analog cables.

#EW7411,5<CR>Enter five W7411's in slot addresses 171012 to 171022 modules connected to system testers DC cables 0 thru 4.

#S-30<CR>Set slot address equal to 30.
NOTE: We are not running A6330's at this time, so slot addresses 24 and 26 have been bypassed.

EM6850,4⟨CR⟩ Enter four M6850's in slot address 30 thru 36. Real addresses 171030 thru 171036.

This completes the loading of the program job buffer to run all modules with the exception of both A6330's.

7.3.8 Type in (L⟨CR⟩) to obtain the module entry loaded into the program. This should be checked against your entry to verify that all entries were made correctly.

7.3.9 After entering the modules into the job buffer, type in (K⟨CR⟩) The program will respond with K ON. This will enable the program to run non stop.

7.3.10 Type in (R⟨CR⟩). This will initiate the test on the file box.

NOTE: Should the program be halted during pass 2, it should not be restarted for 30 minutes, if IAD-IA options are within the filebox configuration. This is to allow for stabilization of flying caps mounted on this module.

7.3.11 Run the diagnostic for a minimum of (1) time specified, or (1) one complete pass. Whichever is longer.

7.3.11.1 The current pass count can be obtained by typing "p" on the teletype.

NOTE: If the ICS file has a maximum load of (16) sixteen analog modules (worst case diagnostic run time), a complete pass will take approximately 1 hour and 40 minutes.

7.3.11.2 Connect all I/O cables from the ICR to the H009 MTC panel (after tests have been run successfully in Acceptance), and have QC inspect the installation.

7.4 ICR 11 Systems Test Program In Conjunction With IDA-OA Option Tester.

7.4.1 Discount all I/O system tester cables from the files that were previously tested.

7.4.2 Reference steps 6.1.3 and 6.1.4 on connecting the IDA-OA option tester if not previously done. Five A6330's can be connected to the option tester at this time, but they will have to be scoped independantly of one another.

NOTE: Don't forget to reconnect the EDC output cable for the IDA-OA option tester.

7.4.3 Enter (Z⟨CR⟩) on the teletype to clear all previously entered jobs.

7.4.4 Enter (K ⟨CR⟩) on the teletype to check what state the "K" command is in. The K command for this test should be in the off mode.

7.4.5 Enter the slot address location for all the IDA-OA options within the file.
NOTE: Only (5) five IDA-OA options can be connected to the tester. If others are present, they can be tested upon the completion of this test.

Example of loading technique to be used for IDA-OA options shown in figure 2.

S = 24 ⟨cr⟩ Set slot address equal to 24
E A6330, 2 ⟨cr⟩ Enable A6330's in slot addresses 24 and 26 real addresses 171024 and 171026, Jobs 0 and 1 respectively.

This completes the loading of both A6330's shown in figure 2.

7.4.6 Adjust all settings for the scope, and switch the option tester to the first option (card/cable output) Job 0. (reference A6330 option test procedure A-SP-A6330-0-5).

7.4.7 Type in RJO⟨cr⟩. This will initiate pass 1 testing on the first IDA-OA option or job 0 at slot address 171024. (see step 7.4.5) ramps will be outputed to the option for scope measurements.

7.4.8 Compare the scope waveform against the tolerances indicated within the option test procedure A-SP-A6330-0-5. If the option is found to be within tolerence, proceed to the next step. If not, repair, adjust, or replace the option, and retest until acceptable.

7.4.8.1 To adjust the A6330, or IDA-OA Option, proceed as follows: (Ref. figure 3)

A. First measure the cards Reference Voltage between "TP2" and "TPC". It should be +2 volts ± 2mv. If out of spec, use the "+2 v adj." pot to adjust it within tolerence.

B. Set the thumbwheel switch to the card under test.

C. Set the thumbwheel switch to channel 0 or the first voltage output.

D. Adjust pot "D/A 0" gain adjust for channel 0. The output on the scope should be adjusted within the ±20mv tolerence.

E. Set the thumbwheel switch to channel 2 or the second voltage output.

F. Repeat step D, but use pot marked "D/A 1" gain adjust.

G. Repeat steps C thru F for remaining two voltage channels 2 and 3 (thumbwheel settings 4 and 6 respectively).

H. Reset thumbwheel switch to channel 1. This is the first current output channel.

I. Adjust the current offset of channel 1 as close as possible ground by using pot. "off 0"

J. Adjust the current gain of channel 1 to fall within the required ± 20 mv tolerence.

K. Reset the thumbwheel switch to channel 3 or the second current output.

L. Repeat steps I thru J and repeat these steps for the remaining current outputs, channels 5 and 7.

7.4.9 Type "Control C" to terminate the test.

7.4.10 If other IDA-0A options have been entered, type in the next job to be run. For example, Job 1 would be entered next for the Figure 2 Configuration. Repeat steps 7.4.7 thru 7.4.9 until all jobs have been tested.

7.4.11 Turn "K" command on by typing "K" on the terminal.

7.4.12 Enter R <cr> and run all IDA-0A options entered in step 7.4.5 for time specified. With the "K" command on, pass 2 will only be run during this test. It is not necessary to scope the outputs for this test.

7.4.13 Type "Control C" to terminate the test.

7.4.14 Repeat steps 7.4.6 thru 7.4.10. Should any of the options fail, repair, and repeat all tests.

7.4.15 If there are more than (5) five IDA-0A options within this file, it will be necessary to repeat steps 7.4.5 thru 7.4.14 to test the remaining.

7.5 Repeat all tests 7.3. thru 7.4.15 for all other files on the systems configuration.

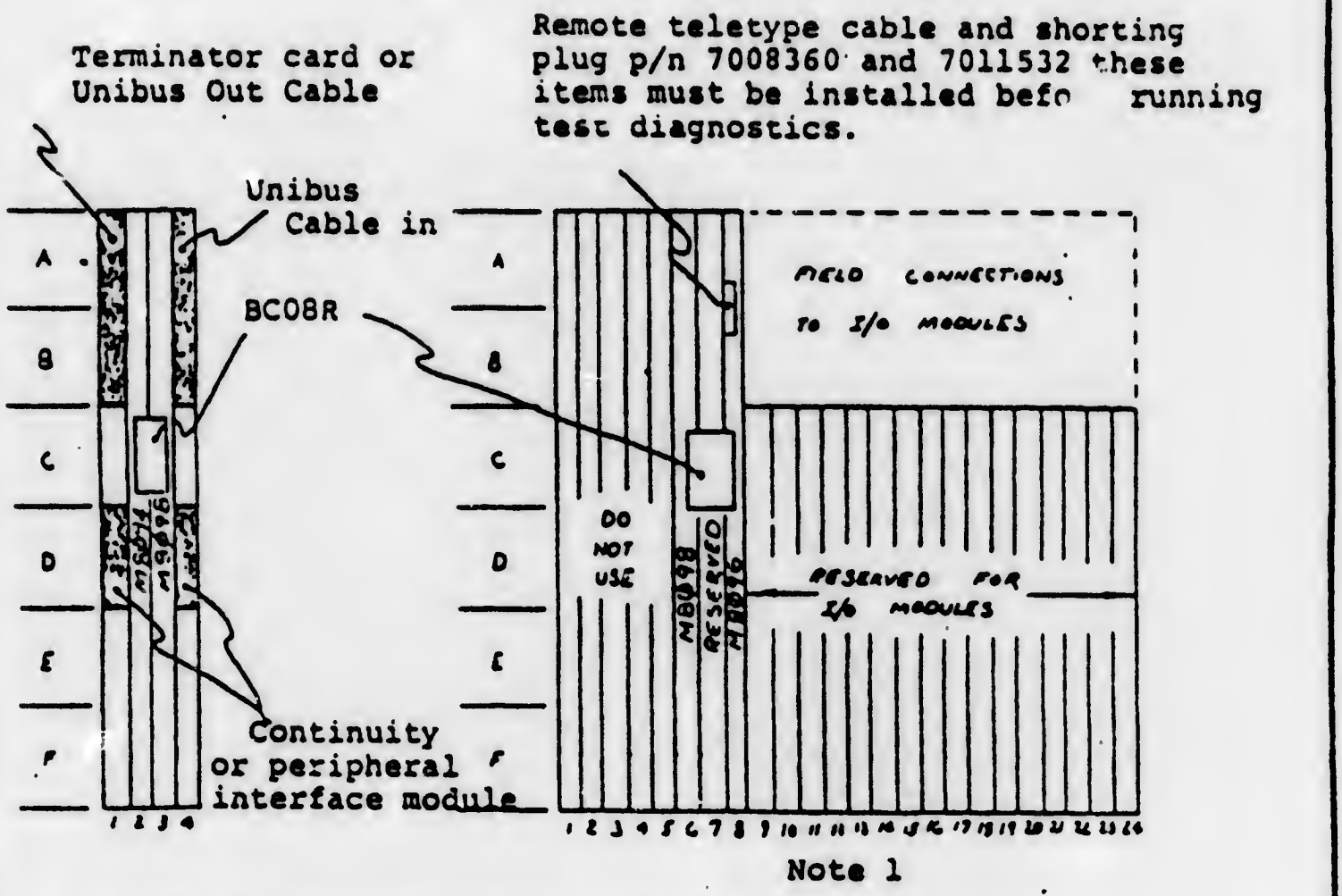
7.6 ICR11 Field Test Program

NOTE: This diagnostic requires the use of a Field UDC/ ICS Tester.

7.6.1 Reference specification A-SP-ICR11-M-5 for indepth explanation.

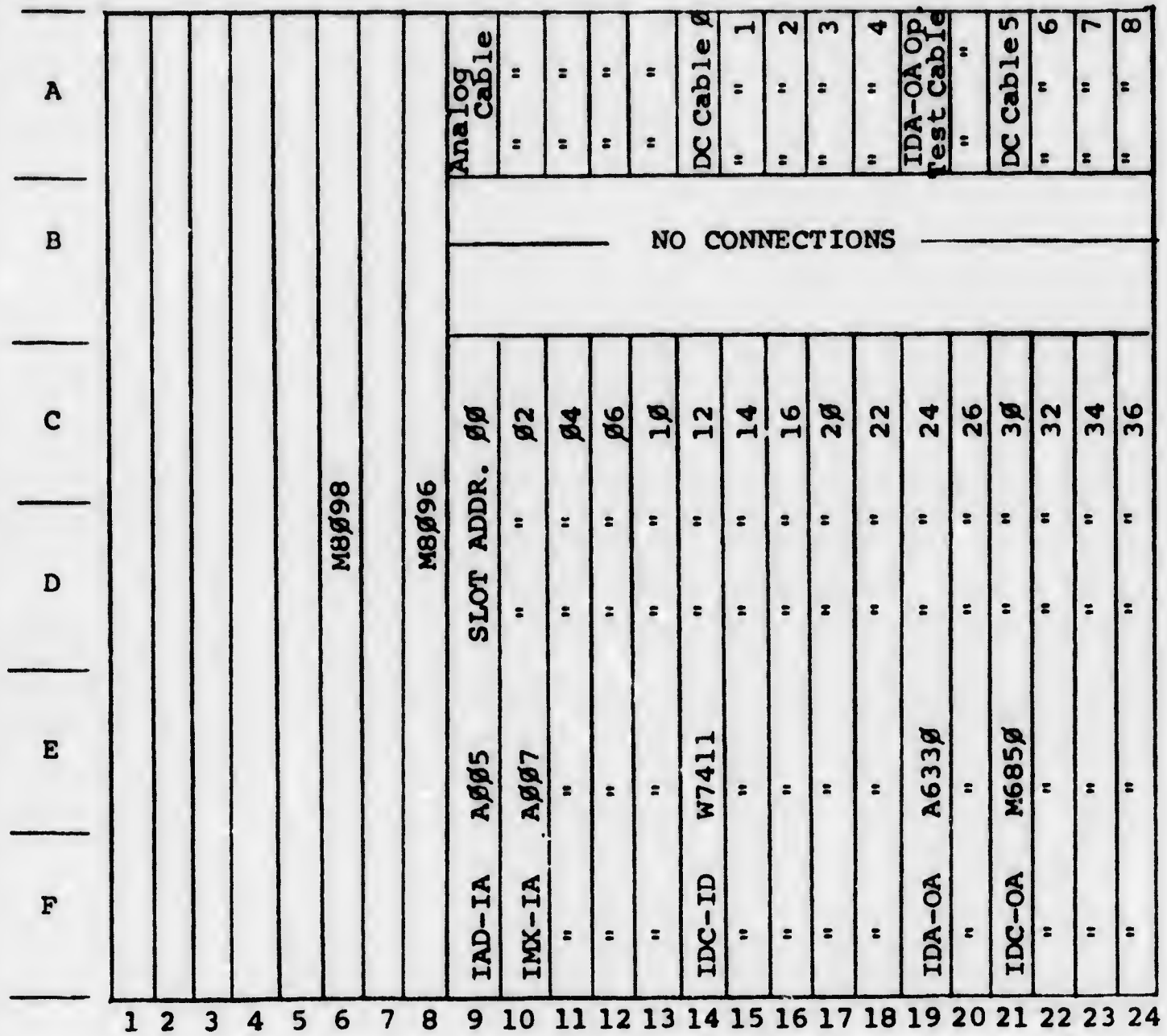
FIGURE 1

CONTROL AND INTERFACE MODULE ASSIGNMENTS AND CABLE LOCATIONS:



EXAMPLE OF TYPICAL FILEBOX CONFIGURATION

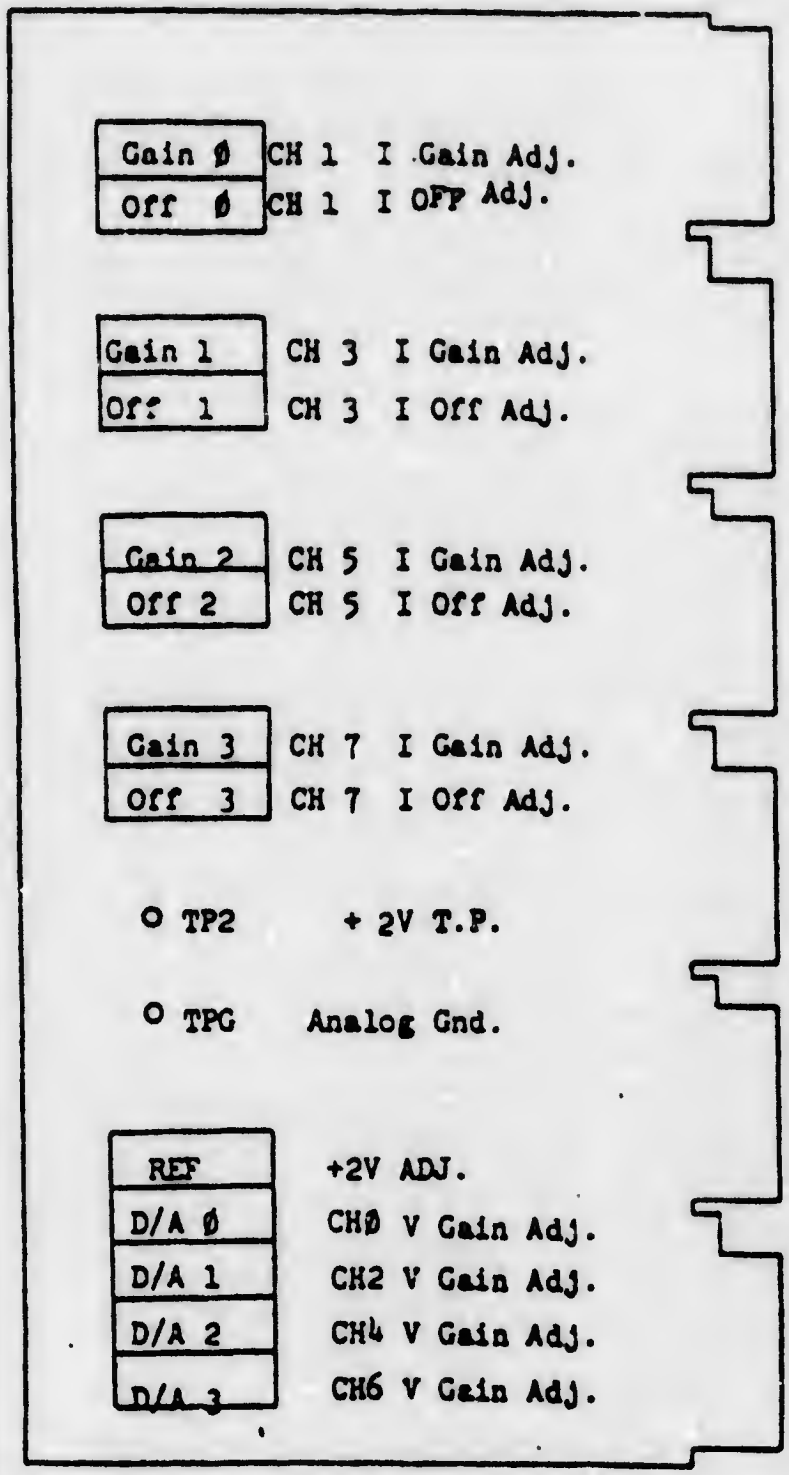
NOTE; A6330 will be tested upon completion of this test.



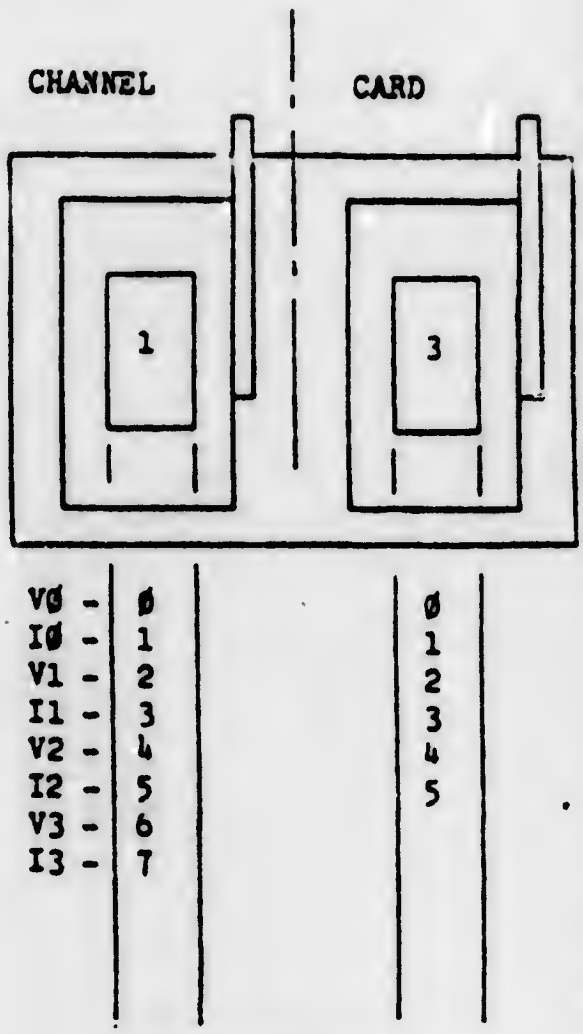
Physical Slot Location
FIGURE 2

NOTE: For module address locations other than filebox Ø reference 9.1 of the diagnostic write-up autocat-11-QZIRB.

Operator entry on teletype for configuration shown in fig. 2.



A6330 DAC Module
Top View



THUMBWHEEL SWITCH
FRONT VIEW

FIGURE 3

TABLE 1

FILE BOX - MODULE PRIORITY TABLE

PRIORITY SEQUENCE	MODULE	OPTION	COMMENTS
1	A005	IAD-IA	
2	A007	IMX-IA	7 MAX
3	A005	IAD-IA	
4	A007	IMX-IA	7 MAX
5	A907	ISH-IA	
6	W7410	IDC-IA	
7	W7411	IAC-IA	H912, + BC40J
8	W7411	IDC-ID	
9	W7440	IDC-IC	
10	W7430	IDC-IB	
11	W7431	IAC-IB	H912, + BC40J
12	W7431	IDC-IE	
13	A6330	IDA-OA	11 MAX
14	M6870	IDC-OB	
15	M6870	IAC-OB	H912, + BC40J
16	M6850	IDC-OA	
17	M6850	IAC-OA	H912, +BC40J
18	M8030	IRL-OA	
19	M8050	IRL-OB	

TABLE 2

A005 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W108	OUT	INTERRUPT MODE
W111	IN	ICS-11

A007 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W21	OUT	SELECT MUX # 1
W22	OUT	SELECT MUX # 2
W23	OUT	SELECT MUX # 3
W24	OUT	SELECT MUX # 4
W25	OUT	SELECT MUX # 5
W26	OUT	SELECT MUX # 6
W27	OUT	SELECT MUX # 7

W7430 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W58	IN	INTERRUPT MODE
W59	OUT	ICS-11

W7431 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W 9	OUT	INTERRUPT MODE
W10	IN	JCS-11

TABLE 3

W7440 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W 2 W16	IN OUT	ICS-11 INTERRUPT MODE

M8094 STANDARD JUMPER CONFIGURATION

File No.	ICSR/ICAR JUMPERS									
	A12 W22	A11 W21	A10 W20	A9 W19	A8 W18	A7 W17	A6 W16	A5 W15	A4 W14	A3 W13
00	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT
01	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	IN
02	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	IN	OUT
03	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	IN	IN
04	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	OUT	OUT
05	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	OUT	IN
06	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	IN	OUT
07	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	IN	IN
08	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	OUT	OUT
09	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	OUT	IN
10	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	IN	OUT
11	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	IN	IN

Jumper OUT = Logic "1"
Jumper IN = Logic "0"

TABLE 4

M8094 FILE JUMPERS

File No.	F3 W12	F2 W11	F1 W10	F0 W9
0	IN	IN	IN	IN
1	IN	IN	IN	OUT
2	IN	IN	OUT	IN
3	IN	IN	OUT	OUT
4	IN	OUT	IN	IN
5	IN	OUT	IN	OUT
6	IN	OUT	OUT	IN
7	IN	OUT	OUT	OUT
8	OUT	IN	IN	IN
9	OUT	IN	IN	OUT
10	OUT	IN	OUT	IN
11	OUT	IN	OUT	OUT

Jumper OUT = Logical "1"
Jumper IN = Logical "0"

M8094 VECTOR JUMPERS

File No.	Vector Address	VECTOR ADDRESS JUMPERS V8 W7	V7 W6	V6 W5	V5 W4	V4 W3	V3 W2	V2 W1
00*	234	IN	OUT	IN	IN	OUT	OUT	OUT
01*	300	IN	OUT	OUT	IN	IN	IN	IN
02	304	IN	OUT	OUT	IN	IN	IN	OUT
03	310	IN	OUT	OUT	IN	IN	OUT	IN
04	314	IN	OUT	OUT	IN	IN	OUT	OUT
05	320	IN	OUT	OUT	IN	OUT	IN	IN
06	324	IN	OUT	OUT	IN	OUT	IN	OUT
07	330	IN	OUT	OUT	IN	OUT	OUT	IN
08	334	IN	OUT	OUT	IN	OUT	OUT	OUT
09	340	IN	OUT	OUT	OUT	IN	IN	IN
10	344	IN	OUT	OUT	OUT	IN	IN	OUT
11	350	IN	OUT	OUT	OUT	IN	OUT	IN

Jumper OUT = Logic "1" Jumper IN = Logic "0"

TABLE 5

M8096 STANDARD JUMPER CONFIGURATION

#of Input Modules	W7	W6	W5	W4	W3
1	out	in	in	in	out
2	out	in	in	out	in
3	out	in	in	out	out
4	out	in	out	in	in
5	out	in	out	in	out
6	ou	in	out	out	in
8	ou	out	in	in	in
9	out	out	in	in	out
10	out	out	in	out	in
11	out	out	in	out	out
12	out	out	out	in	in
13	out	out	out	in	out
14	out	out	out	out	in
15	out	out	out	out	out
16	in	x	x	x	x

x = Do not care

Jumpers minimize polling time for input modules. The selected jumpers short cycle the poll counter after the last module address has been selected.
Installation of jumper W8 causes an I/O signal to be sent to all I/O modules if serial link is lost for more than 20 minutes. (must not be used by FA&T)

TABLE 6

M8098 STANDARD JUMPER CONFIGURATION

Mode Selection	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1
Master	in	in	in	out	out	out	out	in	out	out
Slave	out	out	out	in	in	in	in	out	in	in

Valid for etch Rev. "A" only.

Mode Selection	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1
Master	out	out	out	in	in	in	in	out	out	out
Slave	in	in	in	out	out	out	out	in	in	in

Valid for etch Rev. "B" or higher.

M8098 SWITCH SETTING (E80)

	Mode		
Switch	Master	Slave	Function
S1-1	on	on	ADR 0
S1-2	on	on	ADR 1
S1-3	on	on	ADR 2
S1-4	on	on	ADR 3
S1-5	on	on	ADR 4
S1-6	on	on	ADR 5
S1-7	off	on	Master/Slave Select
S1-8	off	off	Broadcast

TABLE 7

AUTOCAT DIAGNOSTIC "PATCHES"

ADDRESS TO BE CHANGED		
ICS11 AUTOCAT-11-QZICA	ICR11 AUTOCAT-11-QZICA	NEW CONTENTS
033210	033722	100020
033230	033312	100420
033250	033332	100066
033270	033352	100100
033310	033372	100500
033330	033412	100466
033346	033430	100000
033350	033432	101001
033370	033452	101004
033410	033472	101066
033530	033612	101466
033550	033632	101404
033565	033650	100000
033570	033652	101401

TABLE 8

CALIBRATION TABLE FOR A005-YA

EDC Output			Channel		Average		Tolerance (LSB)	
Bipolar	Unipolar	Gain	A005-YA	A007	Bipolar	Unipolar	Bipolar	Unipolar
+0V	+0V	1000	10	*	0000	0000	±4	±6
+0V	+0V	500	10		0000	0000	±2	±3
+0V	+0V	250	10		0000	0000	±2	±3
+0V	+0V	125	10		0000	0000	±2	±3
+5MV	+5MV	1000	10	*	2000	4000	±5	±8
-5MV	----	1000	10		6000	----	±5	--
+9MV	+9MV	1000	10		3463	7146	±5	±10
-9MV	----	1000	10		4315	----	±5	--
+10MV	+10MV	500	10		2000	4000	±3	±5
+36MV	+36MV	250	10		3463	7146	±3	±6
+40MV	+40MV	125	10		2000	4000	±3	±5
+0V	+0V	50	10		0000	0000	±2	±3
+0V	+0V	12.5	10		0000	0000	±2	±3
+0V	+0V	2.5	10		0000	0000	±2	±3
+0V	+0V	1	10		0000	0000	±2	±3
+180MV	+180MV	50	10		3463	7146	±2	±4
+400MV	+400MV	12.5	10		2000	4000	±2	±4
+3.6V	+3.6V	2.5	10		3463	7146	±3	±5
+5V	+5V	1	10		2000	4000	±2	±4
+9.9609V	+9.9609V	1	10	*	3770	7760	±3	±5
-9.9804V		1	10	*	4007	----	±3	--
-5.0V		1	10		6000	----	±2	--

* Channel to be used for each A007

A007 #	1	2	3	4	5	6	7
CHANNEL	21	42	63	84	105	126	147


A6170

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 8/7/80

TITLE DPM23 DISTRIBUTED I/O SUBSYSTEM

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Updated and revised	MA-A0000 ML010				

ENG	APPD	SIZE	CODE	NUMBER	REV
BILL WHITBY	STU ESTES	A	SP	MAA6170-0-0	A

DPM23 DISTRIBUTED I/O SUBSYSTEM

1.0 INTRODUCTION .

The DPM23 is a user programmable subsystem which is based on the KDF11-AA (11/23 CPU) and interfaced to the DEC DATAWAY. It is supported under RSX11S, supports FORTRAN and MACRO, and uses DPM50 Phase 2 communications software. User programs and diagnostics are downloaded from a DPM HOST COMPUTER over the DATAWAY.

This procedure defines minimum test criteria for the base DPM23. For options added to the base, reference other appropriate mast procedures.

The base DPM23 consists of:

BA11-NC/ND	9 slot chassis and power supply
KDF11-AA	CPU with memory management
MSV11-DD	64kb mos memory
ISV11-B	DEC DATAWAY interface board set

2.0 REFERENCE DOCUMENTATION

2.1 MANUALS:

2.1.1 MICROCOMPUTER PROCESSOR HANDBOOK:	EB-15836-18/79
2.1.2 MICROCOMPUTER INTERFACES HANDBOOK:	EB-17723-20/80
2.1.3 MSV11-D,-E USERS MANUAL:	EK-MSV1D-OP-???
2.1.4 PROCESS I/O SUBSYSTEM USERS GUIDE:	EK-PIOS-UG-???
2.1.5 DPM23 USERS GUIDE:	EK-DPM23-UG-???
2.1.6 KDF11-AA USERS GUIDE:	EK-KDF11-UG-???
2.1.7 BA11-N TECHNICAL MANUAL:	EK-BA11N-TM-???

2.2 PRINTS AND SCHEMATICS:

2.2.1 DPM23 PRINTSET: MP001058
2.2.2 DLV11-F PRINTSET: MP000461

3.0 REQUIRED TEST EQUIPMENT:

3.1 HARDWARE AND MEDIA:

3.1.1 Valid DPM HOST SYSTEM configuration.
3.1.2 RSX11-M on appropriate host media.
3.1.3 Attenuation panel.
3.1.4 HEWLETT PACKARD DVM or equivalent accurate to .01V @ 15V.
3.1.5 Serial line unit IE. DLV11-F and Terminal for LSI error information output (LOCAL MODE).

4.0 REQUIRED DIAGNOSTIC PROGRAMS:

4.1 DPM REMOTE DIAGNOSTICS KIT #ZP125-RD

	NAME	DESCRIPTION	MODE
4.1.1	DZKCI	Remote terminal tester	Remote
4.1.2	DZKCH	Serial bus exercizer	Remote
4.1.3	CZKMP	Task Handler	N/A
4.1.4	DVDVC	DLV11-F test	Local
4.1.5	CZQMC	0-124k memory exercizer	Local
4.1.6	DVPCA	Pcs test	Local
4.1.7	CJKDA	F-11 MMU test	Local
4.1.8	CJKDB	F-11 CPU test	Local
4.1.9	CJKDC	KEF11-AA diag 1*	Local
4.1.10	CJKDD	KEF11-AA diag 2*	Local

*=OPTIONAL

5.0 SPECIAL INSTRUCTIONS

5.1.1 RSX11-M must be running in the host system with DPM REMOTE DIAGNOSTICS KIT #ZP125-RD.

5.1.2 A serial line interface (IE. DLV11-F,DLV11-J) and terminal will be required to run diagnostics in LOCAL MODE at the DPM23 subsystem. NOTE: These items are used for test only and are not shipped unless specifically ordered with system.

5.1.3 The M8080 is always the last item on the bus with the exceptions that the M8084 always occupies slot 9, and that the optional BDV11-AA(M8012) always plugs into slot 8.

5.1.4 At this writing only the following options are supported on the DPM23.

A.	MSV11-DD	32K WORDS MOS MEMORY
B.	BDV11-AA	TERMINATOR/BOOT MODULE
C.	DLV11-E	ASYNCHRONOUS LINE UNIT
D.	DLV11-J	FOUR ASYNCHRONOUS SERIAL INTERFACES
E.	DLV11-KA	20MA CURRENT LOOP OPTION
F.	DZV11-A	ASYNCHRONOUS MULTIPLEXER
G.	IBV11-B	INSTRUMENT BUS INTERFACE AND CABLE
H.	IPV11	Q BUS IOCM
I.	LPV11-PA/PD	LINE PRINTER OPTIONS
J.	RXV11-BA/BD	FLOPPY DISK OPTIONS
K.	RXV21-BA/BD	DOUBLE DENSITY FLOPPY DISK OPTIONS
L.	BA11-NE/NF	EXPANDER BOX

5.1.5 In order to run DCF11-AA diagnostic (CJKDB), LTC (LINE TIME CLOCK) interrupts must be disabled, to accomplish this jumper W4 must be installed on the KDF11-AA CPU module prior to testing. If a BDV11-AA (M8012) module has been added to the DPM23 system switchpack E21 #5 may be turned on instead. In either case this procedure must be reversed prior to running D BUS I/O module diagnostic VPCAEO. System must ship with LTC interrupts enabled.

6.0 INSTALLATION AND TEST SETUP INSTRUCTIONS

6.1 UNPACKING AND INSPECTION:

6.1.1 Save all packing material for equipment to be shipped that is not cab mounted.

6.2 MODULE CONFIGURATION SETUPS FOR DPM23

6.2.1 KDF11-AA (M8186) LSI 11/23 CPU MODULE

JUMPER DESIGNATION	JUMPER STATE
W1	IN
W2	AS RECEIVED
W3	AS RECEIVED
W4*	OUT
W5	OUT
W6	OUT
W7	IN
W8 THRU W15	DON'T CARE
W16	IN
W17	IN
W18	IN

*=Note: See special instruction at 5.1.5

Reference FIGURE 2 for jumper locations.

6.2.2 MSV11-DD (M8044-D?) FIRST 32K

S1 SWITCHPACK	SWITCH STATE
SW1	ON
SW2	ON
SW3	ON
SW4	ON
W2	IN
W3	IN
PIN 1 TO 3	IN
PIN 5 TO 7	IN
PIN 10 TO 14	IN
PIN 15 TO 16	IN

Reference FIGURE 4 for switch and jumper locations.

6.2.3 DLV11-F (M8028) SERIAL LINE UNIT

JUMPER DESIGNATION	JUMPER STATE
T0	OUT
T1	IN
T2	OUT
T3	IN
R0	OUT
R1	IN
R2	OUT
R3	IN

The DLV11-F is default jumpered for console use, but the above baud rate jumpers must be reconfigured from 110 baud operation to 300 baud.

The DLV11-F is not a standard part of the DPM23 system, but is a frequent option, and is needed in FA&T for diagnostic testing in LOCAL MODE. See FIGURE 5 for jumper locations.

6.2.4 ISV11-B (M8080,M8084) DEC DATAWAY INTERFACE

FACTORY CONFIGURED:

CSR ADDRESS 160140
160142
160144

VECTOR ADDRESS 300
304

JUMPERS	STATE	LOCATION
W1 THRU W6	OUT	M8080
W7 THRU W10	IN	M8080
W11 THRU W16	OUT	M8080
W17 THRU W20	IN	M8080
W21 THRU W23	OUT	M8080
W1,W3,W5,W7,W9	IN	M8084
W2,W4,W6,W8,W10	OUT	M8084

NOTE: If DLV11-J is installed in DPM23 system its default vector address of 300 must be reconfigured because of its conflict with the ISV11-B.

Reference FIGURES 7.1 and 7.2 for jumper locations.

6.3 CABLING OF THE DPM23

6.3.1 Cabling of the DPM23 consists of a serial bus cable (70-15928-03) coming from the M8084 board of the ISV11-B, which interconnects with the DEC DATAWAY cable (70-14152), which in turn is run through an attenuation panel to simulate cable length, finally exiting the attenuation panel and connecting to the HOST CPU'S ISB11. Reference FIGURE 1.

NOTE: The attenuation panel is only used for test and is not shipped with the system.

7.0 POWER CHECKS

7.1 +5VDC ±250MV
+12VDC ±600MV

The +5VDC and +12VDC regulated voltages can be measured at J7 of the backplane or, preferably at the tip jacks on the M8012 (BDV11-AA) module (if it has been added to the system). The pins of J7 are numbered, and color coded. +12VDC and +5VDC are assigned the following pins and colors.

+12VDC----------PIN 2, PURPLE WIRE
+12VDC GROUND----------PIN 3, BLACK WIRE
+5VDC----------PIN 5, RED WIRE
+5VDC GROUND----------PIN 4, BLACK WIRE

The tip jacks on the M8012 module are color coded and labeled as follows:

+12VDC----------J3, PURPLE
+5VDC----------J2, RED
GROUND----------J1, BLACK

If adjustment becomes necessary, remove the two power supply mounting screws to tilt the power supply forward exposing the adjustment potentiometers R1 for +12VDC, and R22 for +5VDC. Reference FIGURES 3.1 and 3.2 for locations.

8.0 DIAGNOSTIC TEST PROCEDURE

The host processor,whether it be an 11/70 or 11/34 along with its ISB11'S must be fully checked out according to MAST prior to connecting a DPM23 to the DATAWAY.

8.1 DPM23 HOST SYSTEM BOOTING PROCEDURE

8.1.1 Obtain a disk pack for the appropriate host media which has the RSX11-M host package #AP-F152A-MC and install it into DRIVE #0. Load DRIVE #0 and insure that "WRITE PROTECT" is off.

8.1.2 When DRIVE #0 is ready and "ON LINE" (heads loaded) BOOT the drive.

8.1.3 When the program asks for the date and time, you may either enter the information or default it by typing a carriage return. An example would be 08:30 04-JUN-80.

8.1.4 The program will continue setting up parameters and will ask: "Do you want to load IPG diagnostics from magtape [Y/N]:". Type in a carriage return which will default your answer to a NO condition.

8.1.5 The program will now output:
>@ <EOF> (This signifies end of file and parameters are now set) and waits for you to key in a command.

8.1.6 Type in:
Set /UIC=[200,270] (This may not be necessary if the UIC is already at 200,270.)

8.2 RUN THE ERROR REPORT TASK IN ORDER TO CLEAR OUT THE ERROR LOG

```
8.2.1 >RUN ISBRPT--------------------------TYPE:<RUN ISBRPT>
      ISBRPT-DEC DATAWAY ERROR REPORT TASK
      >
      PRINT SUMMARY [Y OR N]?N-------------TYPE:<N>
      PRINT ENTIRE FILE [Y OR N]?N---------TYPE:<N>
      DELETE ERROR FILE [Y OR N]?Y---------TYPE:<Y>
      ISBRPT...OPERATION COMPLETE
      TASK "ISBRPT" TERMINATED
      TASK EXIT WITH OUTSTANDING I/O
      PC=125130
      PS=170000
      R0=120720
      R1=125576
      R2=125650
      R3=000000
      R4=143470
      R5=000000
      SP=120476
```

8.2.2 Type:CTRL C to terminate ISBRPT task and receive back MCR> prompt.

8.3 RUN THE DEC DATAWAY DIAGNOSTIC EXERCISER.

```
8.3.1 >RUN DZKCH---------------------------TYPE:<RUN DZKCH>
      DCP-A>STA----------------------------TYPE:<STA>

      #UNITS (D)?1-------------------------TYPE:<1>
      ENTER CONTROLLER NUMBER:(0)0?0-------TYPE:<0>
      ENTER TERMINALS ON THAT CONTROLLER:
      (0)1?1-------------------------------TYPE:<1>
      NUMBER OF ENTERED TERMINALS=1

      UNIT**CONTROLLER**LOGICAL SB**LUN**
       001       000           001       011

      TOTAL ACTIVE PASSES = 21,ACTIVE TERMINALS=1, TIME=8:33

      TOTAL ACTIVE PASSES = 41,ACTIVE TERMINALS=1, TIME=8:34
```

8.3.2 After required run time has elapsed terminate running of diagnostic by typing CTRL C.

```
TASK "TTO" TERMINATED
TASK EXIT WITH OUTSTANDING I/O
PC=046000
PS=170000
R0=000002
R1=000000
R2=000000
R3=000000
R4=000003
R5=000001
SP=001246
```

8.4 After DZKCH has run,The error log must be checked for errors that may have occured during running.

```
8.4.1 >RUN ISBRPT--------------------------TYPE:<RUN ISBRPT>
      ISBRPT-DECDATAWAY ERROR REPORT TASK
      >
      PRINT SUMMARY[Y OR N]?Y--------------TYPE:<Y>
      PRINT ENTIRE FILE [Y OR N]?N---------TYPE:<N>
      OUTPUT TO LINE PRINTER [Y OR N]?N----TYPE:<N>
      WANT ONE CONTROLLER [Y OR N]?N-------TYPE:<N>
      DELETE ERROR FILE [Y OR N]?N---------TYPE:<N>
      ISBRPT...ERROR FILE IS EMPTY
      ISBRPT...OPERATION COMPLETE
```

8.4.2 Type: CTRL C to terminate ISBRPT task and receive back MCR> prompt.

8.4.3 Error reporting can be in the form of hard errors, typed out immediately, or soft errors;(Errors that are logged by the error logger). No errors are allowed.

8.5 RUN ROM RESIDENT TESTS OF ISV11-B

8.5.1
```
MCR>RUN CZKCIB----------------------TYPE:<RUN CZKCIB>
>
DCP-A>STA---------------------------TYPE:<STA>

# UNITS (D) ? 1-------------------TYPE:<1>

UNIT 1
ENTER CONTROLLER NUMBER:(0)0?0------TYPE:<0>
ENTER TERMINALS ON THAT CONTROLLER:
(D)1?1-----------------------------TYPE:<1>

SELECTED SERIAL LINE PORTS

UNIT**CONTROLLER**LOGICAL SB**LUN**TYPE
  1         0           001       9   DPM50-PORT 0

START OF TESTING

END OF PASS     0,   TIME = 9:29

END OF PASS     1,   TIME = 9:31
```

8.5.2 After required run time has elapsed terminate running of the diagnostic by typing CTRL C.

8.6 LOAD DIAGNOSTIC MONITOR CZKMPB

8.6.1
```
>RUN CZKMPB-------------------------TYPE:<RUN CZKMPB>
>
CZKMPB VERSION 2.2
SELECT MODE: LOCAL, HOST, AUTO-MAP, COMMUNICATION OR EXIT
(L,H,A,C,E)L-----------------------TYPE:<L>
ENTER NUMBER OF TERMINALS [D]=1-----TYPE:<1>
ENTER CONTROLLER NUMBER [0]=0-------TYPE:<0>
ENTER TERMINAL NUMBERS [0]=1--------TYPE:<1>
NUMBER OF ENTERED TERMINALS = 1
UNIT**CONTROLLER**LOGICAL SB**
  1         0           1
```

At this point the console terminal at the DPM23 subsystem comes on line and is used to ask for and run subsystem diagnostics.

8.7 RUN 11/23 CPU AND MEMORY DIAGNOSTICS ON DPM23

See Figure 6 for explanation of monitor interaction inputs and outputs at local DPM23 terminal.

8.7.1 >JKDAC0----------TYPE:<JKDAC0>
157776
@200G----------TYPE:<200G>
CJKDAC0 KTF11-AA MMU DIAG.
SWR=000000 NEW=CR----------TYPE:<CR>

END PASS# 1 ;TOTAL ERRORS SINCE LAST START AT 200 0

8.7.2 After required run time has elapsed, terminate running of the diagnostic at the DPM23 console terminal by depressing the break key.

8.7.3 @760144/000000 2----------TYPE:<760144/>
TYPE:<2>
>JKDBC0----------TYPE:<JKDBC0>
157776
@200G----------TYPE:<200G>
CJKDBC0 DCF11-AA CPU DIAGNOSTIC
END PASS# 1
END PASS# 15

NOTE: LTC interrupts must be disabled to run diagnostic JKDBC0. See special instruction at 5.1.5.

8.7.4 After required run time has elapsed,terminate running the diagnostic at the DPM23 console terminal by depressing the break key.

```
8.7.5 @760144/000000 2--------------------TYPE:<760144/>
                                           TYPE:<2>
      >ZQMCG0-----------------------------TYPE:<ZQMCG0>
      157776
      @200G-------------------------------TYPE:<200G>
      SWR=000000 NEW= CR------------------TYPE:<CR>

      KT11(MEMORY MANAGEMENT)AVAILABLE

      MEMORY MAP
      FROM 000000 TO 757777 (WITH 4 MSV11-D INSTALLED)
      NO PARITY REGISTERS FOUND
      PROGRAM RELOCATED TO 720000
      PROGRAM RELOCATED TO 000000
      END PASS# 1
```

Above will be received when 4 MSV11-D modules are installed, typeouts will vary with lesser amounts of memory. No relocation will occur when only 1 MSV11-D is installed.

8.7.6 *NOTE THE following two tests are to be run if the optional KEF11 chip is installed.

```
8.7.7 @760144/000000 2--------------------TYPE:<760144/>
                                           TYPE:<2>
      >JKDCB0-----------------------------TYPE:<JKDCB0>
      157776
      @200G-------------------------------TYPE:<200G>
      CJKDCB, KEF11-A FP DIAGNOSTIC PART 1

      SWR = 000000  NEW=CR----------------TYPE:<CR>

      END PASS #    1
      END PASS #    2
```

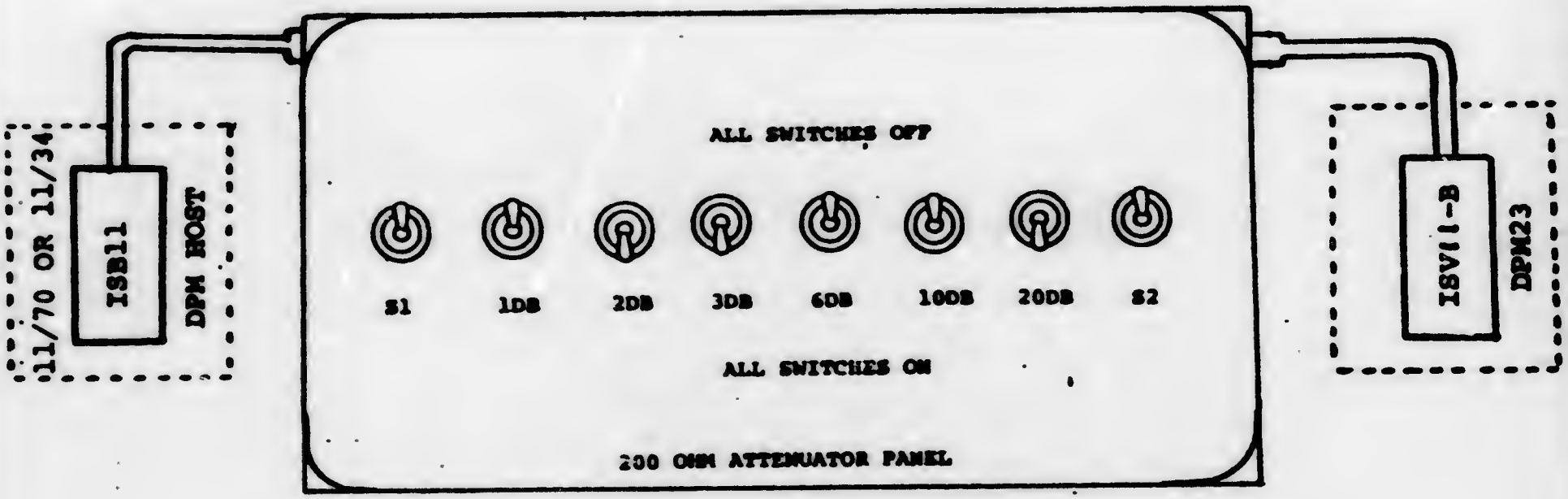
8.7.8 After required run time has elapsed, terminate running of the diagnostic at the DPM23 console terminal by depressing the break key.

```
8.7.9 @760144/000000 2--------------------TYPE:<760144/>
                                           TYPE:<2>
      >JKDDB0-----------------------------TYPE:<JKDDB0>
      157776
      @200G-------------------------------TYPE:<200G>
      CJKDDB KEF11-A DIAGNOSTIC PART 2

      SWR = 000000  NEW =CR---------------TYPE:<CR>

      END PASS #    1
      END PASS #    2
```

8.7.10 After required run time has elapsed, terminate running of the diagnostic at the DPM23 console terminal by depressing the break key.

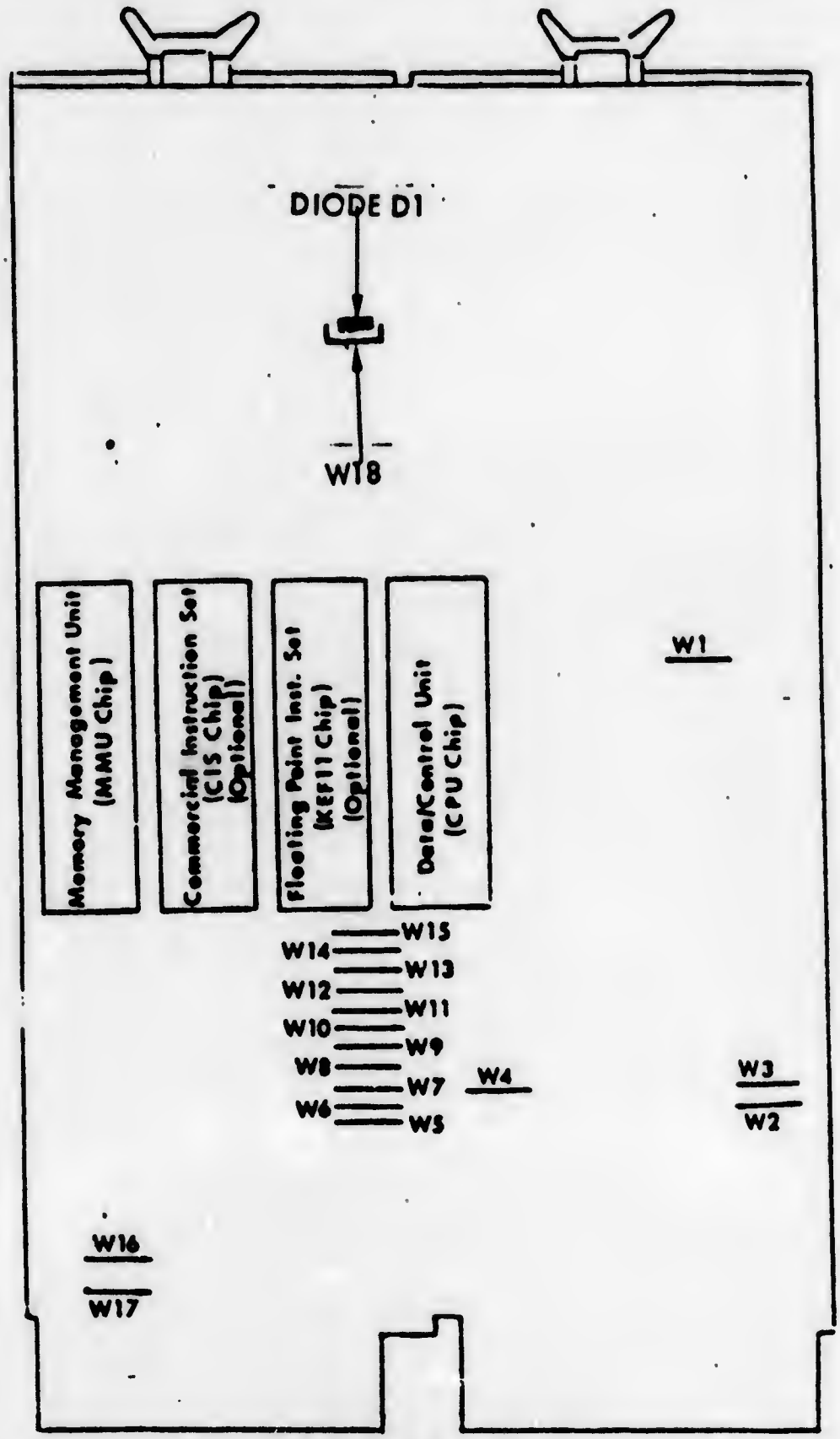
8.7.11 Load and run diagnostics for any additional LSI option modules installed, using same method used to run the CPU tests.

8.7.12 After all LSI modules have been run, if any D BUS I/O modules exist within the DPM23 subsystem, load diagnostic VPCAE0 and follow procedure POO-00COA-00-0000WM-06-0055. Reference section 4.0 DIAGNOSTIC TESTING.



# OF TERMINALS	ATTENUATOR SETTING	
1 TO 9	25DB	(SHOWN ABOVE)
10 TO 19	24DB	
20 TO 29	23DB	
30 TO 39	22DB	
40 TO 49	21DB	
50 TO 59	20DB	
60 TO 63	19DB	

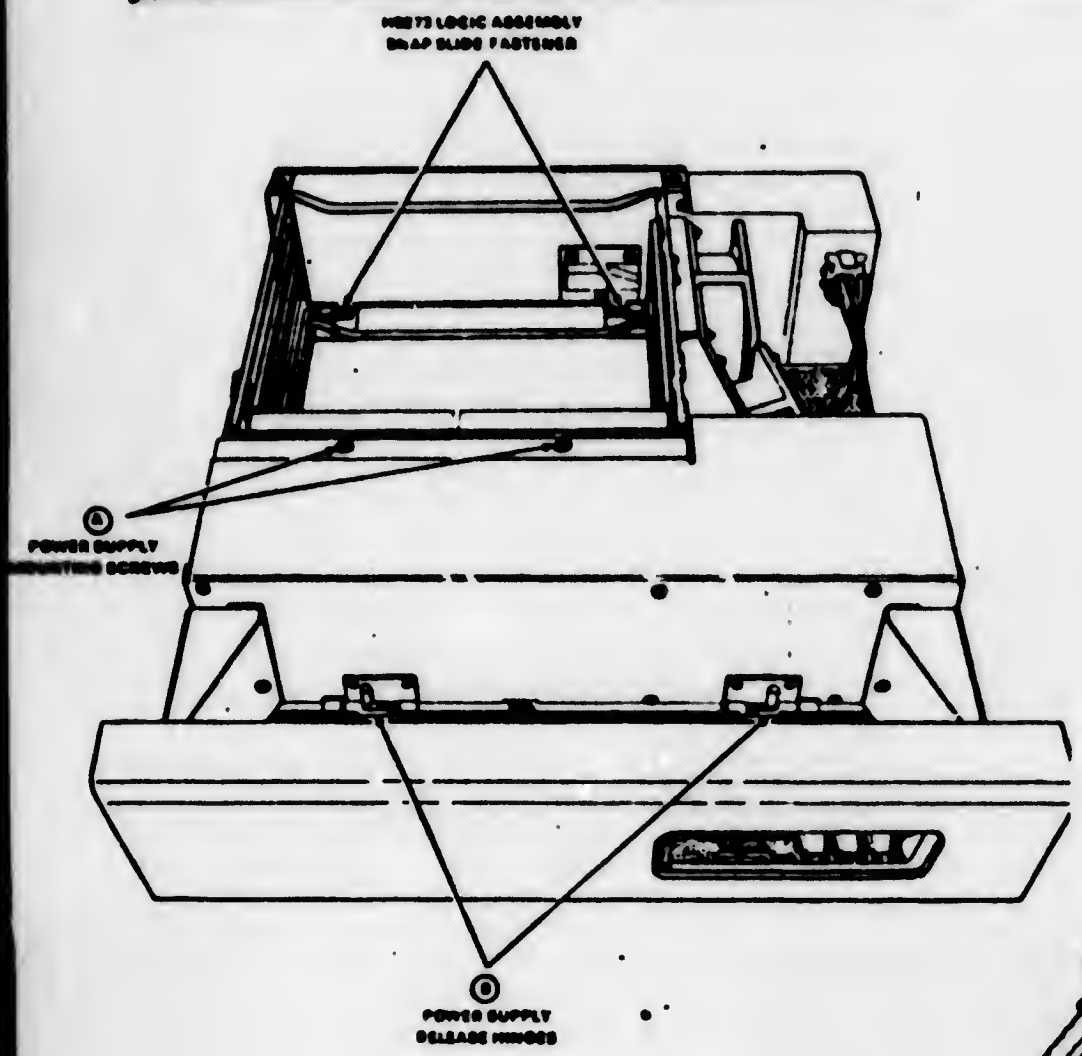
FIGURE 1



KDF11-AA

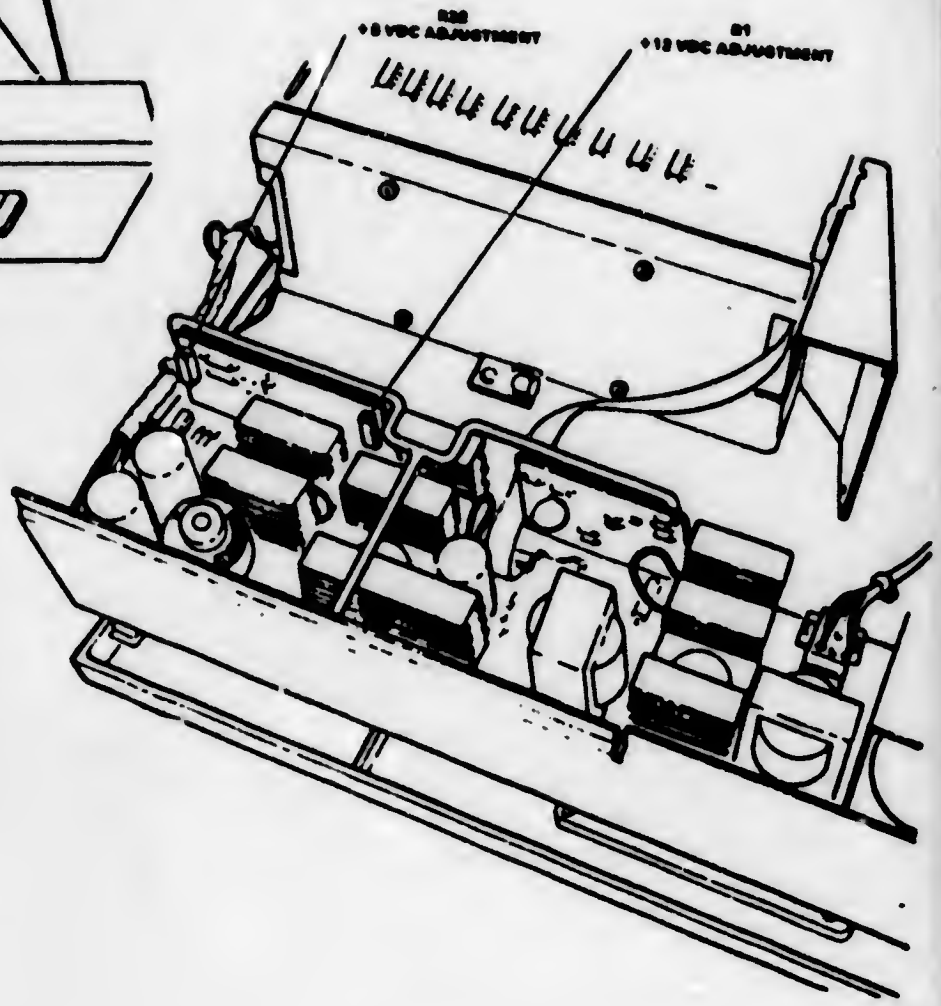
(M8186 DUAL SIZE MODULE)

FIGURE 2



Power Supply Assembly

FIGURE 3.1



Power Supply Adjustments

FIGURE 3.2

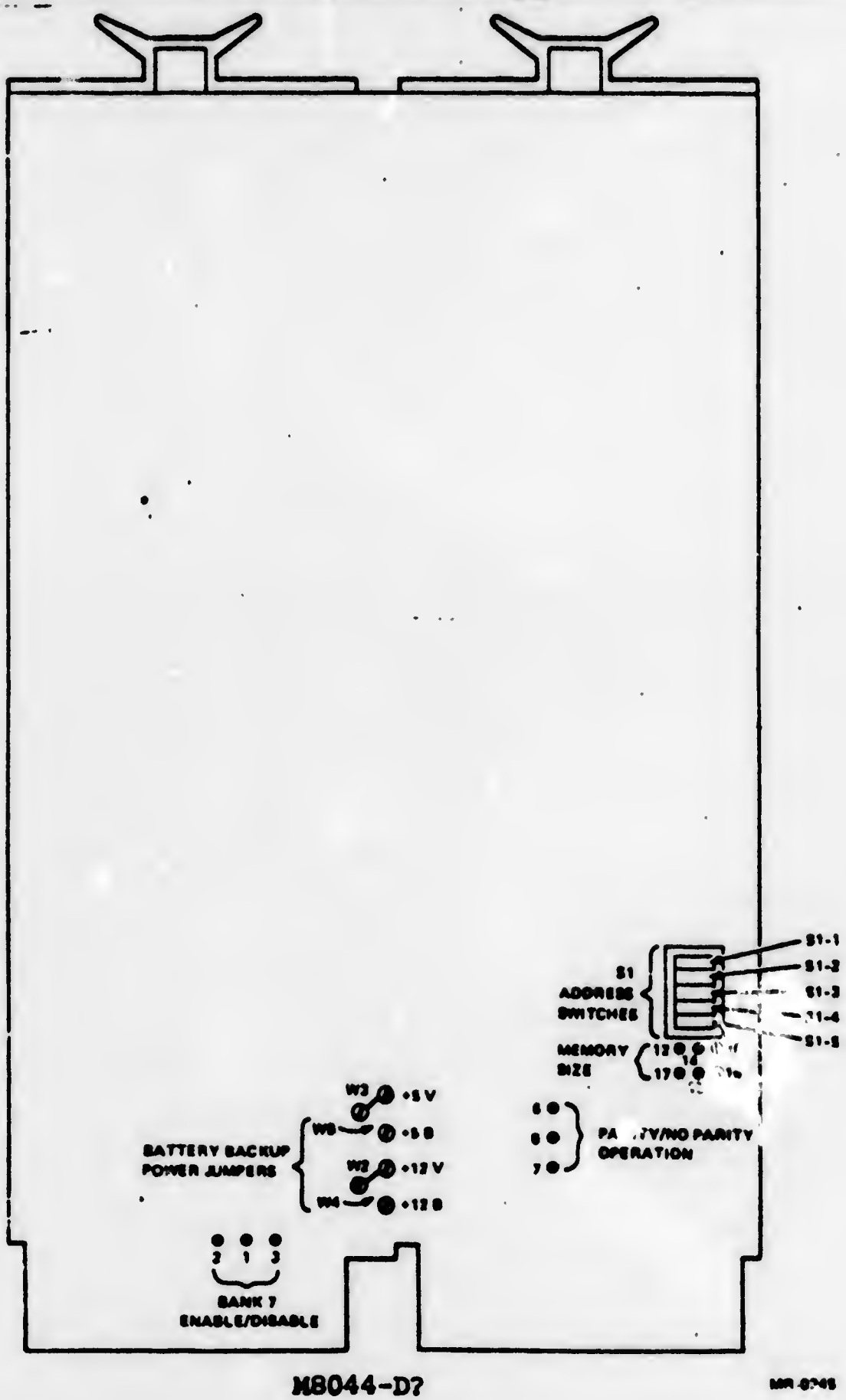


Figure 4 MSV11-D, MSV11-E Switch and Jumper Locations

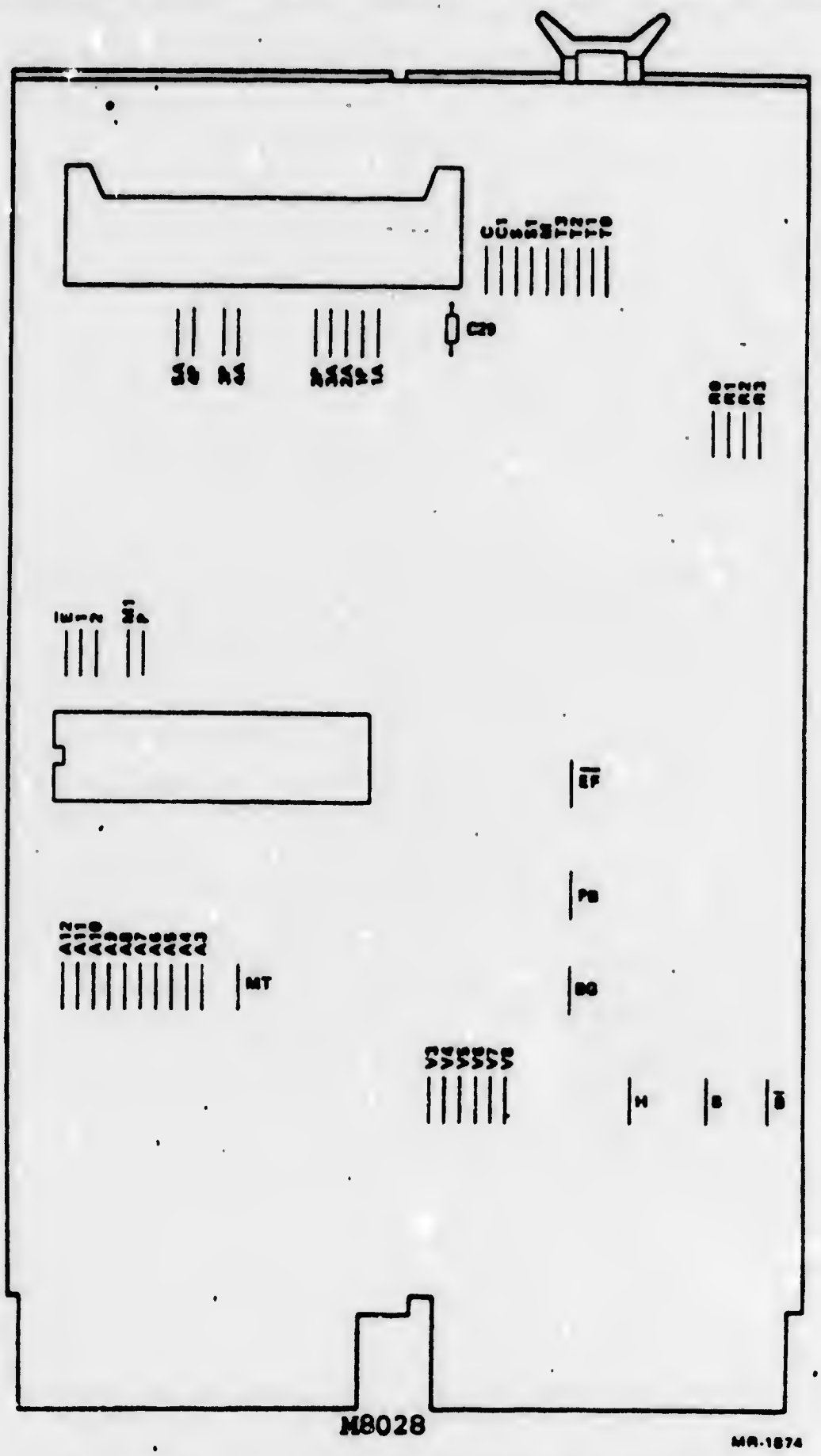


Figure 5 DLV11-F Jumper Locations

MONITOR INTERACTION AT LOCAL TERMINAL

Prompts

>	Operator may enter file name to call next diagnostic, or type control Z to put LSI-11 in ODT mode.
@	If following 157776 after a file name has been entered, indicates the diagnostic is in the LSI-11 and the operator may communicate with it via ODT. If following "End pass" and the current PC, indicates the operator may give further instructions in ODT. Giving "760144" reestablishes communication with local monitor.

Inputs

	File names	Used following ">" to call diagnostics.
	200G	Not to monitor - starts diagnostic if LSI-11 is in ODT.
	Break	Not to monitor - stops diagnostic.
	760144/	Reestablishes communication with local monitor if LSI-11 is in ODT.
Deposit	2	Following "000000" tells monitor that operator wishes to run another diagnostic.
Deposit	1	Follow "000000" aborts monitor to boot. This is the last input by the operator.
	Control P	Following ">" puts LSI-11 in ODT.

Outputs

157776	Following file name entry indicates the diagnostic has been downloaded.
NX	The requested file cannot be found.
BDLD	The attempt to download the diagnostic was unsuccessful.
END PASS	Diagnostic has completed a pass.
Current PC	Following break indicates diagnostic has stopped at address printed.
000000	Following "760144" indicates operator may input further instructions to local monitor (1 or 2).
EX	Monitor has terminated at boot.

Figure 6

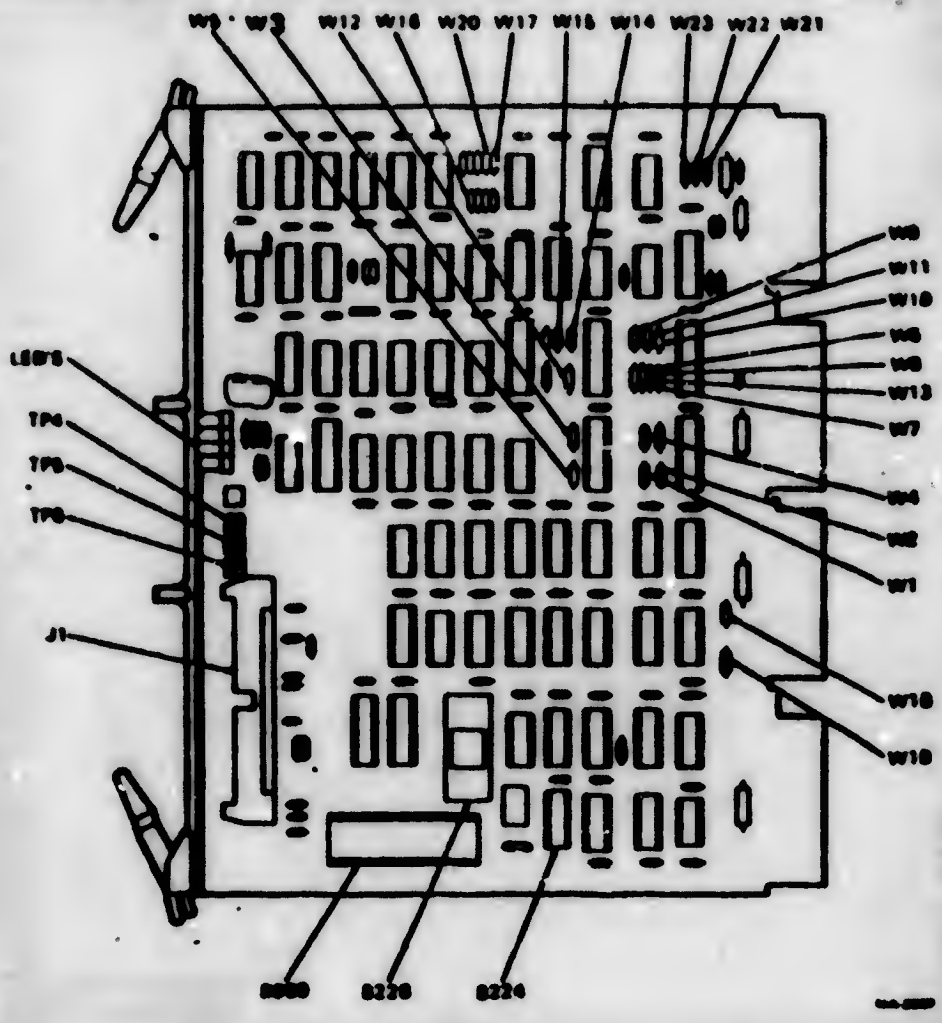


FIGURE
7.1

M8080

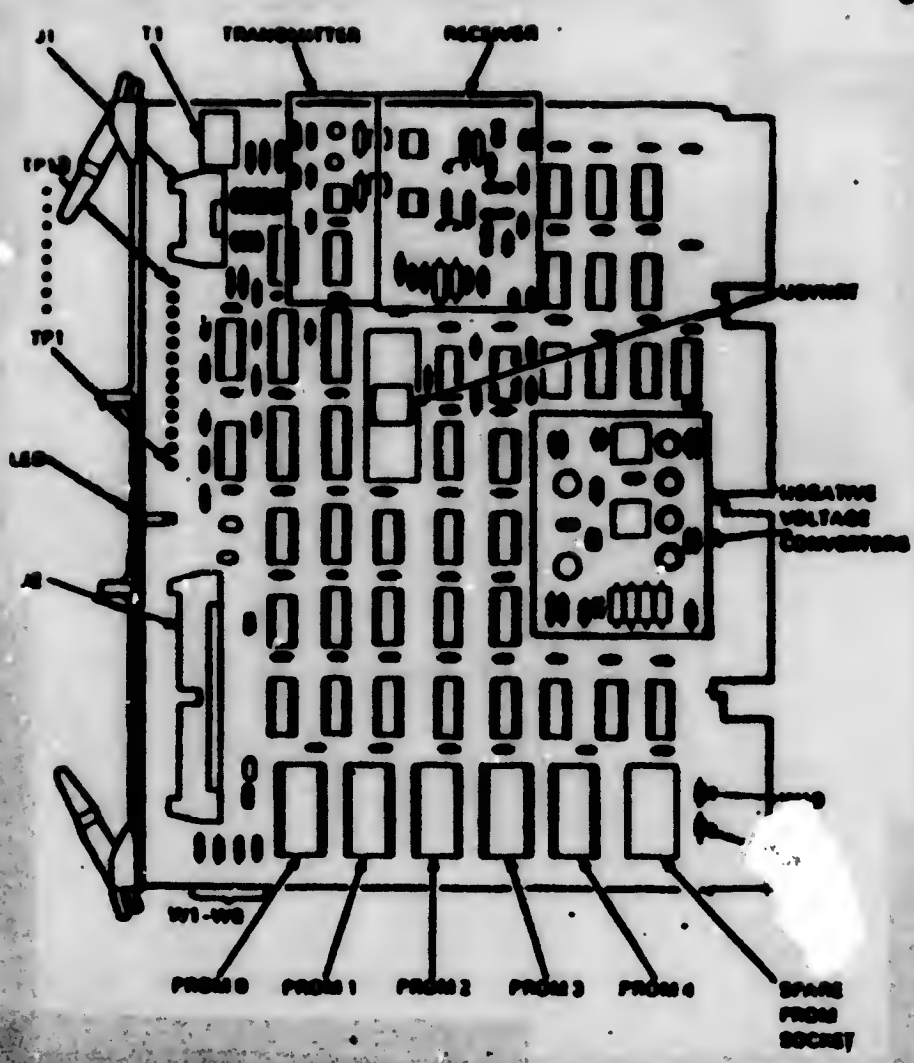


FIGURE
7.2

ISY11B

M8084

	SIZE	CODE	NUMBER	REV
	A	SP	MAA [redacted]170-0-0	A

DEC 16-[illegible]-1983-00328

A61176

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. **DATE** 11 Jan 80

TITLE ISB-11 DEC DATAWAY CONTROLLER

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6175					
B	New update ECO CHANGE	MA-A0000-ML00?7	L.LECLERC	1-80	L. LaClare (Last)	7-24-80

ENG	APPD	SIZE	CODE	NUMBER	REV
Wayne Burgett		A	SP	MAA 6175-0-0	B

EN-01063-16-00672-(398)

ISB-11 DEC DATAWAY CONTROLLER

1.0 REFERENCE DOCUMENTATION

1.1 Print sets order # MP00452

1.2 Maintenance Manual: EK-KMCMP-OP, EK-DMCLU-OP

1.3 ISB-11 Users Guide: EK-ISB-11-US

1.4 ISB-11 Field Acceptance Procedure: A-SP-ISB-11-07

1.5 Lib Kit: (KMC-11 Lib Kit) #ZJ234-RB

1.6 DZKCH Serial Bus Exercisor (document) #MD-11-DZKCH-D

1.7 CZQRT RSX11M Test System (document) #AC-F153A-MC

2.0 REQUIRED TEST EQUIPMENT

2.1 PDP 11/34 or PDP 11/70 with minimum of 16K of memory, some type of disc load media, and one DD11-C SPC block.

2.2 SPC must be DD11-C.

2.3 SPC must provide +5, +15, and -15 volts.

2.4 Oscilliscope H475 or equivalent.

2.5 Digital volt meter

2.6 Multilayer Extender Module (M9048-Hex)

2.7 One 16 pin I.C. clip

2.8 Test Cable #7014152

2.9 Frequency counter may be required.

2.10 Some type of DPM terminal; such as a RT801, RT803, RT805, DPM01, VT110, or DPM50.

3.0 AVAILABLE DIAGNOSTIC PROGRAMS

3.1 Stand Alone Diagnostics Kit #ZJ-234-RB

Maindec	Description
CZKCC	Static Test, M8204 Data Path Test
CZKCD	Static Cram Branch Test (M8202)
CZKCA	Free Run, M8204 Data Path Test
CZKCE	Line Unit Test (M8202)
CZKCF	Bit Stuff Line Unit Test (M8202)
KMCA	DEC X-11 System Test

3.2 On-Line Diagnostics Kit #ZP-125-RD (Mag tape kit)

AP-F152A-MC	CZQRH RSX11M Test System Diagnostic

NOTE: The ZP-125-RD kit must be used to sys-gen a disc test pack before on-line diagnostics can be run.

4.0 INSTALLATION INSTRUCTIONS

4.1 M8204 Installation

4.1.1 The M8204 module should be installed in slot #2 of the DD11-C SPC block before installing. Remove the NPR Grant continuity wire that runs between pins CA1 and CB1 on the back plane for slot #2. If a system change requires removal of the M8204, this wire must be replaced.

4.1.2 The address and vectors for this module fall into the floating range, and a standard setup configuration is required.

ISB-11 #	Address	Vector
#1	160140	400
#2	160150	410
#3	160160	420
#4	160170	430

4.2 M8202 Installation

4.2.1 The M8202 module should be installed in Slot #3 of the DD11-C SPC block.

4.2.2 All switches on the module should be placed in the OFF position, for they are not used.

4.2.3 An ISB-11 Test Cable #7014152 should be fastened to the cable connector, attached to the module.

4.2.4 Some type of DPM terminal should be attached to the #7014152 test cable; such as a RT801, RT802, RT803, DPM01, VT110, or DPM50.

5.0 TEST SET UP

5.1 No special test set up is required, unless problems occur running diagnostics. If problems occur, refer to the maintenance manual for adjusting the line unit clock and read data one shot on the M8202 module.

6.0 POWER CHECKS

6.1 The ISB-11 utilizes 8 amperes of plus five volts per ISE. Care should be exercised that any test stand, or system installation considers the minimum current per regulator.

6.2 Voltage settings for the ISB-11 are very critical, and a Digital volt meter is recommended for making any adjustments. Test points, given below, for making adjustments should be taken on the module when making -15 volt adjustments on the 11/34's only. Set the -15 volts for exactly the same as the +15 volt reading, which is non-adjustable.

Voltage Test Points

Voltage	Module	Test Point
+15	M8202	+ side of C65
-15	M8202	- side of C64
+5	M8202	E 35 pin 16

6.3 Unibus Loading

The ISB-11 presents one DC and seven AC unibus loads to the system, A maximum of 20 AC loads are acceptable before separation by an M9202, or a 2 ft. bus cable is required.

The ISB-11 presents one DC and seven AC unibus loads to the system. A maximum of 20 AC loads are acceptable before separation by an M9202, or a 2ft. bus cable is required.

7.0 DIAGNOSTIC TEST PROCEDURE (STAND ALONE)

7.1 See Section 3.0 for order of diagnostics. The following procedure is used for all diagnostics.

7.1.1 Load diagnostic.

7.1.2 Load address at 200.

7.1.3 Set switch register to all zeros. Start program.

7.1.4 End of pass will be shown by type out.

7.1.5 No errors allowed.

8.0 DIAGNOSTIC TEST PROCEDURE (ON-LINE)

8.1 Host System Booting Procedure

8.1.1 Obtain a disk pack from the appropriate host media, which contains the RSX11M test system diagnostic package #ZP125-RD, and install it into Drive #0. Load Drive #0, and insure that "WRITE PROTECT" is off.

8.1.2 When Drive #0 is ready, and "ON LINE", boot the drive.

8.1.3 074036 000024 000652 001472

```
$DKO ----------------------------------TYPE: <DKO-RK05, DLO-
DEVICE DB00: NOT IN CONFIGURATION       RL01, DM0-RK06 or 07,
DEVICE DB01: NOT IN CONFIGURATION       DR0-RM02 or 03, DB0-
DEVICE DR00: NOT IN CONFIGURATION       RP04, 5, or 06>
DEVICE DR01: NOT IN CONFIGURATION
DEVICE MT00: NOT IN CONFIGURATION

RSX-11M V3.1  BL22  64K  MAPPED
>RED DK0:=SY0:
>RED DK0:=LB0:
>MOU DK0:SYSTEM
>@C1, 2]STARTUP
>* PLEASE ENTER TIME AND DATE (HR:MN DD-MMM-YY) [S]:
08:30 10-DEC-79  ----------------TYPE: <08:30 10-DEC-79>
```

```
>TIM 08:30  10-DEC-79
>INS  $ISBRPT
>INS  $ISBERR
>INS  $ISBOWL
>INS  $ISBINI
>INS  [7,7]FDCTIM
>FIX  FDCTIM
>LOA  SB:/PAR=GEN
>RUN  FDCTIM  M/RSI=20S
>INS  $PIP
>INS  $FLX
>* DO YOU WANT TO LOAD IPG DIAGNOSTICS
FROM MAGTAPE? [Y/N]:N----------TYPE: (N)
>@ <EOF>
>SET /UIC=[200,270]----------TYPE: <SET /UIC=[200,270]>
```

8.2 Run the error report task in order to clear out the error log.

8.2.1
```
>RUN ISBRPT ----------TYPE: <RUN ISBRPT>
ISBRPT - DEC DATAWAY ERROR REPORT TASK
>
PRINT SUMMARY [Y OR N]? N ----------TYPE: <N>
PRINT ENTIRE FILE [Y OR N]? N ----------TYPE: <N>
DELETE ERROR FILE [Y OR N]? Y ----------TYPE: <Y>
ISBRPT . . . OPERATION COMPLETE
```

8.3 Run the ISB11 DEC Dataway Diagnostic Exercisor.

8.3.1
```
RUN DZKCH ----------TYPE: <RUN DZKCH>
DCP-A>STA ----------TYPE: <STA>
# UNITS (D)  ? 1 ----------TYPE: <1>
UNIT 1 ----------TYPE: <1>
ENTER CONTROLLER NUMBER: (0) 0 ? 0 ----------TYPE: <0>
ENTER TERMINALS ON THAT CONTROLLER: (0) 1 ? 1 -----TYPE: <1>

NUMBER OF ENTERED TERMINALS = 1
UNIT ** CONTROLLER ** LOGICAL SB ** LUN **
001      000            001          011
```

8.4 After a complete run, the diagnostic must be terminated with a carriage return ----------TYPE: <CR>

```
TASK "TTO    " TERMINATED
TASK EXIT WITH OUTSTANDING IO
  PC = 046000
  PS = 170000
  R0 = 000002
  R1 = 000000
  R2 = 000000
  R3 = 000000
  R4 = 000003
  R5 = 000001
  SP = 001246
```

8.5 After a complete run, the error log must be checked to make sure there are no errors reported.

```
8.5.1 >RUN ISBRPT ----------TYPE: <RUN ISBRPT>
       ISBRPT - DEC DATAWAY ERROR REPORT TASK
      >
       PRINT SUMMARY [Y OR NO]? Y ----------TYPE: <Y>
       PRINT ENTIRE FILE [Y OR N]? N ----------TYPE: <N>
       OUTPUT TO LINE PRINTER [Y OR N]? N ----------TYPE:<N>
       WANT ONE CONTROLLER [Y OR N]? N ----------TYPE:<N>
       DELETE ERROR FILE [Y OR N]? N ----------TYPE:<N>
       ISBRPT . . . ERROR FILE IS EMPTY
       ISBRPT . . . OPERATION COMPLETE

       MCR>
```

8.6 Error reporting can be in the form of hard errors, typed out immediately, or soft errors; errors that are logged by the error logger. No errors are allowed.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE 20 June 80

TITLE DPM50 DISTRIBUTED I/O SUBSYSTEM

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	Updated and revised	MA-A0000 ML010		20/06/80		

ENG	APPD	SIZE	CODE	NUMBER	REV
BILL WHITBY	STU ESTES	A	SP	MAA 6176-0-0	C

DPM-50 DISTRIBUTED I/O SUBSYSTEM

1.0 INTRODUCTION:

The DPM-50 distributed systems are based on single boxed configurations of either the KD11-H LSI-11 microcomputer or the KDF11-AA (11/23) microcomputer,power supply,process I/O modules and DEC DATAWAY interface. The purpose is to provide process I/O for the LSI-11 and thereby offer low cost distributed intelligent systems fully supported by software. The KDF11-AA configuration offers in addition PDP-11/34 functionality on the LSI-11 bus, memory management as a standard feature and optional floating point option(KEF11-A).

2.0 REFERENCE DOCUMENTATION:

2.1 MANUALS:

2.1.1 MICROCOMPUTER HANDBOOK: EB 15836-18/79
2.1.2 MSV11-D,-E USERS MANUAL: EK MSV1D-OP-???
2.1.3 PROCESS I/O SUBSYSTEM USERS GUIDE: EK-PIOS-UG-???
2.1.4 DPM50 USERS GUIDE: EK-DPM50-UG-???
2.1.5 KDF11-AA USERS GUIDE: EK-KDF11-UG-???
2.1.6 MICROCOMPUTER INTERFACES HANDBOOK EB-17723-20/80

2.2 PRINTS AND SCHEMATICS:

2.2.1 H333 PRINT SET: MP00424
2.2.2 ISV11-A PRINT SET: MP00609
2.2.3 TEV11 PRINT SET: MP00074
2.2.4 KD11-S PRINT SET: MP00433
2.2.5 DLV11-F PRINT SET: MP00461
2.2.6 KDF11-AA PRINT SET MP00734
2.2.7 MSV11-D PRINT SET: MP00566

3.0 REQUIRED TEST EQUIPMENT:

3.1 HARDWARE AND MEDIA:

3.1.1 Valid DPM host system configuration.
3.1.2 RSX11-M on appropriate media.
3.1.3 Attenuation panel.
3.1.4 HEWLETT PACKARD DVM or equivalent, accurate to .01V @ 15V.
3.1.5 Serial line unit IE. DLV11-F and terminal for LSI error information output (local).

4.0 REQUIRED DIAGNOSTIC PROGRAMS:

4.1 DPM50 Diagnostics Kit #ZP125-RD

	NAME	DESCRIPTION	MODE
4.1.1	DZKCI	Remote Terminal Tester	Remote
4.1.2	DZKCH	Serial Bus Exerciser	Remote
4.1.3	CZKMP	Task Handler	N/A
4.1.4	DVKAA	Basic Instruction Test	Local&Remote
4.1.5	DVKAB	EIS Instruction Test	Local&Remote
4.1.6	DVKAC	FIS Instruction Test	Local&Remote
4.1.7	DVKAD	LSI-11 Traps Test	Local&Remote
4.1.8	DVDVC	DLV11-F Test	Local&Remote
4.1.9	DVKAH	4K System Exerciser	Local
4.1.10	CZQMC	0-124K Memory Exerciser	Local&Remote
4.1.11	DVPCA	PCS Test	Local&Remote
4.1.12	CJKDA	F-11 MMU Test	Local&Remote
4.1.13	CJKDB	F-11 CPU Test	Local&Remote
4.1.14	CVDLA	DLV11-J Test	Local&Remote
4.1.15	CJKDC	KEF11-AA Diag 1	Local&Remote
4.1.16	CJKDD	KEF11-AA Diag 2	Local&Remote
4.1.17	CZKMA	0-124K Memory Exerciser	Local&remote

5.0 SPECIAL INSTRUCTIONS:

5.1.1 RSX11-M must be running in the host system with DPM50 diagnostics kit #ZP125-RD.

5.1.2 Due to power supply limitations, only two of the below supported options can be installed at any one time in F and H variations of the DPM50. Since a terminal interface is required to run diagnostics in local mode one of the two options must be the DLV11-F or DLV11-J

A. DLV11-F
B. DLV11-J/DLV11-KA
C. DZV11-B
D. MSV11-D
E. RXV11 or RXV21 *

* Floppy disk options not supported by a local boot.

6.0 INSTALLATION AND TEST SETUP INSTRUCTIONS:

6.1 UNPACKING AND INSPECTION:

6.1.1 Save all packing material for equipment to be shipped that is not cab mounted.

6.2 MODULE CONFIGURATION SETUPS FOR DPM50

6.2.1 KD11-H(M7264) LSI CPU MODULE

JUMPER DESIGNATION	JUMPER STATE
W1	OUT
W2	OUT
W3	OUT
W4	IN
W5	OUT
W6	OUT
W7	IN
W8	IN
W9	IN
W10	OUT
W11	OUT

The KEV11A EIS/FIS chip is installed in location E75 on M7264 LSI CPU module. Refer to Figure 1.

6.2.2 KDF11-AA(M8186) LSI 11/23 CPU module (DPM50 F/H variations only).

JUMPER DESIGNATION	JUMPER STATE
W1	IN
W2	AS RECEIVED
W3	AS RECEIVED
W4	OUT
W5	OUT
W6	OUT
W7	IN
W8 THRU W15	DON'T CARE
W16	IN
W17	IN
W18	IN

Reference Figure 2 for jumper locations.

6.2.3 MSV11-DD(M8044-D?) FIRST 32K

S1 SWITCHPACK	SWITCH STATE
SW1	ON
SW2	ON
SW3	ON
SW4	ON
W2	IN
W3	IN
PIN 4 TO 3	IN
PIN 5 TO 7	IN
PIN 10 TO 14	IN
PIN 15 TO 16	IN

Reference Figure 4 for switch and jumper locations.

6.2.4 DLV11-F(M8028) SERIAL LINE UNIT

JUMPER DESIGNATION	JUMPER STATE
T0	OUT
T1	IN
T2	OUT
T3	IN
R0	OUT
R1	IN
R2	OUT
R3	IN

The DLV11-F is default jumpered for console use,but the baud rate jumpers must be reconfigured from 180 baud operation to 300 baud.

The DLV11-F is not a standard part of the DPM50 system, but is a frequent option. See Figure 9 for jumper locations.

6.2.5 ISV11-A (M8080,5413290) SERIAL BUS INTERFACE

FACTORY CONFIGURED:

CSR ADDRESS	160140
	160142
	160144
VECTOR ADDRESS	300
	304

JUMPERS	STATE	LOCATION
W1 THRU W6	OUT	M8080
W7 THRU W10	IN	M8080
W11 THRU W16	OUT	M8080
W17 THRU W20	IN	M8080
W21 THRU W23	OUT	M8080
W1,W3,W5,W7,W9	IN	5413290
W2,W4,W6,W8,W10	OUT	5413290

See Figures 7.1 and 7.2 for jumper locations.

If DLV11-J installed default starting vector address of 300 must be reconfigured because of its conflict with the ISV11-A.

6.2.6 I/O CONTROL MODULE(M7958)

CSR ADDRESS	171000
VECTOR ADDRESS	234

VECTOR SWITCH PACK E7	SWITCH STATE
SW1	ON
SW2	ON
SW3	ON
SW4	OFF
SW5	OFF
SW6	ON
SW7	OFF
SW8	OFF

ADDRESS SWITCH PACK E34	SWITCH STATE
SW1	OFF
SW2	ON
SW3	OFF
SW4	OFF
SW5	ON
SW6	OFF
SW7	OFF
SW8	ON

Reference Figure 8 for switchpack locations.

6.2.7 TEV11(M9400-YB) TERMINATOR MODULE

JUMPER DESIGNATION	JUMPER STATE
W1	IN
W2	OUT
W3	IN
W4	OUT

Reference Figure 3 for jumper locations.

6.3 CABLING OF THE DPM50

6.3.1 Cabling of the DPM50 consists of a serial bus cable (70-15928-03) coming from the daughter board (54-13290) of the ISV11-A mother/daughter pair,which interconnects with the DEC DATAWAY cable (70-14152),which in turn is run through an attenuation panel to simulate cable length,finally exiting the attenuation panel and connecting to the host CPU'S ISB11. See Figures 5,7.2 and 10.

Attenuation panel is only used for test and is not shipped with the system.

DEC DATAWAY is keyed.

7.0 POWER CHECKS

7.1 +5.1VDC +.1-.15
+12VDC +.1-.36

If voltages are out of tolerance remove the H7870 power supply cover and slide the power supply out until access to the adjustments is possible. Reference Figure 6.

8.0 DIAGNOSTIC TEST PROCEDURE

The host processor,whether it be an 11/70 or 11/34 along with its ISB11'S must be fully checked out according to MAST prior to connecting a DPM50 to the DATAWAY.

8.1 DPM50 HOST SYSTEM BOOTING PROCEDURE

8.1.1 Obtain a disk pack for the appropriate host media which has the RSX11-M host package #AP-F152A-MC and install it into DRIVE #0. Load DRIVE #0 and insure that "WRITE PROTECT" is off.

8.1.2 When DRIVE #0 is ready and "ON LINE" (heads loaded) BOOT the drive.

8.1.3 When the program asks for the date and time, you may either enter the information or default it by typing a carriage return. An example would be 08:30 04-JUN-80.

8.1.4 The program will continue setting up parameters and will ask: "Do you want to load IPG diagnostics from magtape [Y/N]:". Type in a carriage return which will default your answer to a NO condition.

8.1.5 The program will now output:
>@ <EOF> (This signifies end of file and parameters are now set) and waits for you to key in a command.

8.1.6 Type in:
Set /UIC=[200,270] (This may not be necessary if the UIC is already at 200,270.)

8.2 RUN THE ERROR REPORT TASK IN ORDER TO CLEAR OUT THE ERROR LOG

8.2.1 >RUN ISBRPT----------TYPE:<RUN ISBRPT>
```
ISBRPT-DEC DATAWAY ERROR REPORT TASK
>
PRINT SUMMARY [Y OR N]?N------------TYPE:<N>
PRINT ENTIRE FILE [Y OR N]?N--------TYPE:<N>
DELETE ERROR FILE [Y OR N]?Y--------TYPE:<Y>
ISBRPT...OPERATION COMPLETE
TASK "ISBRPT" TERMINATED
TASK EXIT WITH OUTSTANDING I/O
PC=125130
PS=170000
R0=120720
R1=125576
R2=125650
R3=000000
R4=143470
R5=000000
SP=120476
```

8.2.2 Type:CTRL C to terminate ISBRPT task and receive back MCR> prompt.

8.3 RUN THE DEC DATAWAY DIAGNOSTIC EXERCISER.

```
8.3.1 >RUN DZKCH----------------------------TYPE:<RUN DZKCH>
      DCP-A>STA-----------------------------TYPE:<STA>

      #UNITS (D)?1--------------------------TYPE:<1>
      ENTER CONTROLLER NUMBER:(O)0?0-------TYPE:<0>
      ENTER TERMINALS ON THAT CONTROLLER:
      (O)1?1--------------------------------TYPE:<1>
      NUMBER OF ENTERED TERMINALS=1

      UNIT**CONTROLLER**LOGICAL SB**LUN**
       001       000           001       011

      TOTAL ACTIVE PASSES = 21,ACTIVE TERMINALS=1, TIME=8:33

      TOTAL ACTIVE PASSES = 41,ACTIVE TERMINALS=1, TIME=8:34
```

8.3.2 After required run time has elapsed terminate running of diagnostic by typing CTRL C.

```
      TASK "TTO" TERMINATED
      TASK EXIT WITH OUTSTANDING I/O
      PC=046000
      PS=170000
      R0=000002
      R1=000000
      R2=000000
      R3=000000
      R4=000003
      R5=000001
      SP=001246
```

8.4 After DZKCH has run,The error log must be checked for errors that may have occured during running.

```
8.4.1 >RUN ISBRPT--------------------------TYPE:<RUN ISBRPT>
      ISBRPT-DECDATAWAY ERROR REPORT TASK
      >
      PRINT SUMMARY[Y OR N]?Y--------------TYPE:<Y>
      PRINT ENTIRE FILE [Y OR N]?N---------TYPE:<N>
      OUTPUT TO LINE PRINTER [Y OR N]?N----TYPE:<N>
      WANT ONE CONTROLLER [Y OR N]?N-------TYPE:<N>
      DELETE ERROR FILE [Y OR N]?N---------TYPE:<N>
      ISBRPT...ERROR FILE IS EMPTY
      ISBRPT...OPERATION COMPLETE
```

8.4.2 Type: CTRL C to terminate ISBRPT task and receive back MCR> prompt.

8.4.3 Error reporting can be in the form of hard errors, typed out immediately, or soft errors; Errors that are logged by the error logger. No errors are allowed.

8.5 RUN ROM RESIDENT TEST3 OF ISV11-A

8.5.1
```
MCR>RUN CZKCIB----------------------TYPE:<RUN CZKCIB>
>
DCP-A>STA---------------------------TYPE:<STA>

# UNITS (D) ? 1-----------------------TYPE:<1>

UNIT 1
ENTER CONTROLLER NUMBER:(0)0?0------TYPE:<0>
ENTER TERMINALS ON THAT CONTROLLER:
(D)1?1------------------------------TYPE:<1>

SELECTED SERIAL LINE PORTS

UNIT**CONTROLLER**LOGICAL SB**LUN**TYPE
  1         0           001       9   DPM50-PORT 0

START OF TESTING

END OF PASS     0,   TIME = 9:29

END OF PASS     1,   TIME = 9:31
```

8.5.2 After required run time has elapsed terminate running of the diagnostic by typing CTRL C.

8.6 LOAD DIAGNOSTIC MONITOR CZKMPB

8.6.1
```
>RUN CZKMPB-------------------------TYPE:<RUN CZKMPB>
>
CZKMPB VERSION 2.2
SELECT MODE: LOCAL, HOST, AUTO-MAP, COMMUNICATION OR EXIT
(L,H,A,C,E)L------------------------TYPE:<L>
ENTER NUMBER OF TERMINALS [D]=1-----TYPE:<1>
ENTER CONTROLLER NUMBER [0]=0-------TYPE:<0>
ENTER TERMINAL NUMBERS [0]=1--------TYPE:<1>
NUMBER OF ENTERED TERMINALS = 1
UNIT**CONTROLLER**LOGICAL SB**
  1         0           1
```

At this point the console terminal at the DPM50 subsystem comes on line and is used to ask for and run subsystem diagnostics.

If DPM50 contains an 11/23 CPU (KDF11-AA), proceed to section 8.8 otherwise go to section 8.7.

8.7 RUN 11/03 (KD11-H) BASED DPM50 LSI DIAGNOSTICS

See Figure 11 for explanation of monitor interaction at DPM50 local terminal.

LTC switch must be in the off position to run diagnostics.

8.7.1
```
>VKAACO----------------------------TYPE:<VKAACO>
157776
@200G------------------------------TYPE:<200G>
END PASS
END PASS
```

8.7.2 After required run time has elapsed, terminate running of the diagnostic by depressing the break key on the DPM50 console terminal.

8.7.3
```
@760144/000000 2--------------------TYPE:<760144/>
                                    TYPE:<2>
>VKABA0----------------------------TYPE:<VKABA0>
157776
@200G------------------------------TYPE:<200G>
END PASS
END PASS
```

8.7.4 After required run time has elapsed, terminate running of the diagnostic by depressing the break key on the DPM50 console terminal.

8.7.5
```
@760144/000000 2--------------------TYPE:<760144/>
                                    TYPE:<2>
>VKACC1----------------------------TYPE:<VKACC1>
157776
@200G------------------------------TYPE:<200G>
DVKACC-LSI-11 FIS INSTRUCTION TEST
END PASS
END PASS
```

8.7.6 After required run time has elapsed, terminate running of the diagnostic by depressing the break key on the DPM50 console terminal.

```
8.7.7 @760144/000000 2----------------------TYPE:<760144/>
                                             TYPE:<2>
      >VKADC0--------------------------------TYPE:<VKADC0>
      157776
      @200G----------------------------------TYPE:<200G>
      CVKADC0 LSI-11 TRAPS TEST

      EIS/FIS OPTION PRESENT
      DIBOL INSTRUCTION SET NOT PRESENT
      END OF PASS
```

8.7.8 After required run time has elapsed, terminate running of the diagnostic by depressing the break key on the DPM50 console terminal.

```
8.7.9 @760144/000000 2----------------------TYPE:<760144/>
                                             TYPE:<2>
      >ZKMAF0--------------------------------TYPE:<ZKMAF0>
      157776
      @200G----------------------------------TYPE:<200G>
      CZKMAF0
      000000-157776
      TST 13 BNK  00
      TST 13 BNK  01
      TST 13 BNK  02
      TST 13 BNK  03
      TST 13 BNK  04
      TST 13 BNK  05
      TST 13 BNK  06
      RELOC
      TST 13 BNK  00
      PASS# 01
```

8.7.10 After required run time has elapsed,terminate running of the diagnostic by depresaing the break key on the DPM50 console terminal.

8.7.11 Load and run diagnostics for any additional LSI option modules added to the base DPM50 system, using same method used to run CPU tests.

8.7.12 After all LSI modules have been run, if any D Bus I/O modules exist, load in diagnostic VPCAE0 from the host processor and follow procedure P00-00C0A-00-000-WM-06-8055. Reference section 4.0 DIAGNOSTIC TESTING

8.8 RUN 11/23(KDF11-AA) BASED DPM50 DIAGNOSTICS

See Figure 11 for explanation of monitor interaction inputs and outputs at local DPM50 terminal.

LTC switch must be in OFF position to run diagnostics.

8.8.1
```
>JKDAC0------------------------------TYPE:<JKDAC0>
157776
@200G--------------------------------TYPE:<200G>
CJKDAC0 KTF11-AA MMU DIAG.
SWR=000000 NEW=CR--------------------TYPE:<CR>

END PASS#   1  ;TOTAL ERRORS SINCE LAST START AT 200   0
```

8.8.2 After required run time has elapsed, terminate running of the diagnostic at the DPM50 console terminal by depressing the break key.

8.8.3
```
@760144/000000 2---------------------TYPE:<760144/>
                                      TYPE:<2>
>JKDBC0------------------------------TYPE:<JKDBC0>
157776
@200G--------------------------------TYPE:<200G>
CJKDBC0 DCF11-AA CPU DIAGNOSTIC
END PASS#  1
END PASS#  15
```

8.8.4 After required run time has elapsed,terminate running the diagnostic at the DPM50 console terminal by depressing the break key.

8.8.5
```
@760144/000000 2---------------------TYPE:<760144/>
                                      TYPE:<2>
>ZQMCG0------------------------------TYPE:<ZQMCG0>
157776
@200G--------------------------------TYPE:<200G>
SWR=000000 NEW= CR-------------------TYPE:<CR>

KT11(MEMORY MANAGEMENT)AVAILABLE

MEMORY MAP
FROM 000000 TO 757777 (WITH 4 MSV11-D INSTALLED)
NO PARITY REGISTERS FOUND
PROGRAM RELOCATED TO 720000
PROGRAM RELOCATED TO 000000
END PASS# 1
```

Above will be received when 4 MSV11-D modules are installed, typeouts will vary with lesser amounts of memory. No relocation will occur when only 1 MSV11-D installed.

8.8.6 *NOTE THE following two tests are to be run if the optional KEF11 chip is installed.

8.8.7 @760144/000000 2----------TYPE:<760144/>
TYPE:<2>
>JKDCB0----------TYPE:<JKDCB0>
157776
@200G----------TYPE:<200G>
CJKDCB, KEF11-A FP DIAGNOSTIC PART 1

SWR = 000000 NEW=CR----------TYPE:<CR>

END PASS # 1
END PASS # 2

8.8.8 After required run time has elapsed, terminate running of the diagnostic at the DPM50 console terminal by depressing the break key.

8.8.9 @760144/000000 2----------TYPE:<760144/>
TYPE:<2>
>JKDDB0----------TYPE:<JKDDB0>
157776
@200G----------TYPE:<200G>
CJKDDB KEF11-A DIAGNOSTIC PART 2

SWR = 000000 NEW =CR----------TYPE:<CR>

END PASS # 1
END PASS # 2

8.8.10 After required run time has elapsed, terminate running of the diagnostic at the DPM50 console terminal by depressing the break key.

8.8.11 Load and run diagnostics for any additional LSI option modules installed, using same method used to run the CPU tests.

8.8.12 after all LSI modules have been run, if any D BUS I/O modules exist within the DPM50 subsystem, load diagnostic VPCAE0 and follow procedure P00-00C0A-00-0000WM-06-8055. Reference section 4.0 DIAGNOSTIC TESTING.

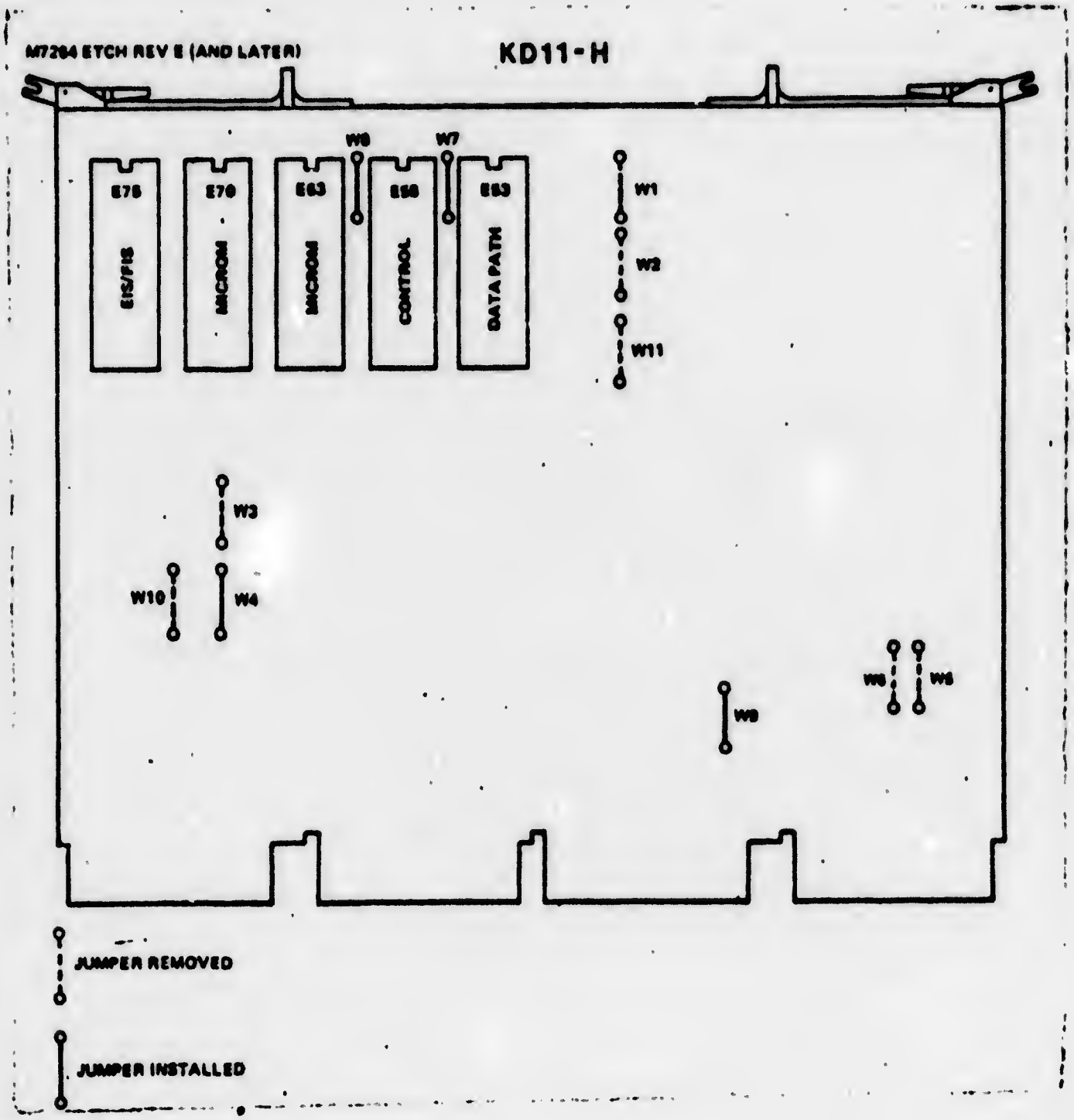
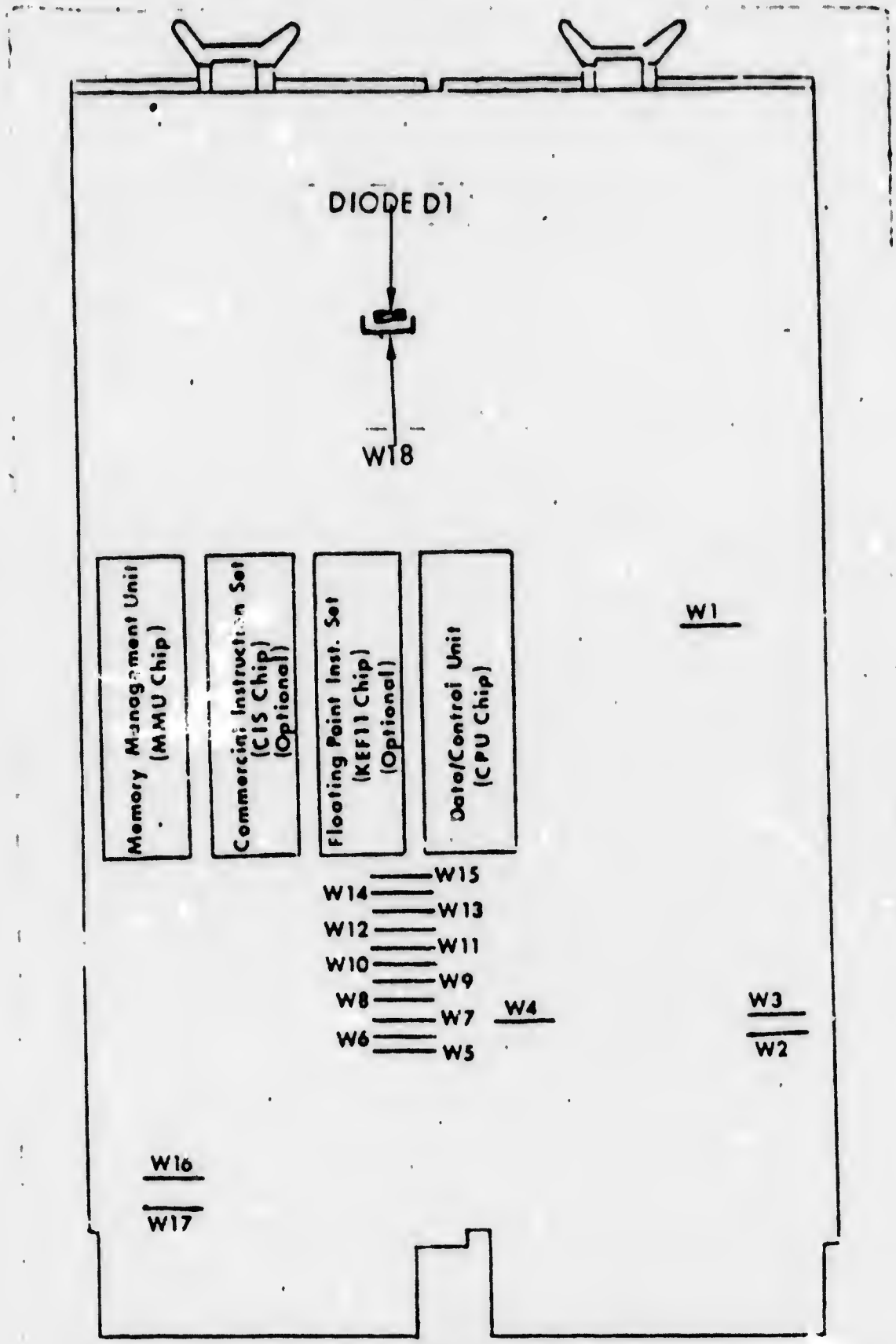


FIGURE 1

	SIZE	CODE	NUMBER	REV
	A	SP	MAA 6176-0-0	C



KDF11-AA

(M8186 DUAL SIZE MODULE)

FIGURE 2

TEV11 M9400-YB

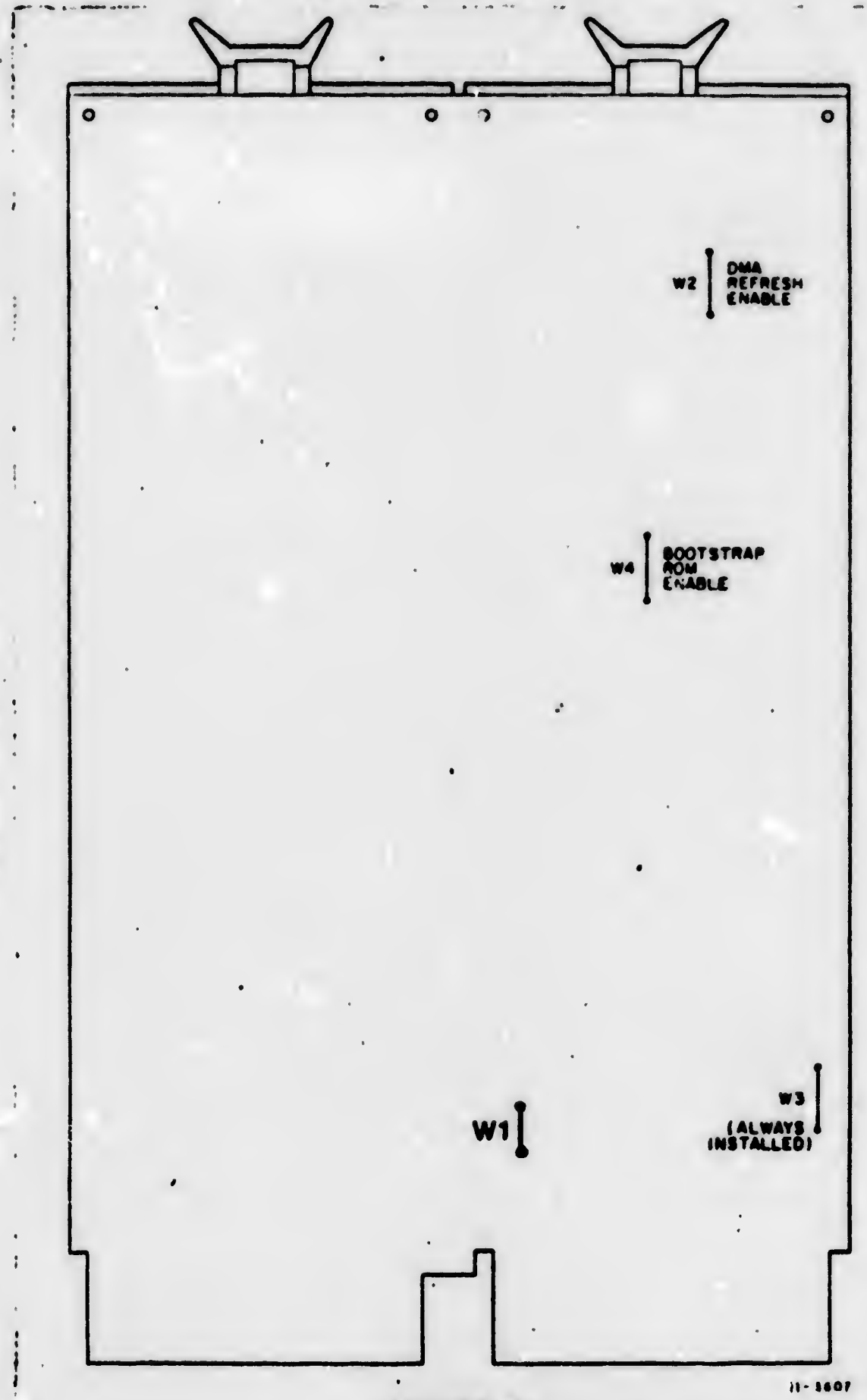


FIGURE 3

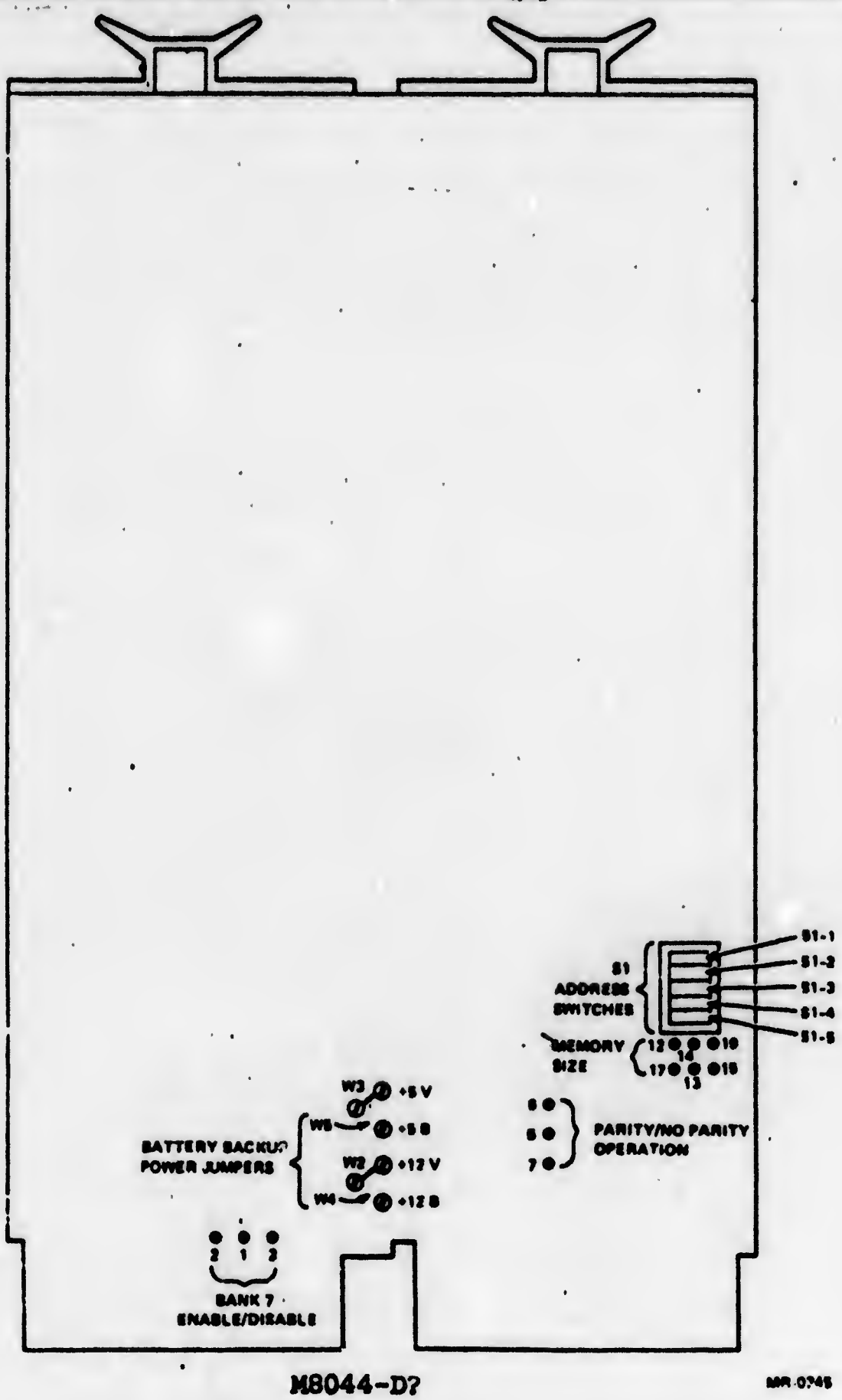


Figure 4 MSV11-D, MSV11-E Switch and Jumper Locations

	SIZE	CODE	NUMBER	REV
	A	SP	MAA 6176-0-0	C

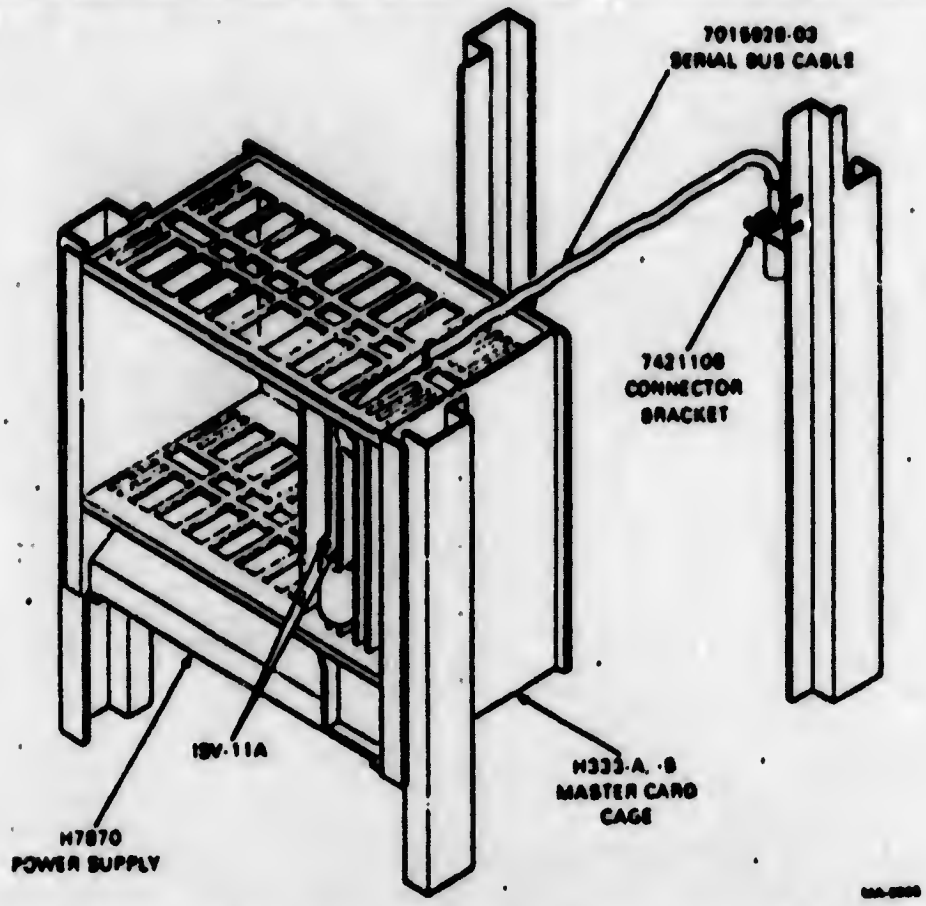


Figure 5 DECdataway Connector Mounting

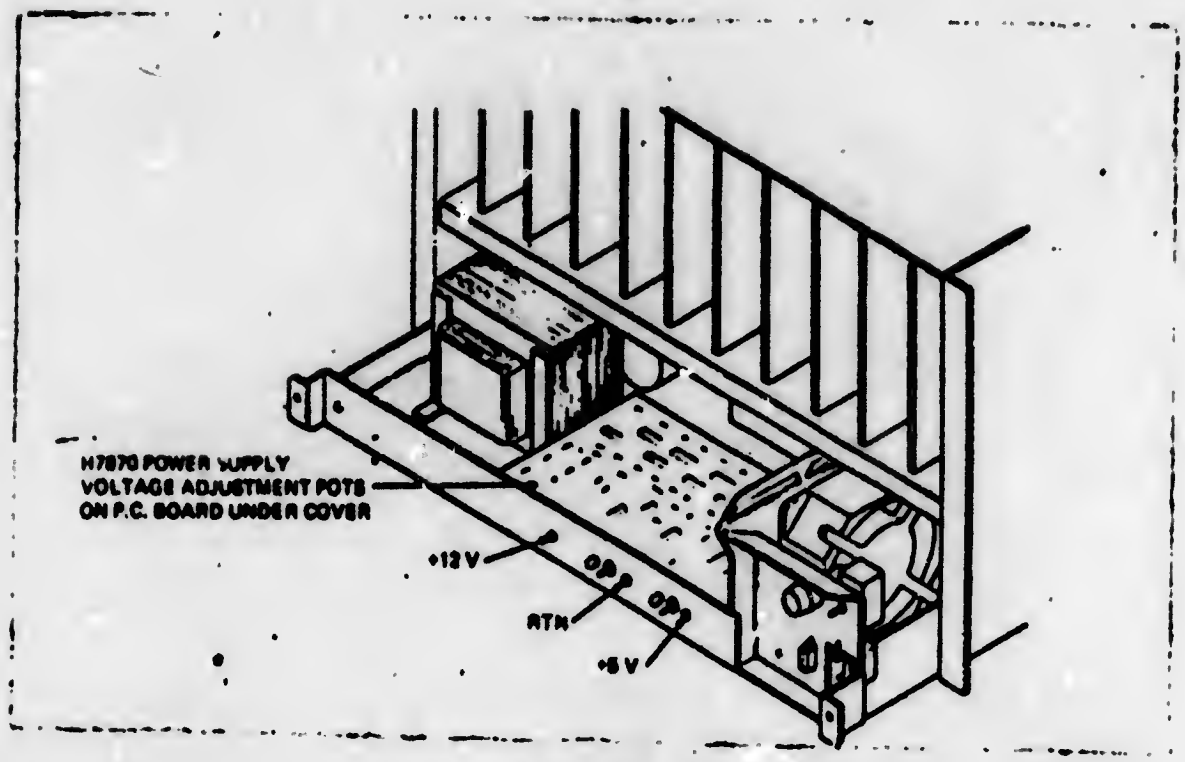


FIGURE 6

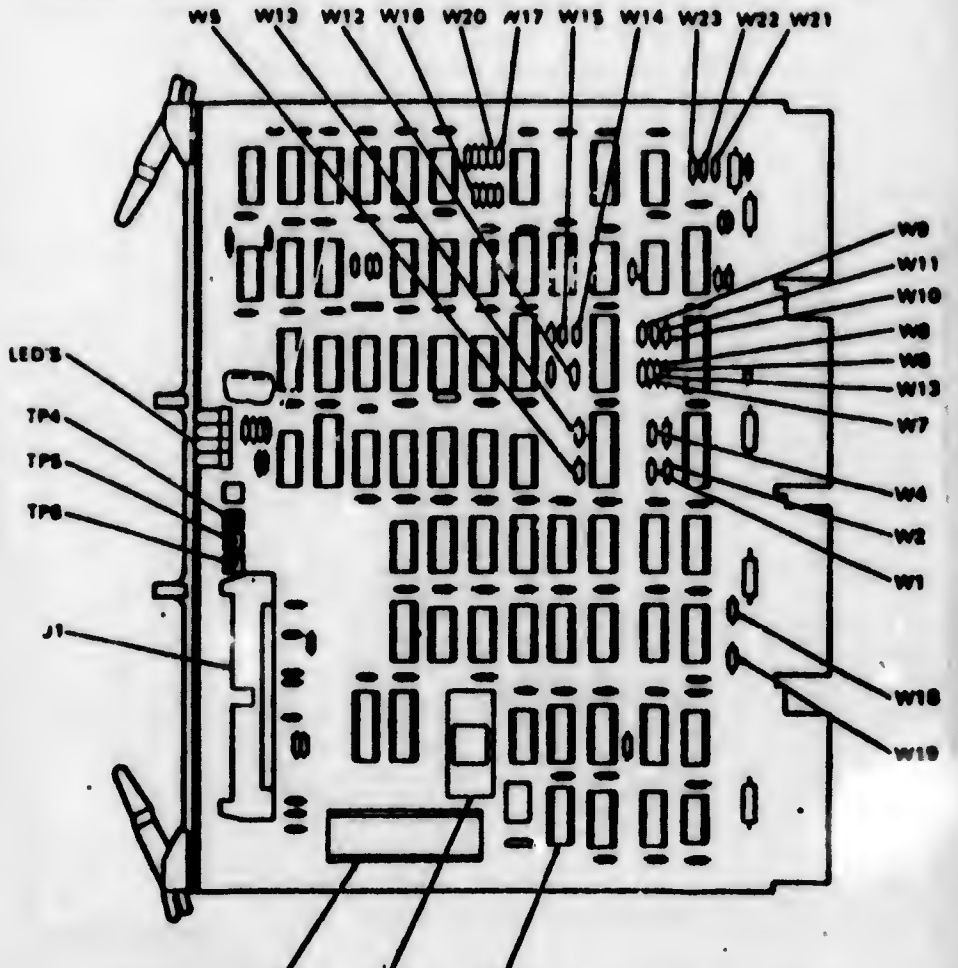


Figure 7-1 M8080 Board

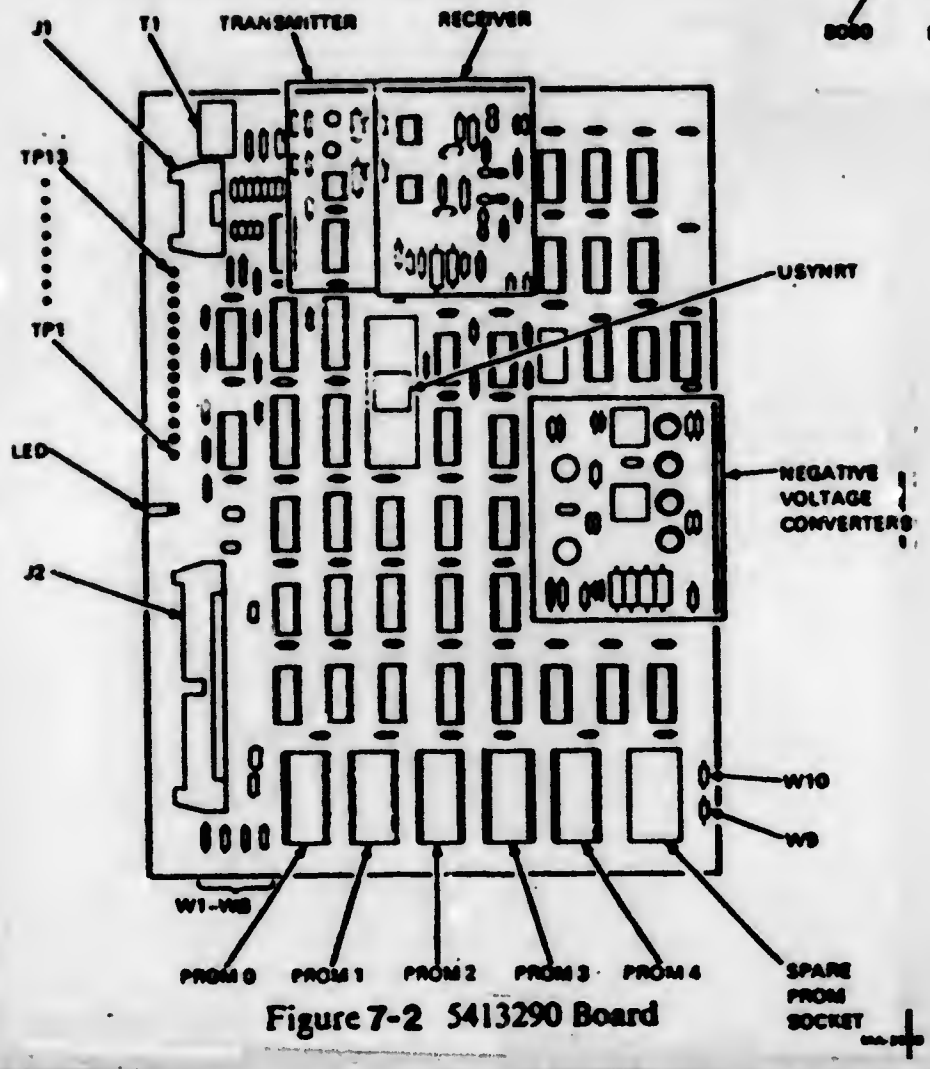


Figure 7-2 5413290 Board

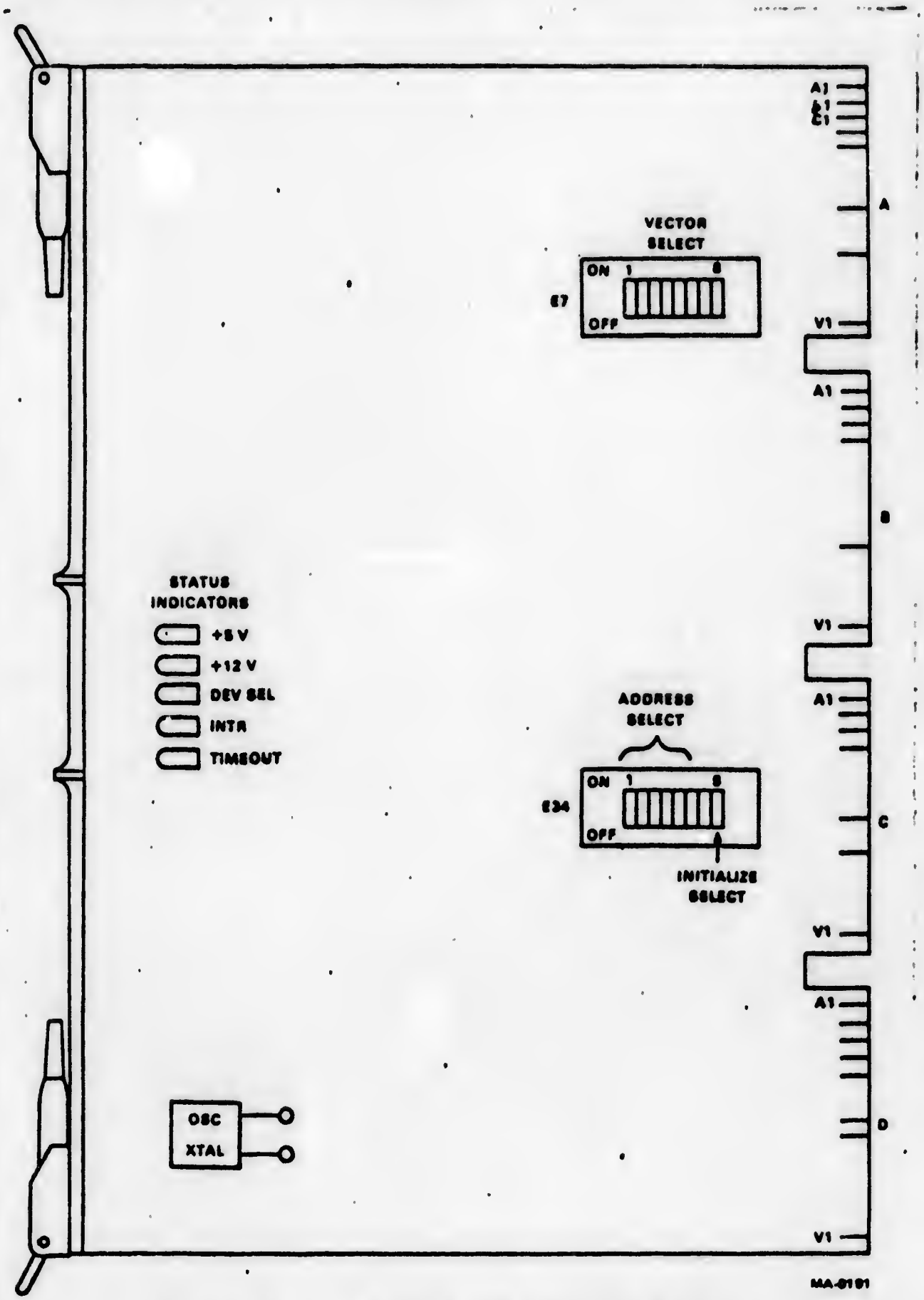


Figure 8 M7958 I/O Control Module

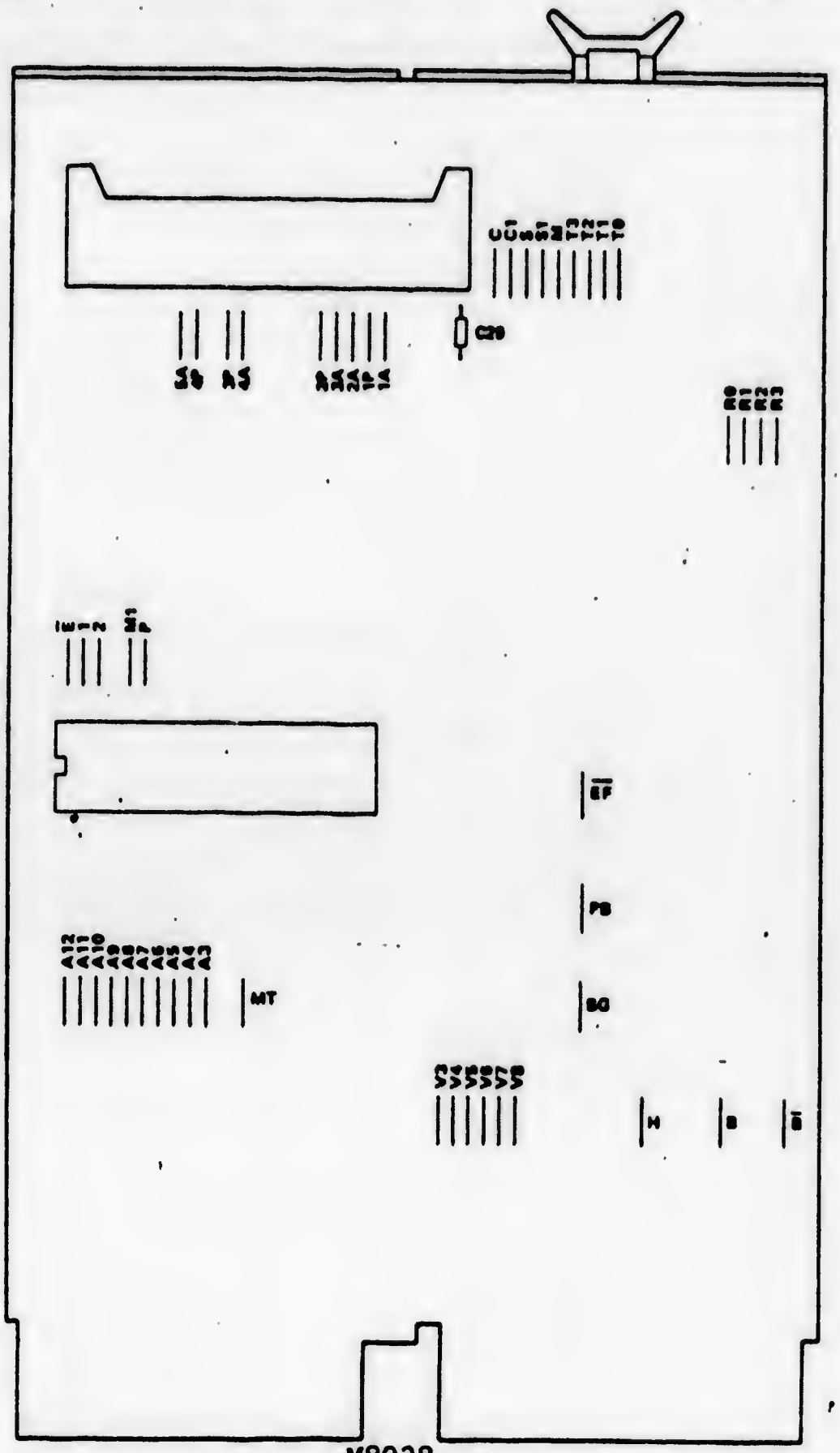
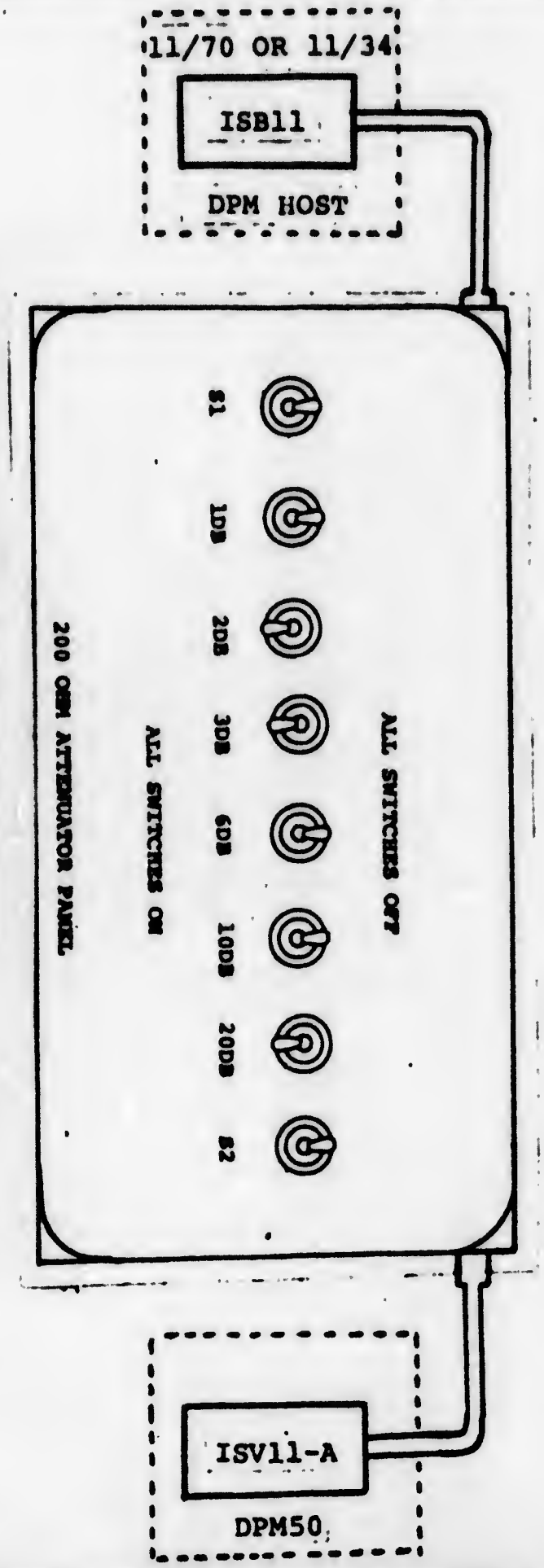


Figure 9 DLV11-F Jumper Locations



# OF TERMINALS	ATTENUATOR SETTING
1 TO 9	25DB
10 TO 19	24DB
20 TO 29	23DB
30 TO 39	22DB
40 TO 49	21DB
50 TO 59	20DB
60 TO 63	19DB

FIGURE 10

MONITOR INTERACTION AT LOCAL TERMINAL

	Prompts	
	>	Operator may enter file name to call next diagnostic, or type control Z to put LSI-11 in ODT mode.
	@	If following 157776 after a file name has been entered, indicates the diagnostic is in the LSI-11 and the operator may communicate with it via ODT. If following "End pass" and the current PC, indicates the operator may give further instructions in ODT. Giving "760144" reestablishes communication with local monitor.
	Inputs	
	File names	Used following ">" to call diagnostics.
	200G	Not to monitor - starts diagnostic if LSI-11 is in ODT.
	Break	Not to monitor - stops diagnostic.
	760144/	Reestablishes communication with local monitor if LSI-11 is in ODT.
Deposit	2	Following "000000" tells monitor that operator wishes to run another diagnostic.
Deposit	1	Follow "000000" aborts monitor in host. This is the last input by the operator.
	Control Z	Following ">" puts LSI-11 in ODT.
	Outputs	
	157776	Following file name entry indicates the diagnostic has been downloaded.
	NX	The requested file cannot be found.
	BDLD	The attempt to download the diagnostic was unsuccessful.
	END PASS	Diagnostic has completed a pass.
	Current PC	Following break indicates diagnostic has stopped at address printed.
	000000	Following "760144" indicates operator may input further instructions to local monitor (1 or 2).
	EX	Monitor has terminated at host.

FIGURE 11

A6180

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AR11 SYSTEM INSTALLATION AND ACCEPTANCE PROCEDURE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6180					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Sobieniowski	Tom Feller	A	SP	MAA6180-0-0	A

AR11 SYSTEM INSTALLATION AND ACCEPTANCE PROCEDURE

1.0 AR11 INSTALLATION/ACCEPTANCE

Refer to Document A-SP-AR11-0-4

1.1 Diagnostic Package

(A) AR11 Logic Test MainDEC-11-DZARA-A
(B) AR11 Analog Tests MainDEC-11-DZARB-A
(C) AR11 Wrap-Around Test MainDEC-11-DZARC-A

1.2 Error Diagnosis and Repair

Refer to Document A-SP-AR11-0-6

1.3 Other Related Documents

(A) AR11 Circuit Description A-SP-AR11-0-5
(B) AR11 Users Guide DEC-11-HARU6-B-D

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE NC 11-A GAMMA CAMERA INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6190					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jeleniewski	Tom	A	SP	MAA6190-0-0	A

NC 11-A GAMMA CAMERA INTERFACE

Ref. Adjustment Procedure A-SP-NC11-A-23

Checkout and Acceptance A-SP-NC11-A-22


A6192

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE NCV11 GAMMA CAMERA INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A						

ENG	APPD	SIZE	CODE	NUMBER	REV
Dwayne Herbert	Tom DeLaurenti	A	SP	MAA6192-0-0	A

EN-01063-16-01672-(202)

NCV11 GAMMA CAMERA INTERFACE

1.0 INTRODUCTION:

The Gamma Camera is used to record the distribution of radioactive isotopes that are introduced into a patient under study and concentrated in the organ of interest. The output of the Gamma camera is processed by the NCV11 interface, loaded into a computer memory, and written on a mass storage device. The stored information may be called back and displayed at a later date.

2.0 REFERENCE DOCUMENTATION:

2.1 Reference Manual EK-NCV11-TM-???

2.2 Reference Parts List PL-NCV11

2.3 Checkout Procedure SP-NCV11-0-10

2.4 Print Set MP00491

3.0 TEST EQUIPMENT:

3.1 Test philosophy will be to module swap and return for repair.

3.2 The Self Test connector (Part No. 70-12894) is the only special equipment required to run these tests. The connector is shipped with the NCV11 option. You may find it plugged into J1 on the A017 module.

3.3 Add DVM - Voltmeter.

4.0 REQUIRED DIAGNOSTIC PROGRAMS:

4.1 DVNCA NCV11 Logic Test

4.2 DVNCA NCV11 Differential Linearity Test

5.0 SPECIAL INSTRUCTIONS:

None

6.0 INSTALLATION & TEST SET UP INSTRUCTIONS:

Unibus Based Systems - When making an add-on installation of the NCV11-B Interface Option to an existing Unibus-based system, proceed as follows:

6.1 Mount the DDV11-C backplane in the CPU or expander box in the same manner as a standard Unibus system mounting unit.

NOTE

Disks should normally be first on the Unibus to give them higher priority in DMA arbitration than that of the NCV11.

6.2 If it is necessary to provide an additional SPC slot for the M8217 Converter module, mount the DD11 backplane in the CPU or expansion box.

NOTE

Some old Unibus backplanes are incompatible with the M8217 module. If in doubt, check the DW11 Installation Manual.

6.3 Connect the backplane power harness(es) to the power distribution panel(s).

6.4 Install the M9401 module in slot AB01 of the DDV11-C backplane.

6.5 Install the M8217 in the Unibus backplane.

NOTE

When the M8217 module is mounted in a Unibus backplane, remove the NPG IN/NPG OUT jumper between pins CA1 and CB1 of the SPC slot to be used.

6.6 Connect the two BC05L cables between the M9401 and M8217 modules, J1 to J1, and J2 to J2 (colored stripe adjacent to pins UU/VV).

6.7 Install the NCV11 modules in the DDV11-C backplane in the sequence shown in Figure 2-1.

6.8 Install the M9400-YB module in slot AB02, directly behind the M9401 module in the LSI-11 Bus backplane.

6.9 Install the H322 distribution panel.

6.10 Interconnect the NCV11 modules and the H322, shown in Figure 2-1.

7.0 POWER CHECKS:

7.1 Check BA11 box voltages. +5V ± 5%, +15V ± 5%, -15V ± 5%

8.0 DIAGNOSTIC TEST PROCEDURE:

"For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria; e.g. pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the CHECKLISTS."

8.1 NCV11 Logic Test (Checks the M8026 and M8036)

8.1.1 Load the MD-11-DVNCA program into memory.

8.1.2 Start the program at location 200. (Restart address is 204)

8.1.3 Type L (CR) to start the test

8.1.4 To terminate the test type CTRL/C.

8.2 NCV11 Differential Linearity Test (Checks the A017 and M8036)

8.2.1 Switch the Maintenance Switch (S1) on the A017 module to MAINTENANCE (toward the I/O connector).

8.2.2 Plug the Self Test Connector into J1 on the A017 module. Connect the red jumper wire on the connector to test point R (TPR) on the A017 module.

8.2.3 Load the MD-11-DVNCA program into memory.

8.2.4 Start the program at location 200.

8.2.5 Type D (CR) to start the test.

8.2.6 Type CTRL/C to terminate test.

8.3 NCV11 Final Acceptance Test (This test repeats the logic and differential linearity tests)

8.3.1 MD-11-DVNCA must be loaded into memory.

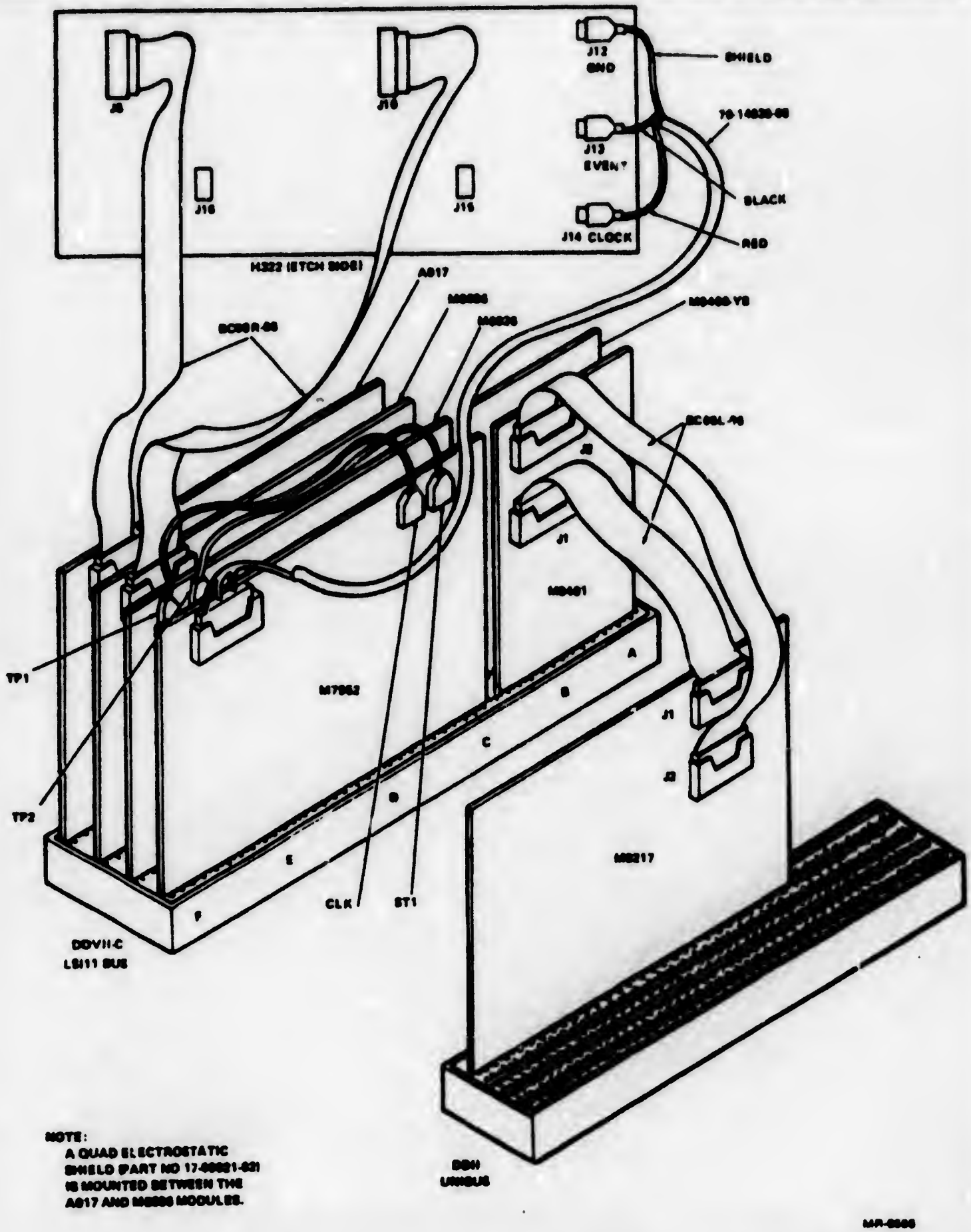
8.3.2 Make sure the Self Test Connector is plugged into connector J1 on the A017 module. The red jumper wire is connected to test point TPR on the A017, and switch S1 on the A017 module is switched to MAINTENANCE.

8.3.3 Type F (CR) to start the test

8.3.4 Type CTRL/C to terminate the test.

9.0 TEST PROCEDURE:

Reference 8.0



NOTE:
A QUAD ELECTROSTATIC SHIELD (PART NO 17-00021-021) IS MOUNTED BETWEEN THE A017 AND M8026 MODULES.

Figure 2-1 DW11-NCV11-H322 Interconnections (Unibus-Based System)

A6:2205

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MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DR11-A GENERAL DEVICE INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6205					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Selegrewski	Tom	A	SP	MAA6205-0-0	A

DR11-A GENERAL DEVICE INTERFACE

REFERENCE DOCUMENTS

DR11-A Engineering Drawings, Print Set.

MAST Phase I Check-Off List.

Workmanship Manual, DEC.

Finish and Color Standard, DEC STD 092.

REQUIRED TEST EQUIPMENT

PDP-11 System with input device.

M980 Maintenance Module.

Digital Voltmeter, Fluke Model 465 or equivalent.

REQUIRED TEST SOFTWARE

MAINDEC-11-D8LA Diagnostic Write-up, DR11A Device Register Test.

MAINDEC-11-D8LA Diagnostic Tape.

CHECKOUT INSPECTION

Following Receipt of the test item(s), perform a brief (quick scan) visual inspection for obviou: discrepancies per the DEC Workmanship Manual and DEC STD 092.

TEST SET-UP

Set-up the test item(s), with all power off, in the configuration shown in Figure 1. Note that the test item has a floating vector. Check that it has the proper jumper configuration.

VOLTAGE CHECKOUT

Power up the system to check the +5VDC at each SPC slot containing a test plan. Use the digital voltmeter to measure the voltage between pins A2 (+5VDC and C2 (GND) at each applicable SPC slot on backplane. The voltage shall be 5.00 VDC ±0.25 VDC. Note that the H744 Regulator has a +5 VDC voltage adjust potentiometer.

11 SYSTEMS CHECKOUT TEST PROCEDURE

Perform the checkout test in the sequence detailed in this section. Program starting address, switch settings and operator action are contained herein. However, refer to the Diagnostic Write-Up, MAINDEC-11-DL8A, for more detailed information, should the need arise.

DEVICE REGISTER TEST

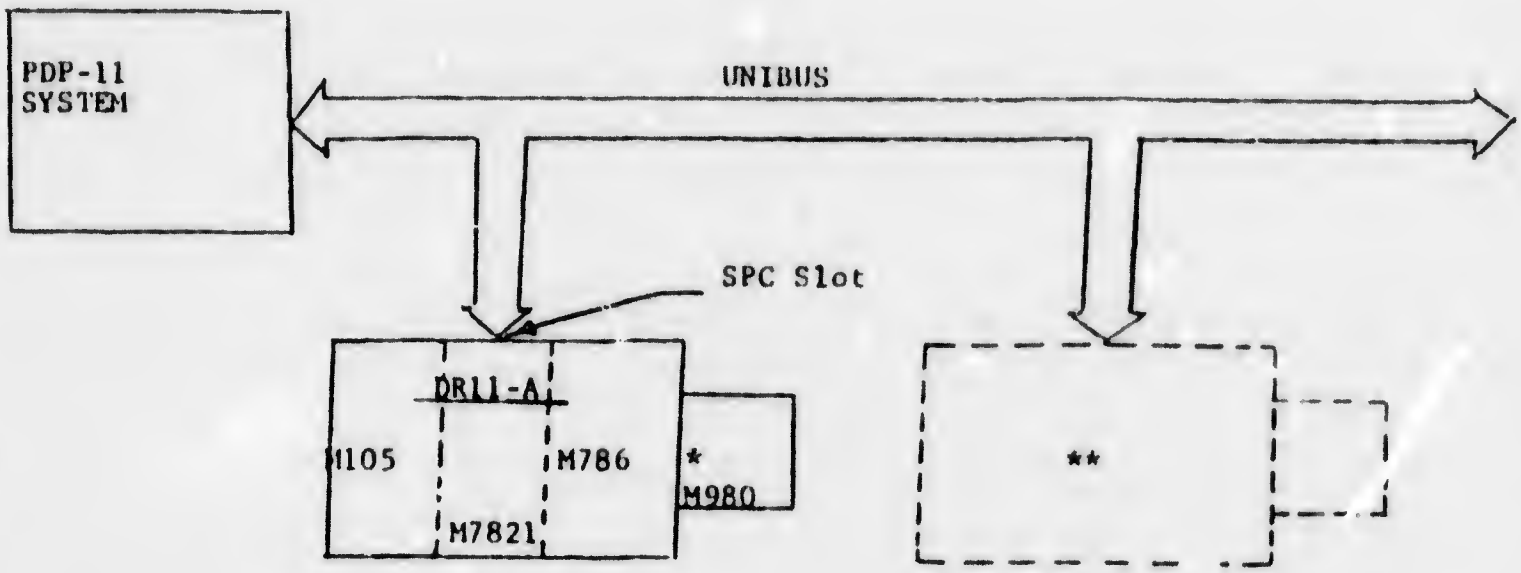
Load starting address 200.

Start program with all control switches down (zero).

Allow test to run for 15 minutes. Note that bell will ring at completion of each pass.

No errors allowed.

For restart after fix, repeat 7.1.1 and 7.1.2.



Notes:

* An M980 Special Maintenance Module must be connected to each DR11-A at the M786 dual connectors.

** A maximum total of 32 sequential DR11-A's may be connected for test.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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DR11-B DIRECT MEMORY (DMA) INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6210					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM SEKANOWSKI	TOM	A	SP	MAA6210-0-0	A

DR11-B DIRECT MEMORY (DMA) INTERFACE

REFERENCE DOCUMENTS

DR11-B Engineering Drawings, Print Set.

MAST Phase I Check-Off List.

Workmanship Manual, DEC.

Finish and Color Standard, DEC STD 092.

DR11-B Manual, DEC-11-HDRC-D.

REQUIRED TEST EQUIPMENT

PDP-11 System with input device.

Digital Voltmeter Fluke Model 465 or equivalent.

REQUIRED TEST SOFTWARE

MAINDEC-11 DZDRB Diagnostic Write-up, DR11B PDP11 General NPR Interface.

MAINDEC-11-DZDRB Diagnostic Tape.

CHECKOUT INSPECTION

Following Receipt of the test item, perform a brief (quick scan) visual inspection for obvious discrepancies per the DEC Workmanship Manual and DEC STD 092.

TEST SET-UP

Set-up the test item, with all power off, in the configuration shown in Figure 1. Remove modules from slots CD4. Then transfer the Test Board from Slots AB2 to Slots CD4.

VOLTAGE CHECKOUT

Power up the system to check the +5VDC at the test item backplane. Use the digital voltmeter to measure the voltage between pins A2 (+5 VDC) and C2 (GND) on the backplane. The voltage shall be 5.00 VDC $\pm$ 0.25 VDC. Note that the H744 Regulator has a +5 VDC voltage adjust potentiometer.

11 SYSTEMS CHECKOUT TEST PROCEDURE

Perform the checkout test in the sequence detailed in this section. Program starting address, switch settings and operator action are contained herein. However, refer to the Diagnostic Write-Up, MAINDEC-11-DZDRB, for more detailed information, should the need arise.

DEVICE REGISTER TEST

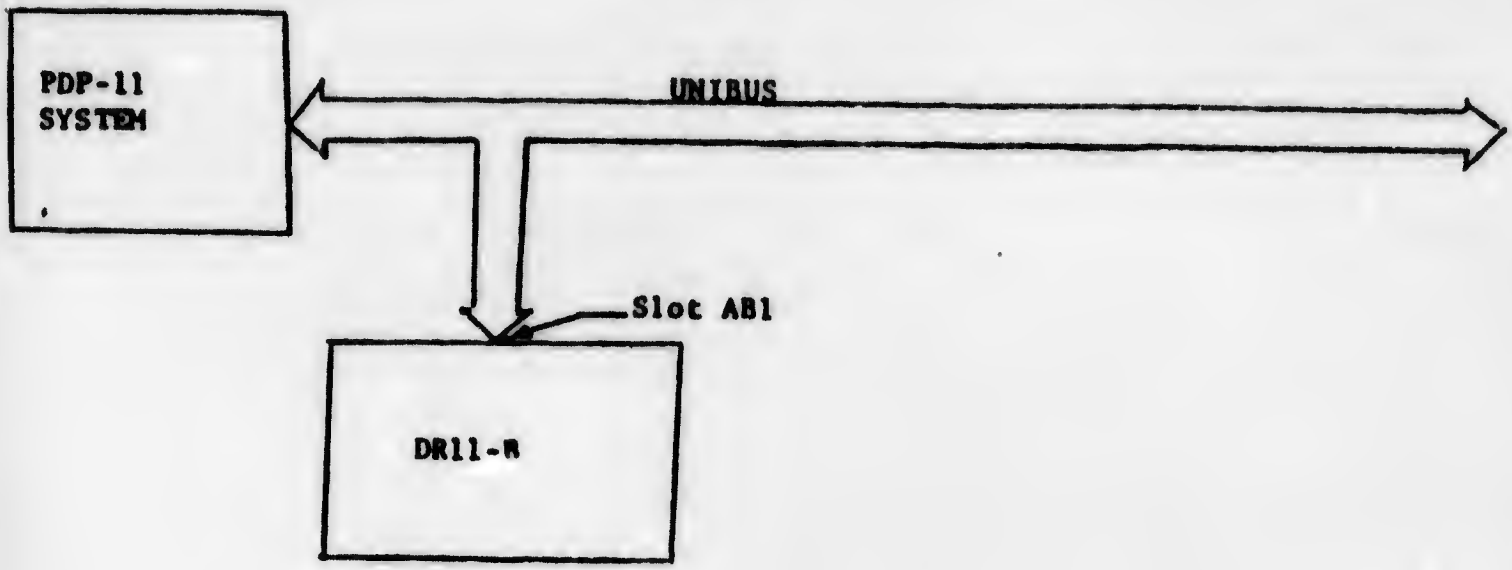
Load starting address 200.

Start program with all control switches down (zero).

Allow test to run for 30 minutes.

No errors allowed.

For restart after fix, repeat first two steps of this section.



FUNCTIONAL TEST CONFIGURATION

FIGURE 1

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MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DR11-C GENERAL DEVICE INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6220					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jakimiewski		A	SP	MAA6220-0-0	A

DR11-C GENERAL DEVICE INTERFACE

REFERENCE DOCUMENTS

DR11-C Engineering Drawings, Print Set.

MAST Phase I Check-Off List.

Workmanship Manual, DEC.

Finish and Color Standard, DEC STD 092.

DR11-C General Device Interface Manual, DEC-11-HRDCA-D-D.

REQUIRED TEST EQUIPMENT

PDP-11 System with input device.

BCØ8R Maintenance Cable.

Digital Voltmeter, Fluke Model 465 or equivalent.

REQUIRED TEST SOFTWARE

MAINDEC-11 DZDRC Diagnostic Write-up, DR11C Device Register Test.

MAINDEC-11-DZDRC Diagnostic Tape.

CHECKOUT PROCEDURE

Following Receipt of the test item(s), perform a brief (quick scan) visual inspection for obvious discrepancies per the DEC Workmanship Manual and DEC STD 092.

TEST SET-UP

Set-up the test item(s), with all power off, in the configuration shown in Figure 1. Note that the test item has a floating vector. Check that it has the proper jumper configuration.

VOLTAGE CHECKOUT

Power up the system to check the +5VDC at each SPC slot containing a test item. Use the digital voltmeter to measure the voltage between pins A2 (+5 VDC) and C2 (GND) at each applicable SPC slot on backplane. The voltage shall be 5.00 VDC $\pm$ 0.25 VDC.

11 SYSTEMS CHECKOUT TEST PROCEDURE

Perform the checkout test in the sequence detailed in this section. Program starting address, switch settings and operator action are contained herein. However, refer to the Diagnostic Write-Up, MAINDEC-11-DZDRC, for more detailed information, should the need arise.

DEVICE REGISTER TEST

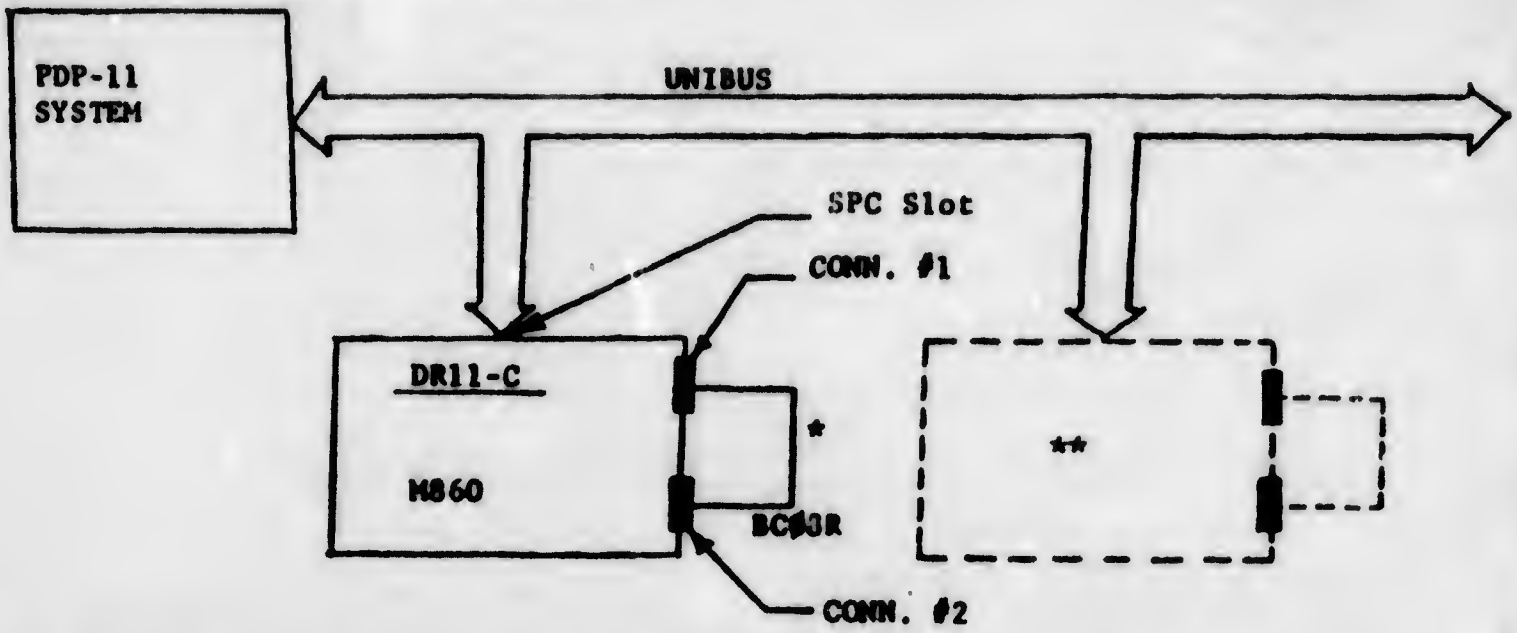
Load starting address 200.

Start program with all control switches down (zero).

Allow test to run for one pass. Note that at completion of each pass, of each test item, an * will be printed.

No errors allowed.

For restart after fix, repeat first two steps of this sectio



Notes: *A BC03R Special Maintenance Cable must be connected to each DR11-C at the M860 dual connectors.

**A maximum total of 32 sequential DR11-C's may be connected for test.

FUNCTIONAL TEST CONFIGURATION

FIGURE 1

A6225

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DRV11 16 BIT PARALLEL LINE UNIT FOR PDP 11/03 Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6225					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Jeleniewski		A	SP	MAA6225-0-0	A

EN-01888-18-N678-(DDA)

DRV11 16 BIT PARALLEL LINE UNIT FOR PDP -11/Ø3

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeups. For the purpose of expediency, the procedure has been kept brief, and to the point, to keep from confusing the user. For additional information, it will be necessary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD. 116)

2.2 DRV11 Engineering Specification A-SP-DRV11

2.3 LSI11 PDP 11/Ø3 User's Manual EK LSI11-TM-ØØ1

2.4 DRV11 Printset

2.5 ADV11-A, KWV11-A, AAV11-A, DRV11-A, User's Manual EK-ADV11-OP-ØØ1

2.6 LSI11 PDP 11/Ø3 Configuration and Installation Guide EK-LSI11-IN-ØØ1

3.0 REQUIRED TEST EQUIPMENT

3.1 LSI11 Standard Computer

3.2 DRV11 Module

3.3 BCØ8R-1 Test Cable

3.4 Output terminal/DLV11

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC 11-DVKAF DRV11 Test Diagnostic and Write up

4.2 MAINDEC 11-DADRC DEC/X11 Exerciser and Write up

5.0 SPECIAL INSPECTIONS AND CHECKS

5.1 If part of DEC LAB Ø3 System variation H or J, module will have 2 BCØ42-15 cables plugged into J1 and J2 for communication with the outside world.

6.0 TEST SET UP

6.1 Insure that jumpers A3 thru A11 are removed and jumper A12 is inserted for a device address of 167770.

6.2 Insure that vector jumpers V3, V4, and V5 are installed and vector jumpers V6 and V7 are removed for a vector of 300.

6.3 Install BC08R-1 Test Cable into Berg connectors J1 and J2.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 DRV11 Test (DVKAF)

7.1.1 Load program through appropriate load media

7.1.2 Program starting address

7.1.2.1 Load address 200
7.1.2.2 Start 000000 software SR default value

7.1.3 Alternate software SR settings (loc 122)

7.1.3.1 SWR15 = 1 Continue on error
7.1.3.2 SWR14 = 1 Loop on current error
7.1.3.3 SWR10 = 1 Loop on current test
7.1.3.4 SWR 9 = 1 Run test module

7.1.4 Operator Action

7.1.4.1 Type 200G

7.1.5 Evidence of End of Pass and Runtime

7.1.5.1 "END OF PASS" will be typed every 10 seconds.

7.1.6 Acceptable Errors: None

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TITLE DT03 - FM - FP Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 76680010-0-6230					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jehmiewski		A	SP	MAA6230-0-0	A

DT03 - FM - FP

SPECIAL INSTRUCTIONS

Before powering up DT03-FM/FP read the option description thoroughly.

The DT03-FM/FP Power Supply, and all shared bus ("C" Bus) devices power source must be on non-switched power from the 861-Power Controller, or from some other unswitched power source.

TEST EQUIPMENT

Two (2) PDP-11 processors
Unibus tester, or a I/O device that can be shared by both PDP-11 CPU's.
For further information refer to option description.

REFERENCE DOCUMENTATION

Manuals:	CSS-MO-F-1[illegible]-19 Option Description
Checkout Procedures:	Reference Option Description Page 2.3 Section 2.5 thru 2.6
Acceptance Procedures:	Reference Option Description Page A-2 Section A.5 thru A.7
Engineering Specs:	Reference Option Description Page 1-3 Section 1.6
Prints:	DT03-F
MAINDEC Listings:	DEC SPEC-11-ATV-ADC ABS MU1:T:TY Processor Diag. DEC SPEC-11-AXAAXC DAS Must be used with slave module DATS DEC SPEC-11-AXJAXB DAS DT03FR Controller Module (Single Device) DEC SPEC-11-AXTAXA DAS DT03FR Controller Module (Multiple Device) DEC SPEC-11-AXASXA SRC DTAS Slave Module for DTAC

A62-240

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DA11-BD Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6240					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jekanowski		A	SP	MAA6240-0-0	A

DA11-BD

SPECIAL INSTRUCTIONS

Reference option description page 2-1, section 2.1 for site considerations, and section 2.2 for cabling.

For further information, read the option documentation.

TEST EQUIPMENT

Two (2) PDP-11 processors

For further information refer to the option description, and the DR11-B Manual.

REFERENCE DOCUMENTATION

Manuals:	CSS-MO-F-10.4-1?A
Checkout Procedures:	Page 2.2, section 2.4.1
Acceptance Procedures:	Reference Diagnostic Listing page 7, section twelve (12)
Engineering Specs:	Page 1, section 1.3
Prints:	Reference DR11-B-DA11-B
MAINDEC Listings:	DEC SPEC-11-DZDRB-C-D HRS DEC SPEC-11-AWYAX8 OBJ. (DEC X11)


A6Z960

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DR11-K GENERAL DIGITAL I/O INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6260					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekiewicz		A	SP	MAA6260-0-0	A

DR11-K GENERAL DIGITAL I/O INTERFACE

REFERENCE DOCUMENTS

DR11-K Engineering Drawings, Print Set.

MAST Phase I Check-Off List.

Workmanship Manual, DEC.

Finish and Color Standard, DEC STD 092.

DR11-K Interface User's Guide and Maintenance Manual, EK-DR11K-MM-001.

REQUIRED TEST EQUIPMENT

PDP-11 System with input device.

DD11-A or DD11-B.

BC08-R-1, one foot long Maintenance Cable.

Digital Voltmeter, Fluke Model 465 or equivalent.

REQUIRED TEST SOFTWARE

MAINDEC-11-DZDRG Diagnostic Write-up, DR11-K Digital I/O Test.

MAINDEC-11-DZDRG Diagnostic Tape.

CHECKOUT INSPECTION

Following Receipt of the test item(s), perform a brief (quick scan) visual inspection for obvious discrepancies per the DEC Workmanship Manual and DEC STD 092.

TEST SET-UP

Set-up the test item(s), with all power off, in the configuration shown in Figure 1. Note that the test item has a floating vector. Check that it has the proper "factory" jumper configuration and M7843 Interrupt Enable switch positions per Chapter 5 of the Maintenance Manual, EK-DR11K-MM-001.

VOLTAGE CHECKOUT

Power up the system to check the +5VDC at each SPC slot containing a test item. Use the digital voltmeter to measure the voltage between pins A2 (+5 VDC) and C2 (GND) at each applicable SPC slot on backplane. The voltage shall be 5.00 VDC ± 0.25 VDC. Note that the H744 Regulator has a +5 VDC voltage adjust potentiometer.

11 SYSTEMS CHECKOUT TEST PROCEDURE

Jumper W21, W22 and W23 in the A position.

Perform the checkout test in the sequence detailed in this section.

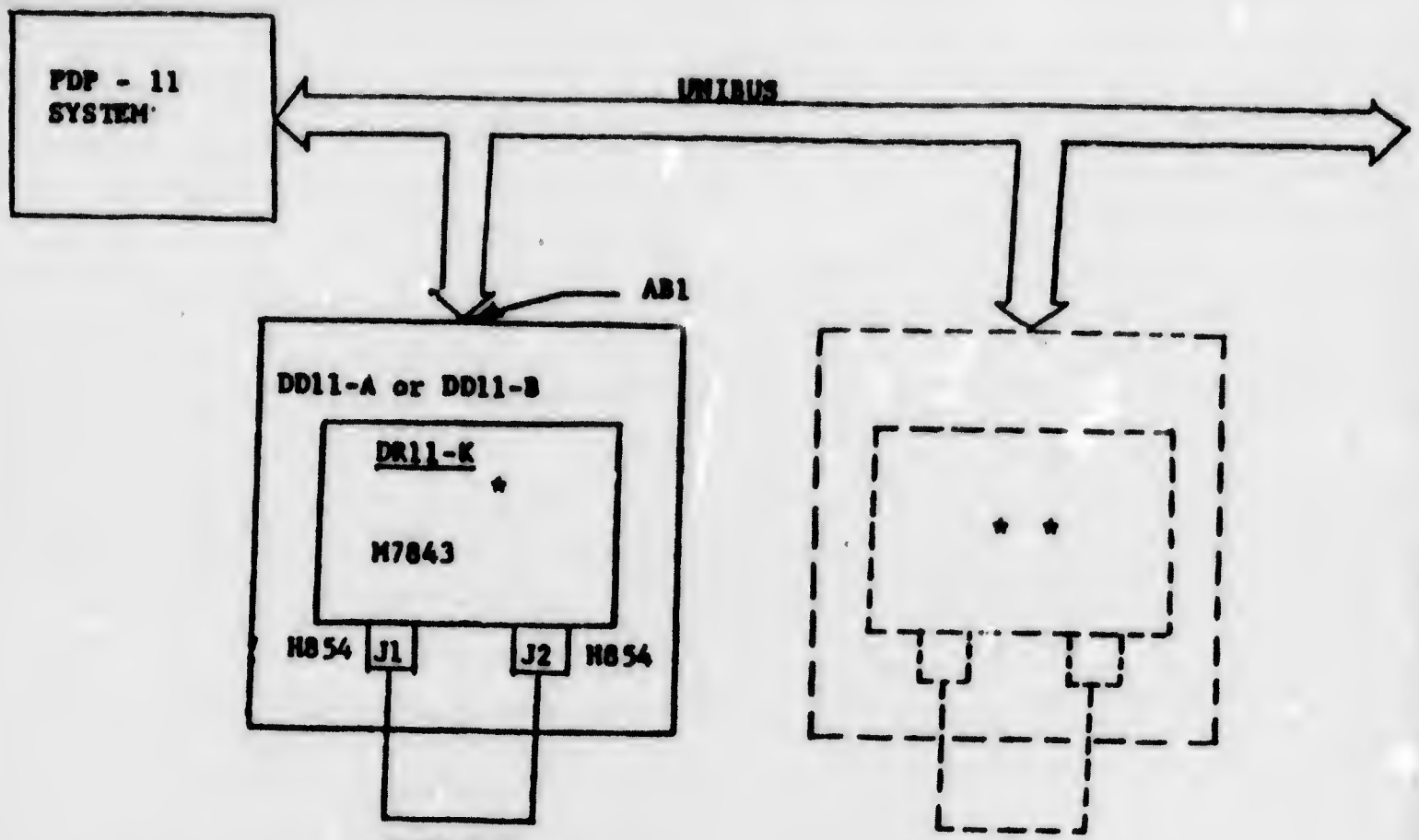
Program starting address, switch settings and operator action are contained herein. However, refer to the Diagnostic Write-Up, MAINDEC-11-DCDRG, for more detailed information, should the need arise.

LOGIC TEST

1. Load starting address 200.
2. Set all the M7843 Module INTERRUPT ENABLE switches on.
3. Start program with all control switches down (zero).
4. Allow test to run for five minutes.
5. Set all the M7843 Module INTERRUPT ENABLE switches off.
6. Start this program with all control switches down (zero).
7. Allow test to run for ten minutes.

   No errors allowed.

   For restart after fix, repeat 1 through 3 for the Interrupt Enable switches on test and repeat 1, 5, and 6 for the Interrupt Enable switches off test.



Notes: * The DRK-11 plugs into SPC slot 2 or 3 of the DD11-B or SPC slot 2 of the DD11-A.

** All DR11-K's have the same interrupt switch settings and data path jumpers.

FUNCTIONAL TEST CONFIGURATION

Figure 1

DIGITAL EQUIPMENT CORPORATION
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MANUFACTURING SPECIFICATION M.A.S.T. DATE 3/27/80

TITLE PHASE I BACKUP DOCUMENTATION FOR DR11-W

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A		MA-A0000-ML009	L.LECLERC	8-80	S. ESTES	8-80

ENG	APPD	SIZE	CODE	NUMBER	REV
BILL WHITBY	TOM JELENIEWSKI	A	SP	MAA6275-0-0	A

1.0 INTRODUCTION

The DR11-W is a general purpose, direct memory access (DMA) device that operates directly to or from memory. It is designed for use in any hex (SPC) small peripheral controller slot. The DR11W can be interfaced with a DRV11B (Q Bus) as well as connected back to back with another DR11-W to form an interprocessor system link. Any number can be added to a single system, with respect to existing configuration guidelines.

The purpose of this document is to define minimum test criteria for FA&T for a single module option and any special steps required to set up option for test. For multiples of this option, refer to reference documentation and diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Manuals and Engineering Specifications:

2.1.1 DR11W Engineering Specification SP DR11-W-C

2.1.2 DR11W Users' Guide EK-DR11W-UG

2.2 Prints and Schematics:

2.2.1 DR11W Field Maintenance Print Set MP00693

3.0 REQUIRED TEST EQUIPMENT

3.1 Hardware & Media:

3.1.1 PDP11 with available Hex SPC Slot

3.1.2 8K of Memory

3.1.3 Input console device

3.1.4 BC05L-01 Loopback Cable (Supplied with DR11-W)

3.1.5 Digital Voltmeter fluke Model 465 or equivalent

3.2 Special Tools:

3.2.1 None

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 CZDRL.?? DR11-W Gen. NPR INTFC.

NOTE: Additional Diagnostic CZDRK?? DR11-W IntrProc. Exer. is not run in FA&T due to need for additional DMA interface and PDP11 Processor.

5.0 SPECIAL INSTRUCTIONS

5.1 For Unibus-11 Systems capacitor C8 (1600 mmf.) must be cut off of of DR11-W Module.

5.2 For UBA (Unibus Adapter) of VAX, both C7 (820 mmf.) and C8 (1600 mmf.) must be installed. Reference Figure 1 drawing for locations of above components.

5.3 Wire in backplane between CA01 and CB01 (NPG jumper) must be removed from slot in wh'.n DR11-W is installed.

NOTE: Jumper must be reinstalled when module is removed unless module is replaced with another DMA (Direct Memory Access) device.

6.0 INSTALLATION AND TEST SET-UP INSTRUCTIONS

6.1 Unpacking Instructions:

6.1.1 If DR11-W module is to be installed in a system, dispose of box it was packed in. If part of an option order, retain for repacking.

6.2 Set-Up Instructions:

6.2.1 Remove G727A grant card from hex slot to be used.

6.2.2 Insure DR11-W module has DVA (Device Address) configured for 77241X. Switch pack E120 will have switches 2, 4, 6, 7, 8 and 9 on and 1, 3, 5 and 10 off. Reference Figure 1.

6.2.3 Insure DR11-W module has vector address configured for 124. Switchpack E15 will have switches 3, 5, 7 and 8 on and 2, 4, and 6 off. Switch #1 is unused and its position does not matter. Reference Figure 1.

6.2.4 Insure DR11-W module has operational mode switchpack E105 configured with switches 1, 3 and 4 on and 2 and 5 off. Reference Figure 1.

6.2.5 Insure burst mode switch S1 is in down position (toward row F of module) to select two-cycle burst operation. Reference Figure 1.

6.2.6 Insure BR plug is installed on module in E62 socket. BR5 is the standard plug part #54-08778. (Supplied with DR11-W).

6.2.7 Install BC05L-01 cable (without a twist) between J1 and J2 of DR11-W module.

6.2.8 Install DR11-W module in hex slot in which backplane jumper was removed.

7.0 POWER CHECKS

7.1 Typically when an additional module is installed in a backplane, it will cause a slight dip in voltage. Use a Digital voltmeter to insure that +5V is still within tolerance ±0.25VDC. To do this place voltmeter leads between A2 and C2 (any row) of slot in which module is installed. If necessary adjust applicable regulator for proper voltage.

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 CZDRL?? DR11-W Gen. NPR INTFC.

8.1.1 Load program into memory using applicable load device.

8.1.2 Load address 200 and press start.

8.1.3 After "Do you wish burst data late calibration? (Y = yes, N = no):" is typed out, type <N>

8.1.4 After "Do you wish multiple board dialogue? (Y = yes, N = no):" is typed out, type <N>

8.1.5 If software switch register is invoked, then the following will be printed "SWR = XXXXXX New = ", type<CR>

8.1.6 Program will now test module in maint. & cable mode/with iterations.

8.1.7 End of pass will be indicated by "End Pass #XXXXXX" after approximately 7 seconds for first pass and 60 seconds for each subsequent pass.

8.2 Allowable Errors:

8.2.1 None

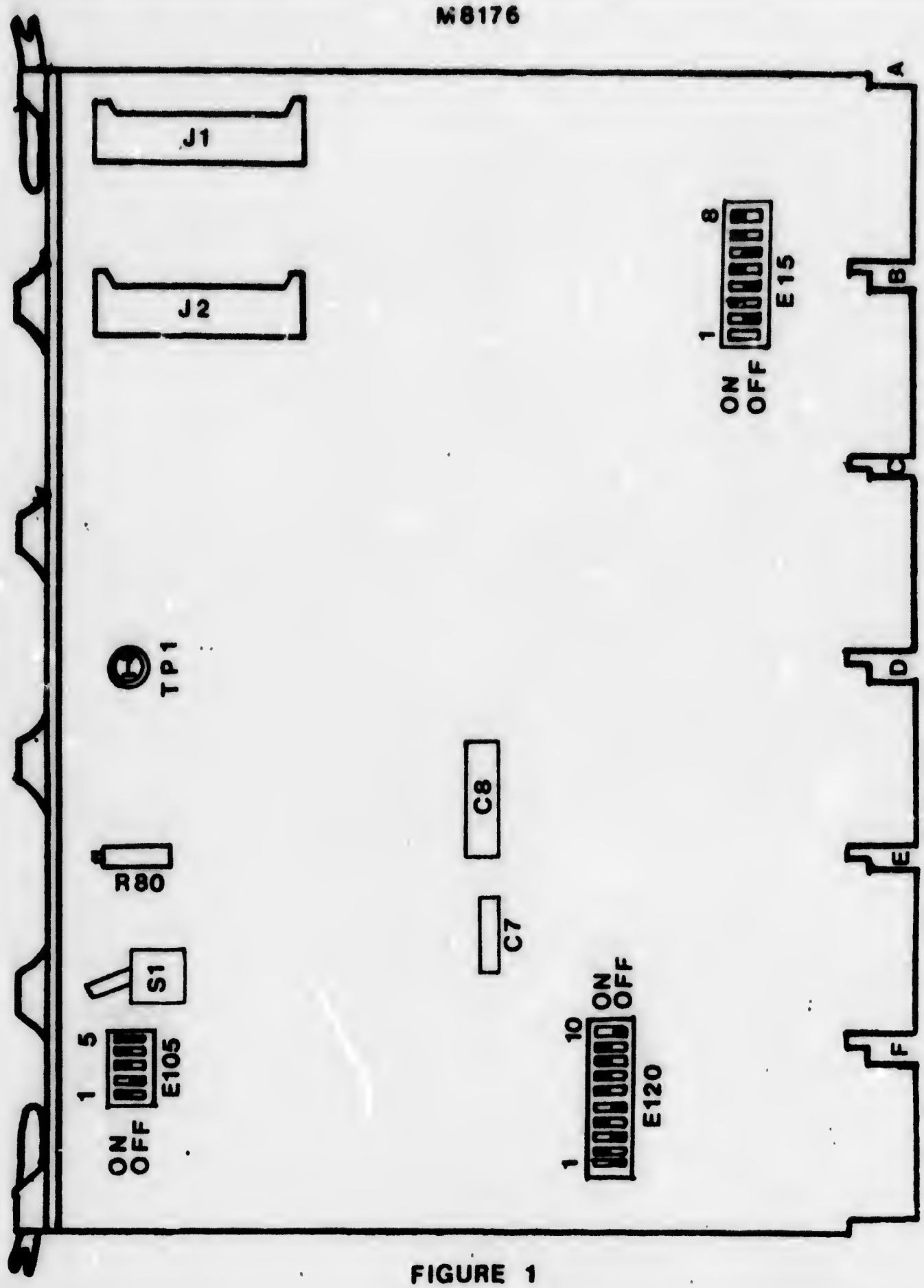

FIGURE 1

	SIZE	CODE	NUMBER	REV
	A	SP	MAA6275 -0-0	A

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE BD03 BINARY/ASCII/BINARY CONVERTER Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7110					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekniewski		A	SP	MAA7110-0-0	A

BD03 BINARY/ASCII/BINARY CONVERTER

SPECIAL INSTRUCTIONS

Refer to Option Description, Appendix A, Page A-1

TEST EQUIPMENT

REFERENCE DOCUMENTATION

Manuals:	Documentation #CSS-MO-F-4.4-SB
Checkout & Acceptance:	OPT. DES. SECT. 2.3 & 2.4
Engineering Specs:	OPT. DES. PAGE 1-1, SEC. 1.2
Prints:	Drawing Sets #A-ML-BD03-0
MainDEC Listings:	DECSPEC-11-AUXADD

DIGITAL EQUIPMENT CORPORATION
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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE BD04 DISK INTERRUPT ALARM Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7120					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jedynakowski	Tom	A	SP	MAA7120-0-0	A

BD04 DISK INTERRUPT ALARM

SPECIAL INSTRUCTIONS

BD04 must be cabled to RF11 controller with cable P/N (ATOK cable BD04) Cable plugs into slot D09 of RF11 and slot B02 of BD04, and requires the addition of a write from RF11 pin D09H2 to D16J2 (to be handwired).

TEST EQUIPMENT

Refer to Option Description Page 2-1

Section 2.1-2.4 and page 5-1, sect. 5.1

REFERENCE DOCUMENTATION

Manuals:	Document #CSS-MO-F-54-11
Checkout & Acceptance:	Option Description Page 2-2, Section 2.3.2
Prints:	Drawing Set #A-ML-BD04-0
MainDEC Listings:	DECSPEC-11-AUYADC

DIGITAL EQUIPMENT CORPORATION

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE BDO5 LINE INTERFACE CONTROLLER Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7130					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekerawski	Tom Feller	A	SP	MAA7130-0-0	A

EN:01000-10-01072-(202)

BD05 LINE INTERFACE CONTROLLER

SPECIAL INSTRUCTIONS

Refer to Option Description Page A-1, Appendix A for all checkout and acceptance procedures.

To check for indication of a test failure, transmitter test - refer to App. A, section A.5.1.5.
Receiver Test - refer to App. A, section A.6.

For DECX11 System Exerciser see System Description CSS-MS-F-73-4A, section 5.4

TEST EQUIPMENT

Refer to Option Description page A-2, section A.4.2
For test box connections and section A.5 thru A.7
For setting up test box and running the diagnostic.

REFERENCE DOCUMENTATION

Manuals:	Document No. CSS-MO-F-33-17-A
Engineering Specs:	Option Description page 1-2, section 1.3
Prints:	A-ML-BD05-0
MainDEC Listings:	DECSPC-11-AVZAD-?


A72-10

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE REORDER TRAP DEVICE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7210					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekowski		A	SP	MAA7210-0-0	A

REORDER TRAP DEVICE

SPECIAL INSTRUCTIONS

There are twelve (12) K281 fixed memory. They are to be inserted into Row "C" from right to left for the frist test. (viewed from module side of logic blocks).

For test two (2) the K281 modules must be moved to Row "D".

TEST EQUIPMENT

Refer to Option Description: page A-1, section A-2

REFERENCE DOCUMENTATION

Manuals:	Document No. CSS-MO-F-37-3-B
Checkout Procedures:	Refer to Option Description page A-1 section A.3 thru A.4.2
Acceptance Procedures:	Same as Checkout Procedure
Engineering Specs:	Refer to section 3.9.3 (M)
Prints:	Drawing Set No. A-ML-7606207-0
MainDEC Listings:	DECSPEC-11-ASOADA-PB

A7510

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 4/15/80

TITLE LPC01/LPD11 M.A.S.T.

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	Added sections 8.2.13 thru 8.2.15 and Table G	MA-A0000-ML009	L.LECLERC	8-80	S. ESTES	8-80

4

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Ayotte	Steven Estes	A	SP	MA-A7510-0-0	C

LPC01/LPD11 M.A.S.T.

1.0 INTRODUCTION

The LPC01 is a general purpose interface used in conjunction with an LDP11. It can be used by most PDP-11's to provide output to a number of photo-composition machines. All I/O from the PDP-11 thru the LPD11, thru the LPC01 to the Photocomposer is done under program control. The LPC01 includes test circuitry to simulate the photocomposer.

2.0 REFERENCE DOCUMENTATION

2.1 Manuals and Engineering Specifications

2.1.1 LPC01 Maintenance Manual EK-LPC01-MM

2.1.2 LDP11 Maintenance Manual DEC-11-HLPDA

2.2 Prints and Schematics

2.2.1 LPC01 Maintenance Print Set DD-LPC01-0

2.2.2 LDP11 Maintenance Print Set DD-LDP11-0

3.0 REQUIRED TEST EQUIPMENT

3.1 PDP-11 System with an operators console.

3.2 Line Clock.

3.3 Two (2) BC06J-XX cables.

3.4 A DVM accurate to .1V at 15VDC.

3.5 Oscilloscope, Tektronics Model 453 or equivalent.

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 LPD11 Interface Diagnostic ..... DZLPJ

5.0 SPECIAL INSTRUCTIONS

5.1 NOTE - The LPC01 must be tested in conjunction with an LPD11.

The LPD11 requires the adjustment of the "DELAY TIME". Using a scope check the delay settings of the M3020 module at pins B07F2 (adjust TOP POT) and B07T2 (adjust BOTTOM POT). Delay settings will differ according to which model of the LPC01 that it will interface to. Use the following charts to determine the pulse width and backplane pins that must be wired together that will apply to the configuration you have.

NOTES

- Be sure to measure the "Positive" pulse width.

- Before an adjustment can be made it will be necessary to have the following "toggle-in" program running:

```
200/    CLR   R0            5000
        CLR   R1            5001
NEXT:   INC   R1            5201
        MOV   R1, 1727X2    10137, 1727X2
LOOP:   INC   R0            5200
        BNE   LOOP          1376
        BR    NEXT          770
```

LPD11 DELAY TIME SETTINGS

TABLE A (M3020 ADJUSTMENT SETTINGS FOR TOP POT)

LPC01 TYPES	DELAYTIME	CONNECT PIN TO	PIN
A A/B	1.5 M SEC	L2	E1
B A/B	150 uSEC	L2	J1
C A/B	100 uSEC	L2	J1
D A/B	3.5 M SEC	L2	E1
E A/B	300 uSEC	L2	J1
F A/B	4.5 M SEC	L2	E1
H A/B	2 M SEC	L2	E1
J A/B	2.5 M SEC	L2	E1
K A/B	1.0 M SEC	L2	E1
L A/B	100 uSEC	L2	J1
M A/B	1.5 M SEC	L2	E1
N A/B	1.5 M SEC	L2	E1
P A/B	150 uSEC	L2	J1
R A/B	60 uSEC	L2	J1
S A/B	50 uSEC	L2	J1
T A/B	200 uSEC	L2	J1
U A/B	50 uSEC	L2	D1
V A/B	2.5 M SEC	L2	E1
W A/B	100 uSEC	L2	J1

TABLE B (M3020 ADJUSTMENT SETTINGS FOR BOTTOM POT)

LPC01 TYPES	DELAYTIME	CONNECT PIN TO	PIN
A A/B	500 uSEC	S2	U1
B A/B	1 M SEC	S2	P1
C A/B	500 uSEC	S2	U1
D A/B	10 uSEC	S2	S1
E A/B	100 uSEC	S2	U1
F A/B	500 uSEC	S2	U1
H A/B	1 M SEC	S2	P1
J A/B	100 uSEC	S2	U1
K A/B	350 uSEC	S2	U1
L A/B	100 uSEC	S2	U1
M A/B	200 uSEC	S2	U1
N A/B	3.5 M SEC	S2	P1
P A/B	50 uSEC	S2	U1
R A/B	35 uSEC	S2	U1
S A/B	50 uSEC	S2	U1
T A/B	35 uSEC	S2	U1
U A/B	50 uSEC	S2	S1
V A/B	100 uSEC	S2	U1
W A/B	25 uSEC	S2	S1

6.1 Unpacking Instructions as Received from High Volume.

6.1.1 The LPC01 is packed in a cardboard shipping container. Unpack the LPC01 as follows:

A. Remove the LPC01 from the shipping container.

B. Remove the polyethylene cover from the unit.

C. Ensure that the unit is clean and free of any foreign material or damage.

D. Place the LPC01 in the location in which it is to be used (tested).

E. Save all packing material if the unit is to be shipped.

6.1.2 The LPD11 is packed in a cardboard shipping container. Unpack the LPD11 as follows:

A. Remove the LPD11 Logic Backplane from it's container and mount as per configuration sheet.

B. Unpack the modules and insert them into the LPD11 Backplane as per MUL (Module Utilization List).

C. Remove the H740-D power supply from it's shipping container and mount it in the cab as per configuration sheet.

D. For ADDRESS and VECTOR assignments, reference the Product Line supplied Configuration Sheets for your system.
NOTE - The use of the FLOAT PROGRAM is illegal in determining these assignments due to "TYPESET" software limitations.

NOTE - For OPTION ORDERS use the following:
ADDRESS - 172720
VECTOR - 340

ADDRESS - M105 - JUMPER "IN" = a logical 0
VECTOR - M7821 - JUMPER "IN" = a logical 1

6.2 LPC01/LPD11 Cabling and Terminations

6.2.1 The LPD11 Interface is connected to the PDP11 Unibus using a BC11A cable of appropriate length (refer to Configuration sheet). The BC11A cable is plugged into LPD11 slot AB01, and either a Unibus Terminator or a BC11A Unibus cable is plugged into slot AB02.

The LPC01 Interface is connected to the LPD11 Control Interface via a BC06J-XX I/O cable from slot location B01 on the LPC01 to LPD11 slot location A12.
NOTE - Both ends of the BC06J-XX Interface cable have identical single-height M908 cable connectors ..... either connector can be inserted into the control interface or the universal interface.

NOTE - The maximum allowable length for the BC06J-XX interface cable is 250 feet.

7.0 POWER CHECKS

7.1 Refer to TABLES C and D.

TABLE C

LPC01 BACKPLANE VOLTAGE CHECKOUT

VOLTAGE	TOLERANCE	PIN NO.
+5VDC	+/-.25V	A01A2
-12VDC	+/-0.6V	B07B1

TABLE D

LPD11 BACKPLANE VOLTAGE CHECKOUT

VOLTAGE	TOLERANCE	PIN NO.
+5VDC	+/-.25V	A01A2
-15VDC	+/-1.0V	A01B2

8.0 DIAGNOSTIC TEST PROCEDURE

For the specific sequence of diagnostics to be run in any situation, or for the current MAST minimum test criteria, e.g.: pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are the detailed step-by-step instructions for executing each individual diagnostic contained in the "CHECKLIST".

NOTE - The LPD11 will be tested in stand-alone mode by itself.....and then the LPD11/LPC01 will be tested together. Also note that in either case; the same diagnostic is used (DZLPJ).

8.1 LPD11 STAND-ALONE ..... DZLPJ

8.1.1 Check to be sure that there is an M783 module in location B04 and no module in location A05. Also check the switch settings on the M523 module in location A10 for the correct settings as per TABLE E. Note that SW 2-8 should be ON for testing purposes.

TABLE E

LPD11 --- M523 SWITCH SETTINGS

SWITCH	1	2	3	4	5	6	7	8	
1	ON	ON	ON	ON	ON	ON	ON	ON	
2	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF-normal/ON-test
3	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	

8.1.2 Load and start the diagnostic at location 200 with the switch register equal to 0.

8.1.3 The console will ask for VECTOR and ADDRESS. Follow the instructions on the print out.

8.1.4 Halt the CPU load address 204, set switches to all zeros and start. It should run with no errors and type "END OF PASS".

8.1.5 Set the console switch 13 to a "1", depress CONTINUE twice. It must run for 10 minutes error free. NOTE - This test will continuously run the logic/data tests and therefore will not print an END-OF-PASS message.

8.1.6 Halt the CPU power down and move the M783 module from location B04 to location A05. Plug the BC06J-XX cable into location A12 and the other end into location B15.

8.1.7 Power up, restart the maintenance diagnostic at location 204 with console switch 13 on a "1". It must run for 10 minutes error free.

8.1.8 Halt the CPU power down and move the M783 module from location A05 to location B04. Remove the BC06J-XX cable from locations A12 and B15. Power up, restart the maintenance diagnostic at location 204 with console switch 11 on a "1". It must run for 5 minutes error free.

8.2 LPD11/LPC01 TESTING ..... DZLPJ

8.2.1 Connect the LPC01 to the LPD11 by plugging the LPD11 I/O cable into LPC01 location B01 and LPD11 location A12.

8.2.2 Plug in another BC06J-XX cable into location B06 of the LPC01 and LPD11 location B15.

8.2.3 Set all switches on the M523 module in the LPC01 to the off position.

8.2.4 Set switch 2-(8) on the M523 on the LPD11 to a "1" and remove the M783 from B04 and plug it into A05.

8.2.5 Plug an M111 module into location A07 of the LPC01 and remove any modules that may be in slots A04, A05, A06.

8.2.6 Put all switches on the LPC01 control panel to the normal position (DOWN).

8.2.7 Load and start the LPD Maintenance Diagnostic at location 200 with SWR = 13.

8.2.8 The program will ask for VECTOR and ADDRESS. Answer it accordingly. Run the program for 5 minutes error free.

8.2.9 Halt the program and power down the system. Remove the LPD11 I/O cable from LPC01 location B01 and plug it into B03. Put SYSTEM 1/SYSTEM 2 switch to SYSTEM 2 position and perform section 8.2.6 - 8.2.7 again.

8.2.10 Halt the program and power down the system. Remove the LPD11 I/O cable from LPC01 location B03 and plug it into B04. Place SYSTEM 1/SYSTEM 2 switch back to SYSTEM 1 position. Place ON-LINE/OFF-LINE switch to the OFF-LINE position and repeat sections 8.2.6 - 8.2.7.

8.2.11 Halt the program and power down the system. Remove the LPD11 I/O cable from LPC01 location B04 and plug it into B01. Place the ON-LINE/OFF-LINE switch back to the ON-LINE position. Place the TEST ENABLE switch in the ENABLE position and remove the IN-HOUSE test cable from the LPD11 and LPC01. Place switch S2-(8) on the M523 module in the LPD11 to the OFF (0) position.

8.2.12 Remove the M783 module from A05 and plug it into slot B04 of the LPD11.

8.2.13 Run the OUTPUT SECTION of the LPD11 Maintenance Diagnostic by setting SWR bit 6 to a "1" and restart the program at location 204. Place the LPC01 TEST ENABLE switch to the "ON" position, place the LPD11 in the "NORMAL MODE" of operation (M523 SW 2-8=0) and type a G. Then enter a series of numeric characters (0-377) and terminate with a "T". This will transmit the characters to the LPC01. Now depress the "TEST" button on the LPC01 and the octal patterns that were transmitted will appear in the DATA LIGHTS of the LPC01.

8.2.14 Power down the system. Remove the LPD11 I/O cable. Set the switches on the M523 module as per TABLE E for the LPD11 and TABLE G for the LPC01, then plug the correct modules into slots A04, or A05, or 6, or A07 etc. as per Table F.

8.2.15 All modules should be left plugged into their proper slots in the backplane and the LPC01 cover should be secured in place using the screws provided.

TABLE F

PHOTOCOMP DRIVE/POLARITY

NOTE - LPC01 module usage is dependant on variation.

LPC01	M050	M111	M205	M624	B7M1 TO *	READER CABLE	INTERFACE CABLE	M5925	
	A4	A5	A6	A7	B10	A6	A7	B7B2	B4	B6	B11	AB12	AB13
A	Y	N	N	N	N	N	N	B7A2	YES	Y	N	N	N
B	N	N	Y	N	N	N	N	B7A2	YES	Y	N	/\	/\
C	N	N	Y	N	N	N	N	B7A2	YES	Y	N	||	||
D	N	N	N	Y	Y	N	N	B7A2	YES	Y	N	||	||
E	N	N	Y	N	N	N	N	B7A2	YES	Y	N	||	||
F	N	N	Y	N	N	N	N	B7A2	YES	Y	N	||	||
H	Y	N	N	N	N	N	N	B7B2	---	Y	N	||	||
J	N	N	N	Y	N	N	N	B7A2	YES	Y	N	||	||
K	N	N	Y	N	N	N	N	B7A2	YES	Y	N	||	||
L	N	N	Y	N	N	N	N	B7A2	YES	Y	N	||	||
M	N	N	Y	N	N	N	N	B7A2	---	Y	N	||	||
N	N	N	Y	N	N	N	N	B7A2	---	Y	N	||	||
P	N	N	N	Y	Y	N	N	B7A2	---	Y	N	||	||
R	N	N	N	N	N	N	N	B7A2	---	Y	N	||	||
S	N	N	N	N	N	N	Y	B7B2	---	N	Y	||	||
T	N	N	N	N	N	N	Y	B7A2	---	N	Y	||	||
U	N	N	N	N	N	Y	N	B7B2	---	N	Y	\/	\/
V**	N	N	N	N	N	N	N	--	---	N	N	N	Y
W	N	N	N	N	N	N	N	--	---	N	N	Y	N

Notes from the chart on the previous page:

* - Wire B7M1 as directed by the above chart for the desired option.

** - The LPC01-V uses an M112 module in slot A14 and an M113 module in slot A15.

TABLE G

M523 SWITCH SETTINGS (SLOT B21 OF THE LPC01)

LPC01 OPTION	SWITCH PACK 1								SWITCH PACK 2								SWITCH PACK 3							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
A	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	0	0	0	0	0	1	0	0	1
B	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
C	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
D	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1
E	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1
F	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
H	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	1	0	0	0	0	0	1	0
J	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1
K	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1
L	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
M	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
N	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0
P	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0
S	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0
T	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1
U	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1
V	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1 = Switch "ON" / 0 = Switch "OFF"

DRAWING NO.	REV.NO.	PPS.	DESCRIPTION
A-SP-MAA5270	B	8	DUP11 PROG SYNC LINE INT.
A-SP-MAA5275	A	12	DYT01 DECDATAWAY TER. INTERFACE
A-SP-MAA5285	A	21	DYS23
A-SP-MAA5290	C	6	DMC11 INTERPROCESSOR LINK
A-SP-MAA5296	A	4	KMC11-A GEN PURPOSE MICROPROC.
A-SP-MAA5298	B	24	DMR11 SYNCRONOUS COMM. CONTR.
A-SP-MAA5310	A	3	DL11-A,B ASYNC INTERFACE
A-SP-MAA5315	A	3	DL11-C,D,E ASYNC INTERFACE
A-SP-MAA5320	B	3	DLV11 SLU FOR 11/03
A-SP-MAA5321	A	12	DLV11-E ASYN INT.W/MODEM CTL.
A-SP-MAA5322	A	12	DLV11-F ASYN .LN.INT.W/20 MA.
A-SP-MAA5324	C	16	DLV11-J 4-LINE SERIAL INTERFACE
A-SP-MAA5330	B	12	DL11-W SLU/RT CLOCK OPT.
A-SP-MAA5510	A	3	KW11-L
A-SP-MAA5520	A	3	KW11-P PROG. CLOCK
A-SP-MAA5530	A	3	KW11-W WATCH DOG TIMER
A-SP-MAA5540	B	8	KW11-K DUAL PROG CLOCK
A-SP-MAA5550	B	4	KWV11-A
A-SP-MAA6110	A	2	AA11 D/A CONVERTER
A-SP-MAA6115	A	3	AAV11-A 4 CH 12 BIT D/A
A-SP-MAA6120	A	2	ADO1-D A/D CONVERTER
A-SP-MAA6124	A	14	LPA11-K A/D CONVERTER
A-SP-MAA6125	A	4	AD11-K A/D CONVERTER
A-SP-MAA6126	A	4	AA11-K D/A CONVERTER
A-SP-MAA6127	A	4	AM11-K MULTIPLEXER EXP
A-SP-MAA6130	A	2	LPS-11 SYSTEM
A-SP-MAA6135	A	4	16 CH 12 BIT A/D FOR 11/03
A-SP-MAA6154	A	9	IB11
A-SP-MAA6160	C	16	ICS-11 SYSTEM INTEG.
A-SP-MAA6165	B	23	ICR-11 SUBSYSTEM
A-SP-MAA6170	A	21	DPM23
A-SP-MAA6175	B	7	ISB-11 DEC DATAWAY CONTR.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 12/12/79

TITLE M.A.S.T.

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	DUP11 PROGRAMMABLE SYNC LINE INTERFACE - UPDATE OLD BACKUP ECO CHANGE	MA-A0000-ML00 7	L.LECLERC	1-80	L LeClerc (Last)	7 Feb 80

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Ayotte	[illegible]	A	SP	MA-A5270-0-0	B

DUP11

1.0 INTRODUCTION

The DUP11 is a single line synchronous communication interface capable of connecting the Unibus to a synchronous serial line. It operates under either SDLC or DDCMP protocol with programmable sync characters and CRC error detection.

The option is comprised of a hex module (M7867), a BC02C-1D, a BC05C-25, and an H325 test connector. The module plugs into a PDP11 hex SPC slot. The DUP11 is fully programmable and operates in both full and half duplex modes. The DUP11 has modem control and EIA RS232C level conversions.

2.0 REFERENCE DOCUMENTATION

2.1 Manuals and Engineering Specification:

2.1.1 DUP11 Maintenance Manual EK-DUP11-MM-?

2.2 Prints and Schematics:

2.2.1 DUP11 Printset MP-DUP11-00

3.0 REQUIRED TEST EQUIPMENT

3.1 PDP11 System with a hex SPC slot
3.2 Console terminal
3.3 DVM accurate to .1V at 15VDC

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 F oat Program ..... DZFLA
4.2 Basic DUP11 and Off-line SDLC Tx Tests ... DZDPB
4.3 DUP11 Off-line SDLC Rx Tests ..... DZDPC
4.4 SDLC and DDCMP Tests ..... DZDPD

6.0 INSTALLATION AND TEST SET-UP INSTRUCTIONS

6.1 Run the Float Program (DZFLA), to determine the correct Vector and CSR Address settings for the DUP11. Refer to SP-MA-A3000 for details on running FLOAT.

6.2 Configure the DUP11 Address by setting the switches on the switch pack at E113. See table A.

6.3 Configure the DUP11 Vector by setting the switches on the switch pack at E59. See table B.

6.4 The seven jumpers on the DUP11 module are used to select desired functions and should be configured as per the customer requirements. The functions and their normal settings are shown in table C and their locations in figure 1.

6.5 Install the DUP11 module in a hex SPC slot and insert the BC02C cable in J1. Connect the BC05C-25 cable to the BC02C and place the H325 test connector on the end of the BC05C-25.

7.0 POWER CHECKS

7.1 Verify the presence of the following voltages on the backplane pins of the hex SPC slot which contains the DUP11:

VOLTAGES	POWER	PIN
+5V +/- 0.25V	3.6A	AA2
-15V +/- 0.75V	325ma	CU1
+15V +/- 0.75V	600ma	CB2

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 DUP11 OFF-LINE SDLC X-MITTER DIAG ..... CZDPB

8.1.1 Load address 200.

8.1.2 Switch Register Equal to BIT ZERO = 1.

8.1.3 Depress Start. The Diagnostic will begin by typing out the MAINDEC name and PROGRAM name.

NOTE - If multiple DUP11's are to be tested, they must all be configured the same (i.e. jumpers W1 to W7 and H325).

8.1.4 The console will print REC CSR ADDR? Type in the address of the first (if more than one DUP11 is to be tested) reciever status register.

8.1.5 The console will print VEC ADDR? Type in the vector address of the first DUP11.

8.1.6 The console will print PRIORITY? Type in the priority level of the DUP11(s).

8.1.7 The console will ask for the # of DUP11's (in octal)? Type in the number of DUP11's to be tested.

8.1.8 The console will print IS THE OPTIONAL CLEAR JUMPER IN? (Y OR N) Type in the appropriate answer (y if W3 is in).

8.1.9 The console will print IS THE H325 CONNECTOR ON? (Y OR N) Type in Y.

8.1.10 The console will print SEC TX JUMPER IN? (Y OR N) Type in the appropriate answer (Y if W4 is in).

8.1.11 The console will print SEC RX JUMPER IN? (Y OR N) Type in the appropriate answer (Y if W1 is in and W2 is out).

8.1.12 The console will print a DUP11 Status Map and begin testing. An End Of Pass message will be issued for each DUP11 which passed.

8.1.13 No errors are allowed.

8.2 DUP11 OFF-LINE SDLC RCVR TEST .....CZDPC

8.2.1 Repeat steps 8.1.1 thru 8.1.13 to execute the OFF-LINE SDLC RCVR TEST (CZDPC).

8.3 DUP11 SDLC DECMD TEST .....CZDPD

8.3.1 Repeat steps 8.1.1 thru 8.1.13 to execute the SDLC DECMD TEST (CZDPD).

TABLE A

DUP11 ADDRESS SELECTION CHART

SWITCH	IS	TO SELECT ADDR BIT
E113-1	OFF	3
E113-2	OFF	4
E113-3	OFF	5
E113-4	OFF	6
E113-5	OFF	7
E113-6	OFF	8
E113-7	OFF	9
E113-8	OFF	10
E113-9	OFF	12

TABLE B

DUP11 VECTOR ADDRESS SELECTION CHART

SWITCH	IS	TO SELECT VECTOR BIT
E59-6	ON	3
E59-5	ON	4
E59-4	ON	5
E59-3	ON	6
E59-2	ON	7
E59-1	ON	8

Switches E59-7 and E59-8 are not used.

TABLE C

DUP11 JUMPER SELECTION CHART

JUMPER	FUNCTION	NORMAL	NOTE
W1	SEC. RX. ENABLE	IN	1
W2	SEC. RX. DISABLE	OUT	1
W3	CLEAR OPTION	IN	2
W4	SEC. TX. ENABLE	IN	3
W5	A DATASET CNTL	OUT	4
W6	A&B DATASET CNTL	IN	5
W7	BUS GRANT CNTL	IN	6

****** NOTES ******

1. W1 is IN to allow the DUP11 to monitor the state of the Secondary Recieve lead. W2 must be OUT. If W1 is OUT, the lead at the berg connector is disconnected from the rest of the DUP11. The W2 jumper must then be IN.

2. W3 is IN to allow the clearing of SEC TX, REQUEST TO SEND, and DATA TERMINAL READY on a DEVICE RESET or BUS INIT. W3 OUT disables the clearing of these signals.

3. W4 is IN to allow SEC TX to be sent out to the modem. W4 is OUT to disable this signal.

4. If W5 is OUT, the bit ADAT SET CHG will set if there is a transition on the RI or CTS leads. If W5 is IN, transitions on RI, CTS, CO, DSR, or SEC RX will set the ADAT SET CHG bit. This bit and DSCITEN will cause a reciever interrupt.

5. If W6 is IN, transitions on CO, DSR, and SEC RX will set the BDAT SET CHG bit. W6 OUT disables BDAT SET CHG bit. BDAT SET CHG cannot cause interrupts.

6. W7 is IN to improve the NPR latency and is only taken OUT for the KA11 processor without the KH11 option.

DUP11 (M7867) LAYOUT

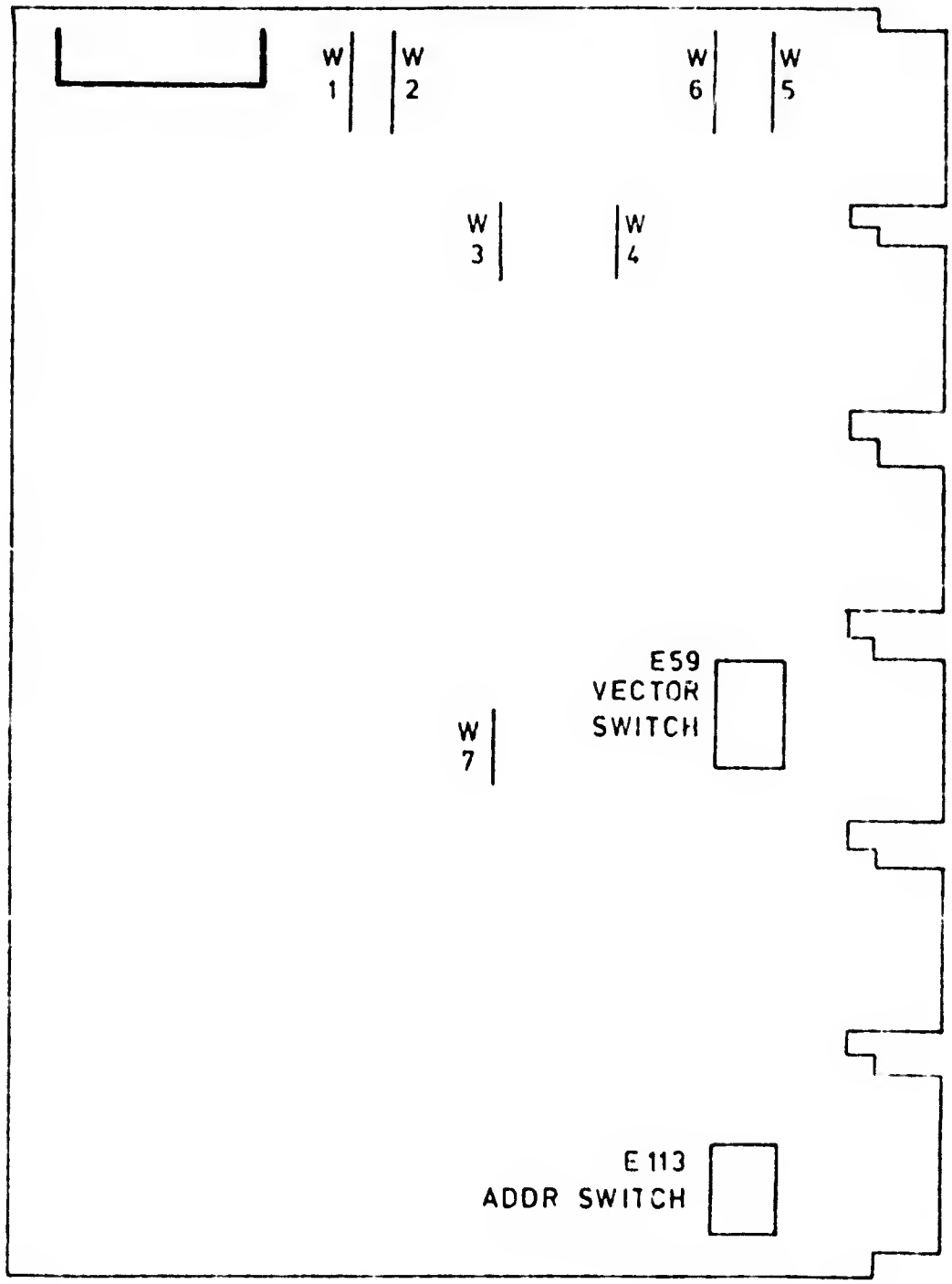


FIGURE 1

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE 7/14/81

TITLE DYT01 DECdataway Terminal Interface

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	New Back-up for DYT01 DECdataway Terminal Interface	MA-0000 ML014	Peter Gronroos	7/14/81		

ENG	APPD	SIZE	CODE	NUMBER	REV
Peter Gronroos	Bob Beck	A	SP	MA-A5275-0-0	A

DYT01 DECdataway Terminal Interface

1.0 INTRODUCTION:

1.1 The DYT01 is a single port interface which connects asynchronous 20 ma or EIA devices to the Dataway. The Dataway is a serial line of up to 15000 feet in length with a maximum of 63 ports connected to it. The DYT01 is program compatable with the DPM01 or VTi10.

2.0 REFERENCE DOCUMENTATION:

2.1 Manuals and Specifications:

2.1.1 DYT01 User Guide EK-DYT01-UG

2.1.2 DYT01 Decdataway Terminal Interface Technical Manual EK-DYT01-TM

2.1.3 Dec Dataway User's Guide EK-ISB11-UG

2.1.4 DPM Systems Application Program Reference Manual AA-C678A-TC

2.1.5 DPM Diagnostic User Guide EK-DPM00-DM

2.1.6 DECdataway Technical Manual EK-ISB11-TM

2.1.7 ISB11 Engineering Specifications SP-ISB11-0-2

2.1.8 ISB11 MAST Backup SP-MA-A617[illegible]-0-0

2.2 Prints and Schematics:

2.2.1 DYT01 Field Maintenance Print Set MP-01065-00

3.0 REQUIRED TEST EQUIPMENT:

3.1 Valid DPM System Configuration

3.2 Serial Bus Test Cable, 70-14[illegible]52

3.3 20 MA Port To Port loop Cable 70-17892-04

3.4 20 MA Test plug, 70-17894-00

3.5 EIA Port To Port loop Cable, 70-17893-04

3.6 EIA Test Plug, 70-17895-00

4.0 REQUIRED DIAGNOSTICS:

4.1 MAINDEC 11-DZRCH-SERIAL BUS EXERCISER

4.2 MAINDEC 11-CZRCI-REMOTE TERMINAL EXERCISER

4.3 DYT01 Exerciser AP-S896A-AC
(800 BPI Mag. Tape includes utilities and instruction for generating the DYT01 exerciser)

NOTE: These programs run under RSX11-M operating system software. The RSX11-M operating system must be built with Fortran IV-Plus and Spawners, Partitions for DYTCOM and DYTLIB must be set for 4 and 12K respectively.

5.0 SPECIAL INSTRUCTIONS:

5.1 To run the DYT01 EXERCISER two DYT01s have to be connected back to back.

6.0 INSTALLATION AND CHECKOUT:

6.1 Unpack and save the packing material. While unpacking inspect the unit for any defects.

6.1.1 Items which should be present are:

1	DYT01 Dataway terminal
2	90-07889 cable ties
1	17-00083-09 115v power cord
1	17-00199 220-240v power cord
1	12-18178 3/8A fuse
1	36-18329-02 Decal
3	90-06613 Mounting Nut
3	74-24129 Mounting Bracket
1	EK-DYT01-UG User Guide
1	MP-01065 Field Maintenance Print Set
1	70-17893-04 Test Cable (DYT01-MA only)
1	70-17895-00 Test Plug (DYT01-MA only)
1	70-17892-04 Test Cable (DYT01-EA only)
1	70-17894-00 Test Plug (DYT01-EA only)

6.2 Inspect the DYT@1 for the correct voltage.

6.2.1 The DYT@1 is configured for 12@ volt operation, for conversion to 22@-24@ volts first remove the power cord from the AC input. (Figure #2)

6.2.2 Slide the plastic cover to the left to expose the fuse, then pull the fuse extracter out and remove the 3/4 Amp fuse. (Figure #3)

6.2.3 Remove the voltage selector printed circuit board rotate it 18@ degrees and re-insert it so the 24@ is visible.

6.2.4 Install a 3/8 amp fuse (pn 12-18178), move the fuse extractor to its normal position and slide the plastic cover to the right.

6.2.5 Place the "This unit is configured for 22@-24@v" decal (PN 36-18329-@2) above the AC input so that it covers the "This unit is configured for 12@v" decal.

6.2.6 Install the 22@-24@ volt power cord (PN 7@-@@199) into the AC input.

6.3 Set the mode switches for the proper configuration to run the internal micro diagnostics in the loop mode.
DYT@1-EA switch 2 should be "ON" all others "OFF".
DYT@1-MA switches 2,4 and 7 should be "ON" all others "OFF". (Figures #2 & 4)

6.3.1 Install the proper test plug at the DYT@1's connectors for the EIA or 2@ MA devices.
DYT@1-MA 7@-17894-@@ 2@ MA
DYT@1-EA 7@-17895-@@ EIA

6.3.2 Apply power to the DYT@1 by plugging the AC line cord into the appropriate power source. Observe that the Status and Carrier lights flash alternately every 12 seconds. (Figure #1)

6.4 Set the DYT@1 for on-line testing by removing the power from the unit under test. Next, remove the loop test plug and set the mode switches for on-line operations.

6.4.1 DYT@1-EA all switches are "OFF".
DYT@1-MA switches 4 & 7 are "ON" all others "OFF" for the active DYT@1 and the passive DYT@1 has all switches off. (Figures @2 & 4)

6.4.2 Connect the loop test cables between the DYT@1s. DYT@1-EA uses cable 70-17892-04. DYT@1-MA uses cable 70-17893-04, insure the cable is connected so the active end (red and white wires in pin locations 3 and 5) is connected to the active DYT@1 and the passive end (red and white wires in pin locations 1 and 8) is connected to the passive DYT@1.

6.5 Connect the DYT@1 to the Dataway.

6.5.1 Using cable 70-14152 connect two DYT@1s to the ISB11 through the DECdataway. (Figure @2) For additional information refer to the Engineering ISB11 Specification. SP-ISB11-0-2

6.5.2 Apply power, the unit should go through a series of micro diagnostics then come on-line. At power up the status light will flash once, the micro diagnostics run and the status light will flash again before the DYT@1 goes on-line. (Figure @1)

7.0 POWER CHECKS:

7.1 The DYT@1 is a sealed unit so no power checks are necessary.

8.0 DIAGNOSTIC TEST PROCEDURE:

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria, e.g.: pass counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the checklist.

Operator responses will be underlined and CR equals a carriage return.

8.1 Run DZKCI by using the following procedure.

8.1.1 Log onto the system, start the error logger and run the diagnostics by typing the following.

```
>HELLO CR
ACCOUNT OR NAME: 4,4 CR (system accounts and
PASSWORD: SYSLIB CR      passwords are examples)

        RSX-11M BL26   MULTI-USER SYSTEM

GOOD MORNING
15-MAY-81 10:02 LOGGED OM TERMINAL TT0:

>SET /UIC=[1,6] CR  (changes the account number)
>ERF CR             (turns error logger off)
>PIP [1,6]*.*;*/DE CR  (clears error file)
>SET /UIC=[200,270] CR
>RUN ERRLOG CR          (starts the error logger)
>
 ERL -- ERROR LOG INITIALIZED


>RUN CZKCI? CR
DCP-A>STA CR

# UNITS  (D)  ? 2 CR

UNIT 1
ENTER CONTROLLER NUMBER : (0)  0 ? CR
ENTER TERMINALS ON THAT CONTROLLER : (D) 1 ? 1,2 CR
```

```
SELECTED SERIAL LINE PORTS

UNIT ** CONTROLLER ** LOGICAL SB ** LUN ** TYPE
  1          0              001        9     DPM01-PORT 0
  2          0              002       10     DPM01-PORT 1

START OF TESTING

END OF PASS     0,   TIME=10:42

END OF PASS     1,   TIME=10:43
```

8.1.3 To stop the test press the CTRL and C keys.

8.2 Run diagnostic DZKCH.

8.2.1 Type the following:

```
>RUN DZKCH CR
DCP-A>STA CR

# UNITS  (D)  ? 2 CR

UNIT 1
ENTER CONTROLLER NUMBER : (0) 1? CR
ENTER TERMINALS ON THAT CONTROLLER : (0) ? 1,2 CR

NUMBER OF ENTERED TERMINALS= 2

UNIT ** CONTROLLER ** LOGICAL SB ** LUN **
001          006            001      011

002          000            002      012

TOTAL ACTIVE PASSES=19, ACTIVE TERMINALS=2, TIME=10:04

TOTAL ACTIVE PASSES=17, ACTIVE TERMINALS=2, TIME=10:05
```

8.2.2 Press the CTRL and C keys to stop the test.

8.3 Run the DYT01 EXERCISER.

8.3.1 Type the following to run the exerciser.

```
>SET /UIC=[7,250] CR
>DYM CR
DYM>SEL1 CR        (this will start the exerciser)
DYM>STA  CR        (this will get the status)

DYT01 EXERCISER                          14-MAY-81  13:52:38

RUN TIME=5.hrs HARD LIMIT=5.SOFT LIMIT=5.TRAN LIMIT=5.
```

UNITS	STATUS	HARD	SOFT	TRANS	PASCNT	ELAPSED TIME
1- 2	SEL...	0.	0.	0.	0.	1.hrs 0.mins
3- 4	.....	0.	0.	0.	0.	0.hrs 0.mins
5- 6	.....	0.	0.	0.	0.	0.hrs 0.mins
7-10	.....	0.	0.	0.	0.	0.hrs 0.mins
11-12	.....	0.	0.	0.	0.	0.hrs 0.mins
13-14	.....	0.	0.	0.	0.	0.hrs 0.mins
15-16	.....	0.	0.	0.	0.	0.hrs 0.mins
17-20	.....	0.	0.	0.	0.	0.hrs 0.mins
21-22	.....	0.	0.	0.	0.	0.hrs 0.mins
23-24	.....	0.	0.	0.	0.	0.hrs 0.mins
25-26	.....	0.	0.	0.	0.	0.hrs 0.mins
27-30	.....	0.	0.	0.	0.	0.hrs 0.mins
31-32	.....	0.	0.	0.	0.	0.hrs 0.mins
33-34	.....	0.	0.	0.	0.	0.hrs 0.mins
35-36	.....	0.	0.	0.	0.	0.hrs 0.mins
37-40	.....	0.	0.	0.	0.	0.hrs 0.mins
41-42	.....	0.	0.	0.	0.	0.hrs 0 mins
43-44	.....	0.	0.	0.	0.	0.hrs 0.mins
45-46	.....	0.	0.	0.	0.	0.hrs 0.mins
47-50	.....	0.	0.	0.	0.	0.hrs 0.mins

```
DYM>DES1 CR        (stops exercising the DYT01's)
```

8.3.2 Press the CTRL and Z keys to exit the test.

9.0 ERRORS:

9.1 Hard errors are printed on the terminal when they occur while running DZKCH and CZKCIB. The DYT01 exerciser prints the errors when STA CR is typed.

9.2 Soft errors are logged in the ISBRPT DECdataway error logger. To run this error logger type the following.

```
>RUN ISBRPT CR
  ISBRPT - DECDATAWAY ERROR REPORT

PRINT SUMMARY [ Y or N ] ? Y CR
PRINT ENTIRE FILE [ Y or N] ? N CR
OUTPUT TO LINE PRINTER [ Y or N ] ? N CR
WANT ONE CONTROLLER [ Y or N ] ? N CR
DELETE ERROR FILE [ Y or N ] ? N CR
ISBRPT . . . ERROR FILE IS EMPTY
ISBRPT . . . OPERATION COMPLETE

MCR>
```

9.3 No errors are allowed for the DYT01.

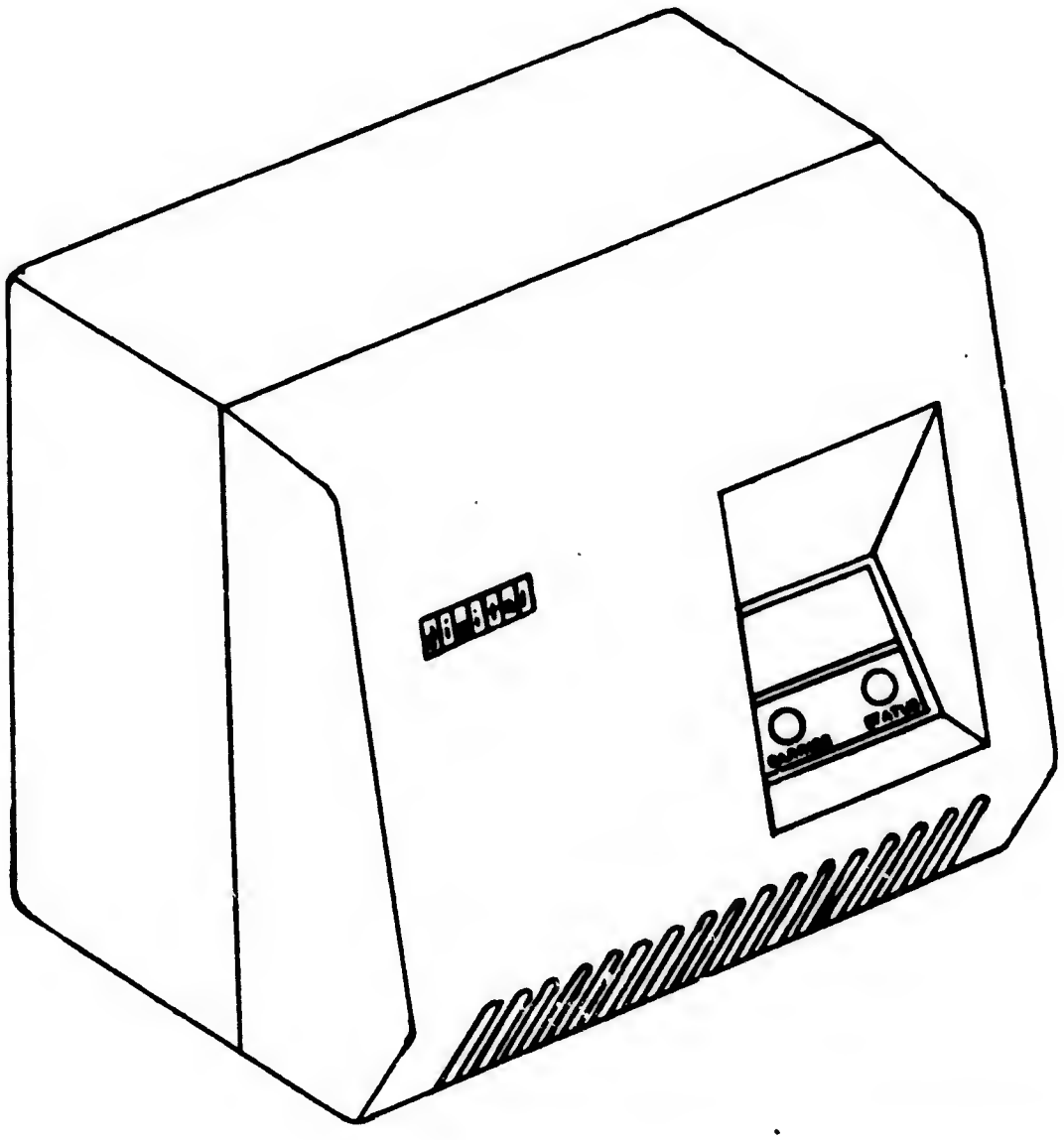


Figure #1
DYT01 Front View

TITLE MODULAR APPROACH TO SYCTEM TEST

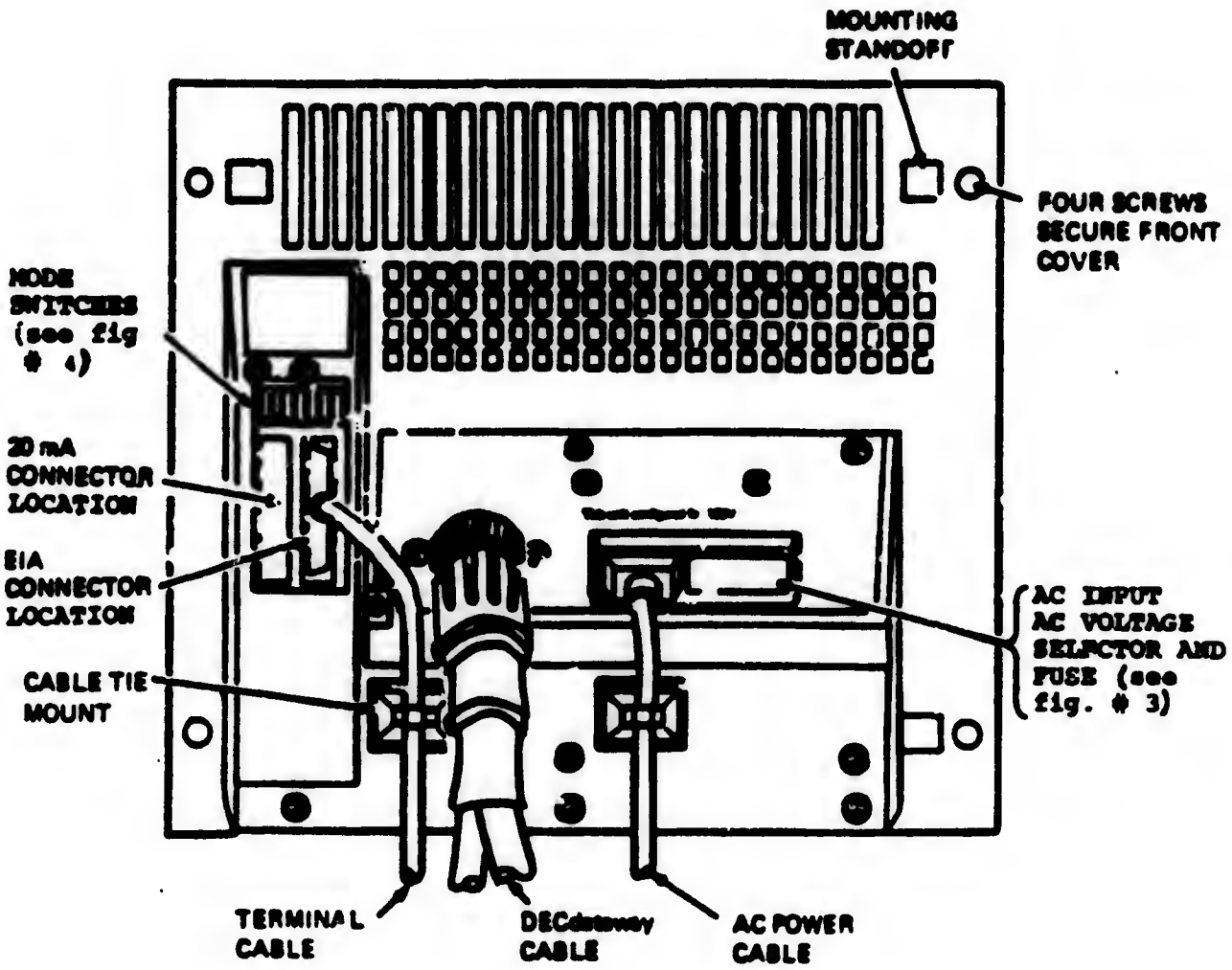


Figure #2
DYT01 Rear View

	SIZE	CODE	NUMBER	REV
	A	SP	MA-A5275-0-0	A

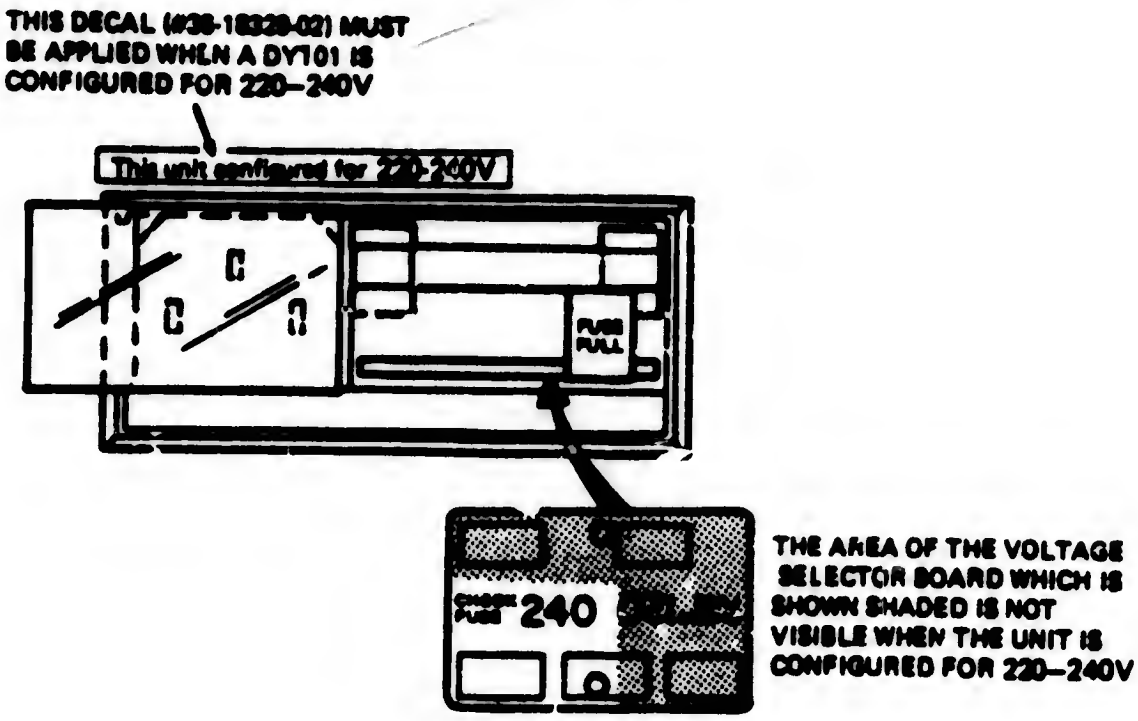


Figure # 3
AC Input AC Voltage Select And Fuse

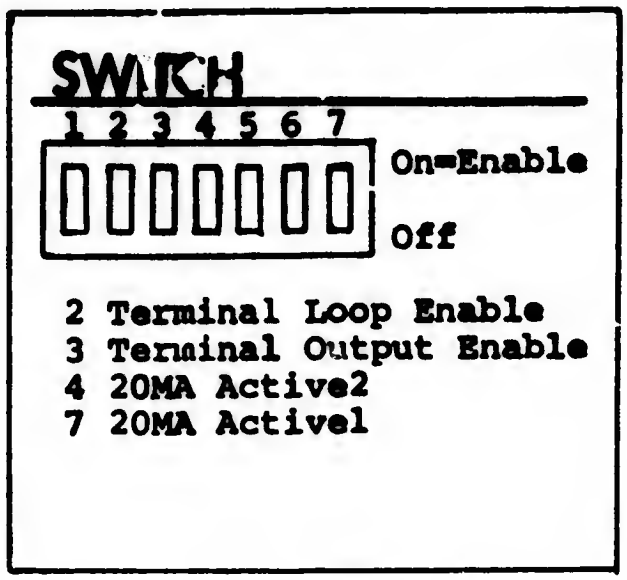
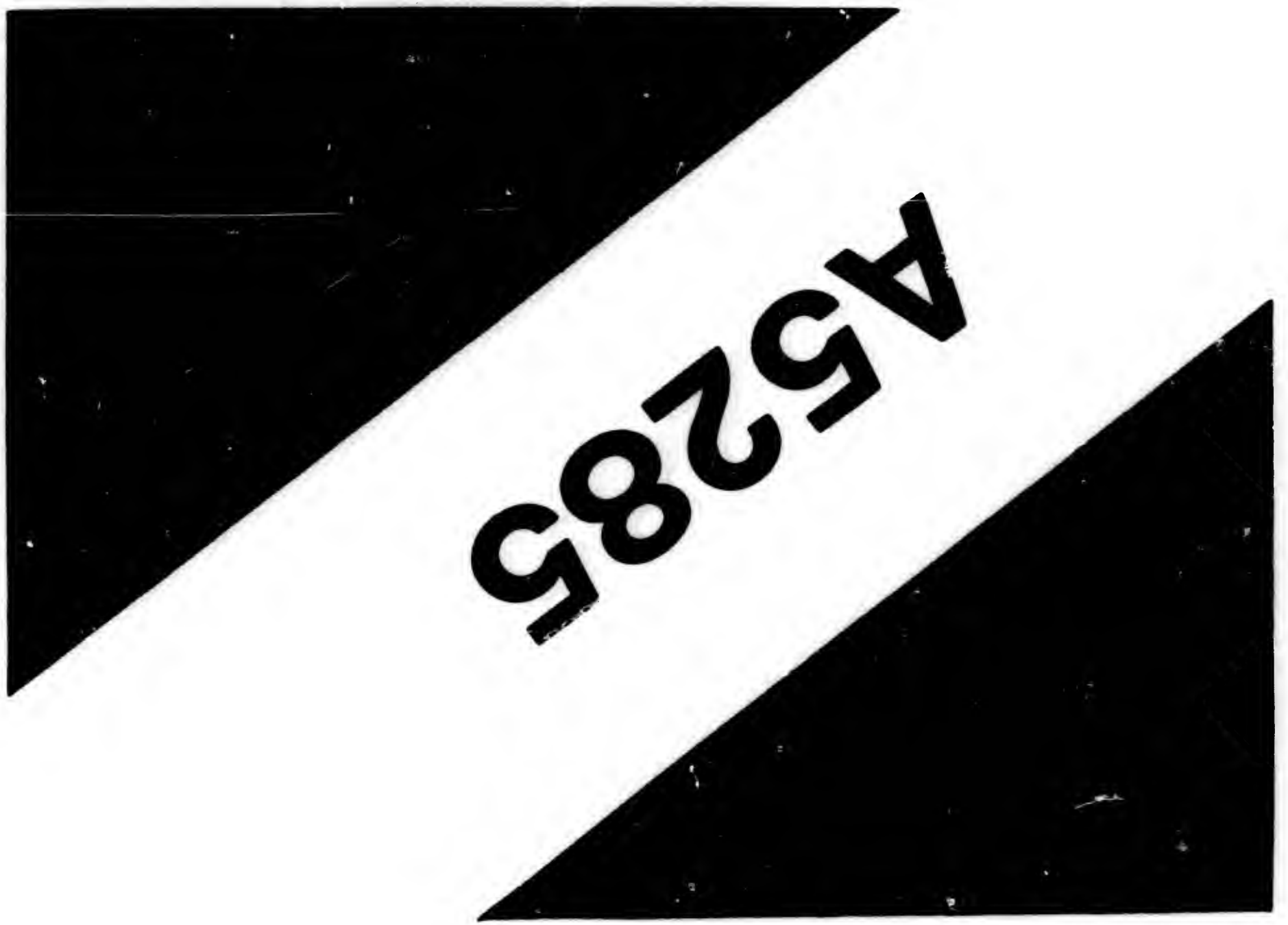


Figure # 4
Mode Switches


ASA
5285

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 10/21/81

TITLE M.A.S.T. DYS23

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
*	Preliminary Release	MA-A0000 ML015	D.HOWELL		B.BECK	
A	Initial Release		D.HOWELL	10/20	B.BECK	

ENG	APPD	SIZE	CODE	NUMBER	REV
D.HOWELL	B.BECK	A	SP	MA-A5285_0-0	A

EN-01083-16-N672-(392)

TABLE OF CONTENTS

DYS23 DISTRIBUTED I/O SUBSYSTEM

1.0 SCOPE

The DYS23 is a user programmable subsystem based on the DPM23. It uses a 30 inch cabinet and is primarily intended to be used in an industrial office enviroment as a terminal cluster controller on the DECdataway. However, it is an unbounded system and supports several standard options. User programs and diagnostics are down-line loaded from a host computer over the DECdataway.

This procedure defines minimum test criteria for the base DYS23. For options added to the base, reference other appropriate mast procedures.

The base DYS23 conists of:

DYS23-A,-D
KDF11-AA CPU
1 - MSV11-DD 32K MOS MEMORY
ISV11-B DECdataway interface
BA11-NC, -ND Enclosure and Power Supply
H9642 CAB

2.0 RESPONSIBILITY

2.1 It is the responsibility of the originator to maintain this document. Changes should be requested through the originator - if possible, or his/her group (if originator is no longer available), or through MAST administration in Salem (NI).

3.0 REFERENCE DOCUMENTATION

3.1 MANUALS:

3.1.1 MICROCOMPUTER PROCESSOR HANDBOOK	EB-18451-20/80
3.1.2 MICROCOMPUTER INTERFACES HANDBOOK	EB-20175-20/80
3.1.3 MSV11-D,-E USERS MANUAL	EK-MSV1D-OP-??
3.1.4 PROCESS I/O SUBSYSTEM USRES GUIDE	EK-PIOS-UG-???
3.1.5 DYS23 USERS GUIDE	EK-DYS23-UG-??
3.1.6 KDF11-AA USERS GUIDE	EK-KDF11-UG-??
3.1.7 BA11-N TECHNICAL MANUAL	EK-BA11-TM-???
3.1.8 DPM PROGRAMMER'S REFERENCE MANUAL	AA-C878D-TC-??

3.2 PRINTS AND SCHEMATICS

3.2.1 DYS Field maintenance print set	MP01099
3.2.2 Unit Assembly	E-UA-DYS23-0-0
3.2.3 Parts list	K-PL-DYS23-0-DBP
3.2.4 Drawing directory	B-DD-DYS23-0
3.2.5 Shipping List	B-PL-DYS23-0

4.0 REQUIRED TEST EQUIPMENT:

4.1 HARDWARE AND MEDIA:

4.1.1 Valid DPM HOST SYSTEM configuration
4.1.2 RSX11-M on appropriate host media.
4.1.3 HEWLETT PACKARD DVM or equivalent accurate to .01v @15v.
4.1.4 Serial line unit ie.; DLV11-F and terminal for LSI error information output (local mode).

5.0 REQUIRED DIAGNOSTIC PROGRAMS:

5.1 DPM REMOTE DIAGNOSTICS KIT #ZP126-RD:

5.1.1	AP-00043C-BC	RSX11M V3.1 DSCSYS MT9
5.1.2	AP-F152A-MC	CZQRHAO RSX11M TEST SYSTEM DIAG.
5.1.3	AP-F146A-MC	CZQRVAO TEST SYS FOR RK05
5.1.4	AP-F147A-MC	CZQRCAO TEST SYS FOR RK06
5.1.5	AP-F148A-MC	CZQRDAO TEST SYS FOR RK07
5.1.6	AP-F149A-MC	CZQREAO TEST SYS FOR RP06
5.1.7	AP-F150A-MC	CZQRFAO TEST SYS FOR RM03
5.1.8	AP-F151A-MC	CZQRGAO TEST SYS FOR RL01
5.1.9	AC-F153A-MC	CZQRTAO RSX11M TEST SYS (DOC)
5.1.10	AC-F404B-MC	CZKCI RMT DIAG EXER (DOC)
5.1.11	AC-F405A-MC	CZKMP DPM50 DIAG MON (DOC)

6.0 SPECIAL INSTRUCTIONS:

6.1.1 RSX11-M must be running in the host system with DPM REMOTE DIAGNOSTICS KIT #ZP126-RD.

6.1.2 A serial line interface (ie. DLV11-F,DLV11-J) AND terminal will be required to run diagnostics in LOCAL MODE at the DYS23 subsystem. NOTE: These items are used for test only and are not shipped unless specifically ordered with the system.

6.1.3 The M8080 is always the last item on the bus with the exceptions that the M3084 always occupies slot 9, and that the optional BDV11-AA (M8012) always plugs into slot 8. (See Figure 1).

6.1.4 Verify that the cable dress is as shown in UA-DYS23-0 (NOTE 14). This is essential to meet FCC requirements.

6.1.5 Supported options (See NOTE below).

The basic DYS23 can be expanded within the initial DPM23 configuration by the addition of one BA11-NE, -NF expander box. The following peripherals are supported:

BDV11-AA	DIAGNOSTIC,BOOTSTRAP, TERMINATOR
DLV11-E	ASYNCHRONOUS LINE INTERFACE (IEAonly,full modem control)
DLV11-F	ASYNCHRONOUS LINE INTERFACE (EIA or20ma., no modem control)
DZV11-B	ASYNCHRONOUS MULTIPLEXER
KEF11-A	FLOATING POINT OPTION
LPV11-PA,-PD	LINE PRINTER OPTIONS
MSV11-DD	32KW MOS MEMORY(128KW MAX PER DYS23 SYS.)
MXV11-AC	MULTIFUNCTION MODULE
RXV21-DA,-DD	FLOPPY DISK OPTION (NON-DMA)

NOTE: When adding options,care must be taken to observe the backplane configuration rules of BA11-N enclosures;
particularly AC loading.

6.1.6 In order to run DCF11-AA diagnostic (CJKDB), LTC (Line Time Clock) interrupts must be disabled, to accomplish this jumper W4 must be installed on the KDF11-AA CPU module prior to testing. If a BDV11-AA (M8012) module has been added to the DYS23 system switchpack E21 #5 may be turned on instead. In iether case this procedure must be reversed prior to running D BUS I/O module diagnostic VPCA??. System must ship with LTC interrupts enabled. Refer to fig. 2.

7.0 INSTALLATION AND TEST SETUP INSTRUCTIONS:

7.1 Unpacking and inspection:

7.1.1 Save all packing material for equipment to be shipped that is not cab mounted.

7.2 MODULE CONFIGURATION SETUPS FOR DYS23:

7.2.1 KDF11-AA (M8186) LSE 11/23 CPU MODULE

JUMPER DESIGNATION	JUMPER STATE
W1	IN
W2	AS RECEIVED
W3	AS RECEIVED
* W4	OUT
W5	OUT
W6	OUT
W7	IN
W8 THRU W15	DON'T CARE
W16	IN
W17	IN
W18	IN

* = NOTE: See special instruction at 5.1.5

Reference FIGURE 2 for jumper locations.

7.2.2 MSVLL-DD (M8044-D?) FIRST 32K

S1 SWITCHPACK	SWITCH STATE
SW1	ON
SW2	ON
SW3	ON
SW4	ON

JUMPER DESIGNATION	JUMPER STATE
W2	IN
W3	IN
PIN 1 TO 3	IN
PIN 5 TO 7	IN
PIN 10 TO 14	IN
PIN 15 TO 16	IN

Reference FIGURE 4 for seitch and jumper locations.

7.2.3 DLV11-F (M8028) SERIAL LINE UNIT

JUMPER DESIGNATION	JUMPER STATE
T0	OUT
T1	IN
T2	OUT
T3	IN
R0	OUT
R1	IN
R2	OUT
R3	IN

THE DLV11-F IS DEFAULT JUMPERED FOR CONSOLE USE, BUT THE ABOVE BAUD RATE JUMPERS MUST BE RECONFIGURED FROM 110 BAUD OPERATION TO 300 BAUD.

THE DLV11-F IS NOT A STANDARD PART OF THE DYS23 SYSTEM, BUT IS A FREQIENT OPTION, AND IS NEEDED IN FA&T FOR DIAGNOSTIC TESTING IN LOCAL MODE. SEE FIGURE 5 FOR JUMPER LOCATIONS.

7.2.4 ISV11-B (M8080, M8084) DEC DATAWAY INTERFACE.

FACTORY CONFIGURED:

CSR ADDRESS	160140 160142 160144
VECTOR ADDRESS	300 304

JUMPERS	STATE	LOCATION
W1 THRU W6	OUT	M8080
W7 THRU W10	IN	M8080
W11 THRU W16	OUT	M8080
W17 THRU W20	IN	M8080
W21 THRU W23	OUT	M8080
W1,W3,W5,W7,W9	IN	M8084
W2,W4,W6,W8,W10	OUT	M8084

NOTE: If DLV11-J is installed in DYS23 system its default vector address of 300 must be reconfigured because of its conflict with the ISV11-B.

Reference FIGURES 6.1 and 6.2 for jumper locations.

TOTAL ACTIVE PASSES = 41, ACTIVE TERMINALS = 1, TIME=8:34

7.3 CABLING OF THE DYS23:

7.3.1 Cabling of the DYS23 consists of a serial bus cable (70-15928-03) coming from the M8084 board of the ISV11-B which interconnects with the DEC DATAWAY CABLE (70-14152) connecting to the HOST CPU'S ISB11.

8.0 POWER CHECKS:

8.1 +5vdc -+250mv
+12vdc -+600mv

The +5vdc and +12vdc regulated voltages can be measured at J7 of the backplane or, preferably at the tip jacks on the M8012 (BDV11-AA) module (if it has been added to the system). The pins of J7 are numbered, and color coded. +12vdc and +5vdc are assigned the following pins and colors.

+12vdc----------PIN 2, PURPLE WIRE
+12vdc GROUND---------PIN 3, BLACK WIRE
+5vdc----------PIN 5, RED WIRE
+5vdc GROUND---------PIN 4, BLACK WIRE

The tip jacks on the M8012 module are color coded and labeled as follows:

+12vdc----------J3, PURPLE
+5vdc----------J2, RED
GROUND----------J1, BLACK

If adjustment becomes necessary, remove the two power supply mounting screws to tilt the power supply forward exposing the adjustment potentiometers, R1 for +12vdc and R22 for +5vdc. Reference FIGURES 3.1 and 3.2 for locations.

9.0 DIAGNOSTIC TEST PROCEDURE:

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria; e.g. pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each indivedual diagnostic contained in the CHECKLIST.

The host processor, along with its ISB11's must be fully checked out according to mast prior to connecting a DYS23 to the DATAWAY.

9.1 DYS23 HOST SYSTEM BOOTING PROCEDURE:

9.1.1 Obtain a disk pack for the appropriate host media which has the RSX11-M package #AP-F152-MC and install it into DRIVE #0. Load DRIVE #0 and insure that "WRITE PROTECT" is off.

9.1.2 When DRIVE #0 is ready and "ON LINE" (heads loaded) BOOT the drive.

9.1.3 When the program asks for the date and time, you may either enter the information or default it by typing a carriage return. An ecample would be 08:30 04-JUN-81.

9.1.4 The program will continue setting up parameters and will ask: "Do you want to load IPG diagnostics from magtape [Y/N]:". Type in a carriage return which will default your answer to a NO condition.

9.1.5 The program will now output:
>@ <EOF> (This signifies end of file and parameters are now set) and waits for you to key in a command.

9.1.6 Type in:
Set /UIC=[200,270] (This may not be necessary if the UIC is already at 200,270.).

9.2 RUN THE ERROR REPORT TASK IN ORDER TO CLEAR OUT THE ERROR LOG.

9.2.1 >RUN ISBRPT----------TYPE:<RUN ISBRPT>
ISBRPT-DEC DATAWAY ERROR REPORT TASK
>
PRINT SUMMARY [Y OR N] ?N---------TYPE:<N>
PRINT ENTIRE FILE [Y OR N]?N------TYPE:<N>
DELETE ERROR FILE [Y OR N]?Y------TYPE:<Y>
ISBRPT...OPERATION COMPLETE
TASK "ISBRPT" TERMINATED
TASK EXIT WITH OUTSTANDING I/O
PC=125130
PS=170000
RC=120720
R1=125576
R2=125650
R3=000000
R4=143470
R5=000000
SP=120476

9.2.2 Type :<ctrl c> to terminate ISBRPT task and receive back MCR> prompt.

9.3 RUN THE DEC DATAWAY DIAGNOSTIC ECERCISER:

```
9.3.1 >RUN DZKC??-------------------------TYPE:<RUN DZKC??>
      DCP-A >STA--------------------------TYPE:<STA>
      # UNITS (D)? 1----------------------TYPE:<1>
      ENTER CONTROLLER NUMBER:(0)0?0------TYPE:<0>
      ENTER TERMINALS ON THAT CONTROLLER:
      (0) 1?1-----------------------------TYPE:<1>
      NUMBER OF ENTERED TERMINALS = 1

      UNIT**CONTROLLER**LOGICAL SB**LUN**
       001     000          001        011

TOTAL ACTIVE PASSES = 21, ACTIVE TERMINALS = 1, TIME = 8:33

9.3.2 After required run time has elapsed terminate running
      of diagnostic by typing <CTRL C>.

      TASK "TTO" TERMINATED
      TASK EXIT WITH OUTSTANDING I/O
      PC=046000
      PS=170000
      R0=000002
      R1=000000
      R2=000000
      R3=000000
      R4=000003
      R5=000001
      SP=001246
```

9.4 After DZKC has run, the error log must be checked for errors that may have occured during running.

```
9.4.1 >RUN ISBRPT-----------------------TYPE:<RUN ISBRPT>
      ISBRPT-DECDATAWAY ERROR REPORT TASK
      >
      PRINT SUMMARY [Y OR N]?Y------------TYPE:<Y>
      PRINT ENTIRE FILE [Y OR N]?N---------TYPE:<N>
      OUTPUT TO LINE PRINTER [Y OR N]?N----TYPE:<N>
      WANT ONE CONTROLLER [Y OR N]?N-------TYPE:<N>
      DELETE ERROR FILE [Y OR N]?N---------TYPE:<N>
      ISBRPT....ERROR FILE IS EMPTY
      ISBRPT....OPERATION COMPLETE
```

9.4.2 TYPE: <CTRL C> to terminate ISBRPT task and recieve back MCR> prompt.

9.4.3 Error reporting can be in the form of hard errors, typed out immediately, or soft errors; (Errors that are logged by the error logger). No errors are allowed.

9.5 RUN ROM RESIDENT TESTS OF ISV11-B

9.5.1 MCR> RUN CZKCI----------TYPE:<RUN CZKCI>
>
DCP-A>STA----------TYPE:<STA>
UNITS (D) ? 1----------TYPE:<1>

UNIT 1
ENTER CONTROLLER NUMBER:(0)0?0---TYPE:<0>
ENTER TERMINALS ON THAT CONTROLLER:
(D) 1?1----------TYPE:<1>

SELECTED SERIAL LINE PORTS

UNIT**CONTROLLER**LOGICAL SB**LUN**TYPE
1 0 001 9 DPM50-PORT 0

START OF TESTING

END OF PASS 0, TIME = 9:29

END OF PASS 1, TIME = 9:31

9.5.2 After required run time has elapsed terminate running of the diagnostic by typing <CTRL C>.

9.6 LOAD DIAGNOSTIC MONITOR CZKMP

9.6.1 >RUN CZKMP----------TYPE:<RUN CZKMP>
>
CZKMPB VERSION 2.2
SELECT MODE: LOCAL, HOST, AUTO-MAP, COMMUNICATION OR
EXIT (L,H,A,C,E)L ----------TYPE:<L>
ENTER NUMBER OF TERMINALS [D]=1-----TYPE:<1>
ENTER CONTROLLER NUMBER [0]=0-------TYPE:<0>
ENTER TERMINAL NUMBERS [0]=1--------TYPE:<1>
NUMBER OF INTERED TERMINALS =1
UNIT**CONTROLLER**LOGICAL SB**
1 0 1

At This point the console terminal at the DYS23 subsystem comes on line and is used to ask and run subsystem diagnostics.

9.7 RUN 11/23 CPU AND MEMORY DIAGNOSTICS ON DYS23

See appendix A for ecplanation of monitor interaction inputs and outputs at local DYS23 terminal.

9.7.1 >JKDAC----------TYPE:<JKDAC>
157776
@200G----------TYPE:<200G>
CJKDACO KTF11-AA MMU DIAG.
SWR=000000 NEW=CR----------TYPE:<CR>

END PASS# 1 ;TOTAL ERRORS SINCE LAST START AT 200 0

9.7.2 After required run time has elapsed, terminate running of the diagnostic at the DYS23 console terminal by depressing the <BREAK> key.

9.7.3 @760144/000000 2----------TYPE:<760144/>
TYPE:<2>
>JKDBC----------TYPE:<JKDBC>
157776
@200G----------TYPE:<200G>
CJKDEC DCF11-AA CPU DIAGNOSTIC
END PASS# 1
END PASS# 15

NOTE: LTC interrupts must be disabled to run diagnostic JKDBC. See special instruction at 5.1.5.

9.7.4 After required run time has elapsed, terminate running the diagnostic at the DYS23 console terminal by depressing the <BREAK> key.

9.7.5 @760144/000000 2----------TYPE:<760144/2>
>ZQMCG----------TYPE:<ZQMCG>
157776
@200G----------TYPE:<200G>
SWR = 000000 NEW = CR ----------TYPE:<CR>

KT11 (MEMORY MANAGEMENT) AVAILABLE

MEMORY MAP
FROM 000000 TO 757777 (WITH 4 MSV11-D INSTALLED)
NO PARITY REGISTERS FOUND
PROGRAM RELOCATED TO 720000
PROGRAM RELOCATED TO 000000
END PASS# 1

Above will be received when 4 MSV11-D modules are installed, typeouts will vary with lesser amounts of memory. No relocation will occur when only 1 MSV11-D is installed.

9.7.6 # NOTE: The following two tests are to be run if the optional KEF11 chip is installed.

9.7.7 @760144/000000 2----------TYPE:<760144/2>
>JKDCB----------TYPE:<JKDCB>
157776
CJKCB, KEF11-A FP DIAGNOSTIC PART 1

SWR = 000000 NEW = CR----------TYPE:<CR>

END PASS # 1
END PASS # 2

9.7.8 After required run time has elapsed, terminate running of the diagnostic at the DYS23 console terminal by depressing the <BREAK> key.

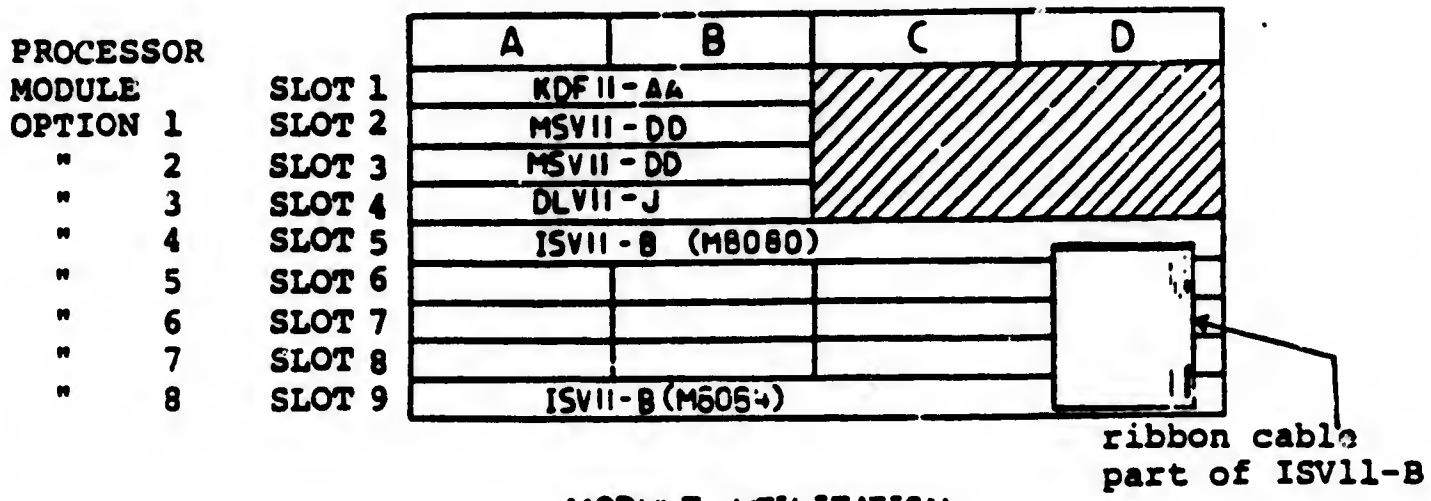
9.7.9 @760144/000000 2----------TYPE:<760144/2>
>JKDDB----------TYPE:<JKDDB>
157776
@200G----------TYPE:<200G>
CJKDDB DEF11-A DIAGNOSTIC PART 2

SWR = 000000 NEW = CR----------TYPE:<CR>

END PASS # 1
END PASS # 2

9.7.10 After required run time has elapsed, terminate running of the diagnostic at the DYS23 console terminal by depressing the <BREAK> key.

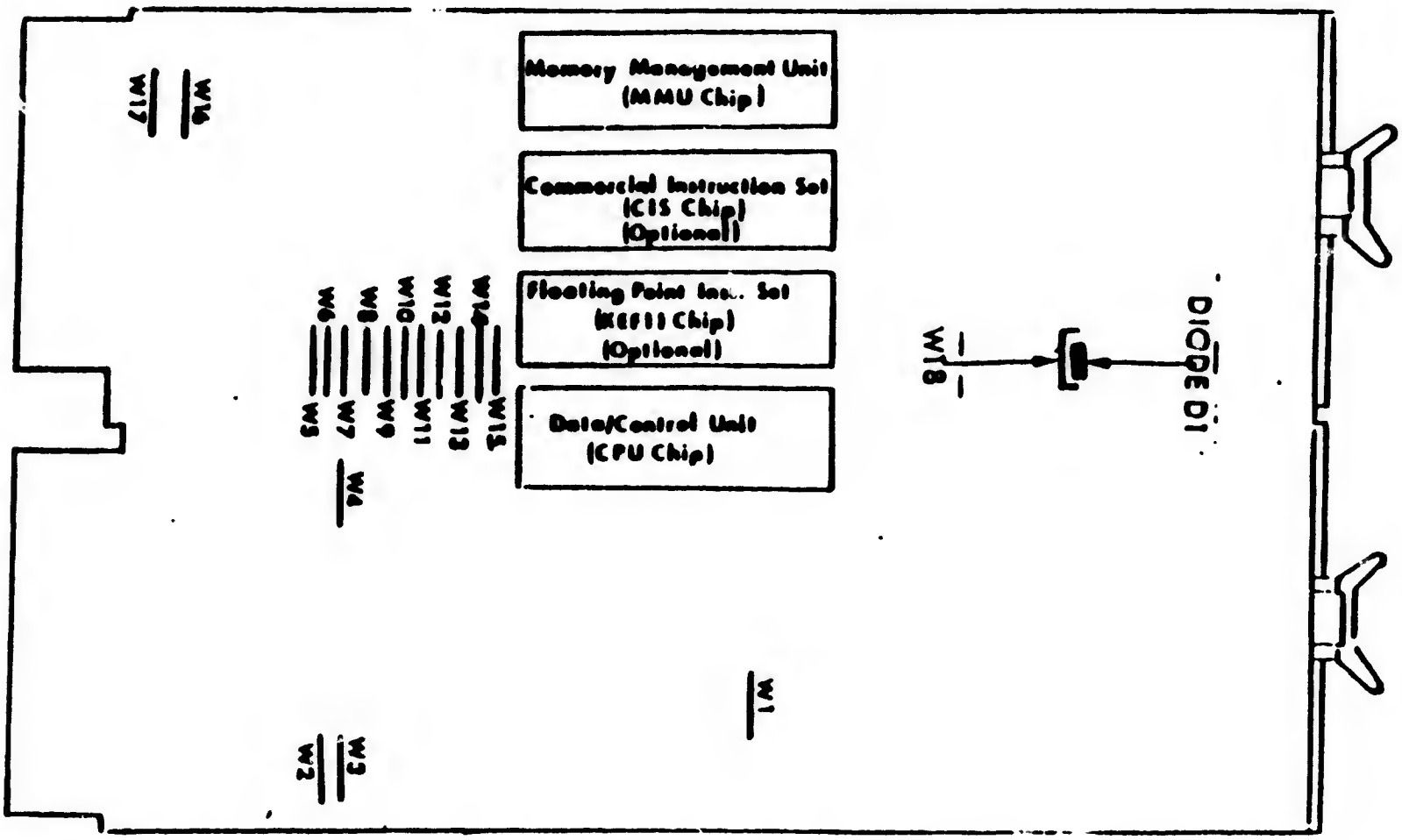
9.7.11 Load and run diagnostics for any additional LSI option modules installes, using same method used to run the CPU tests.



MODULE UTILIZATION

KERNEL DYS23 ONLY
(H9273-A)

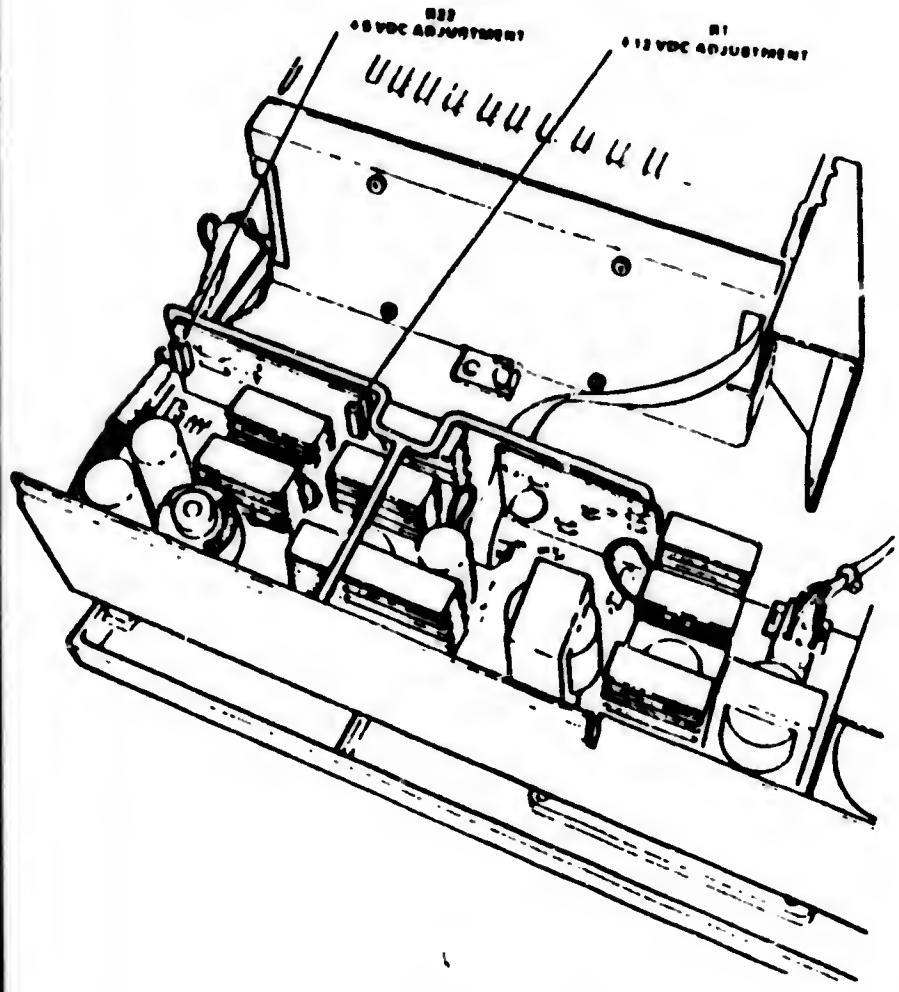
FIGURE 1 KERNEL SYSTEM BACKPLANE CONFIGURATION



KDF11-AA

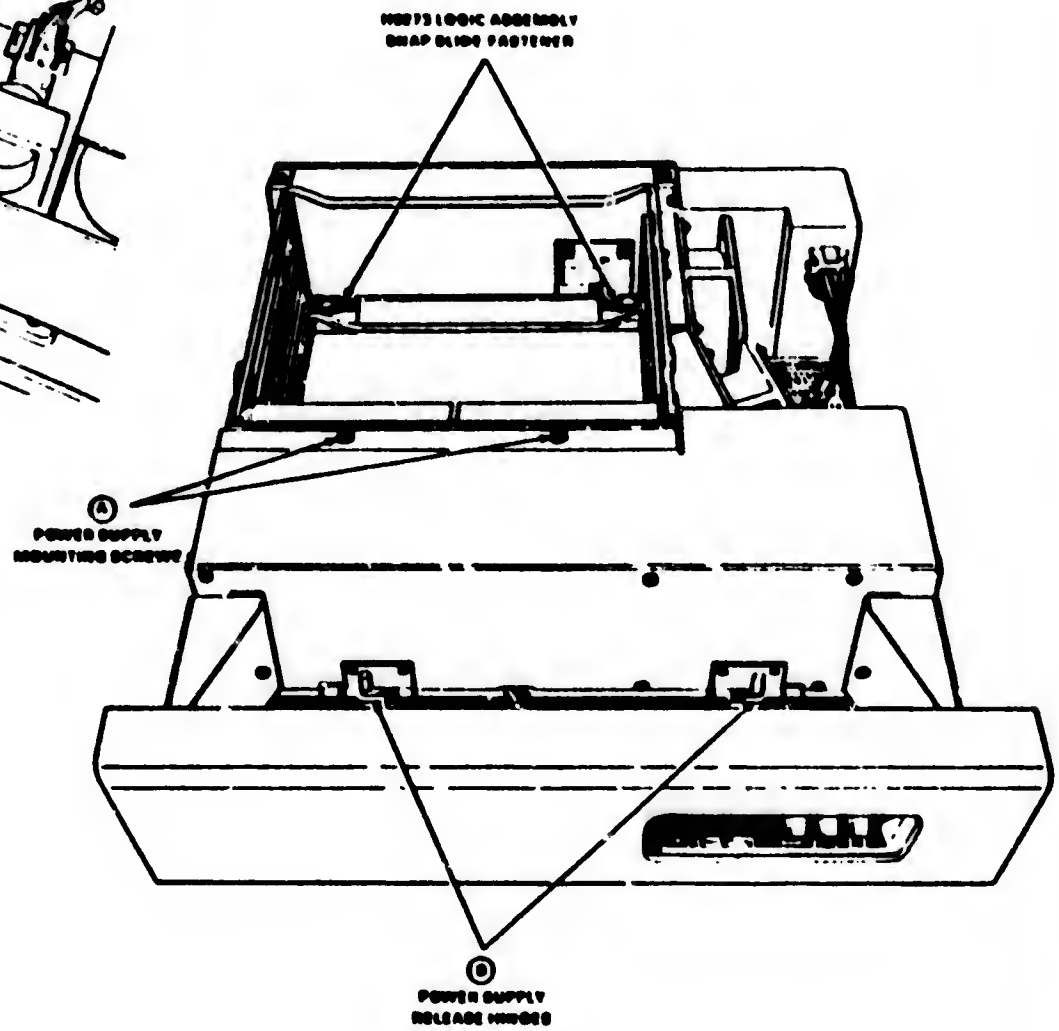
(M8186 11/23 CPU)

FIGURE 2.



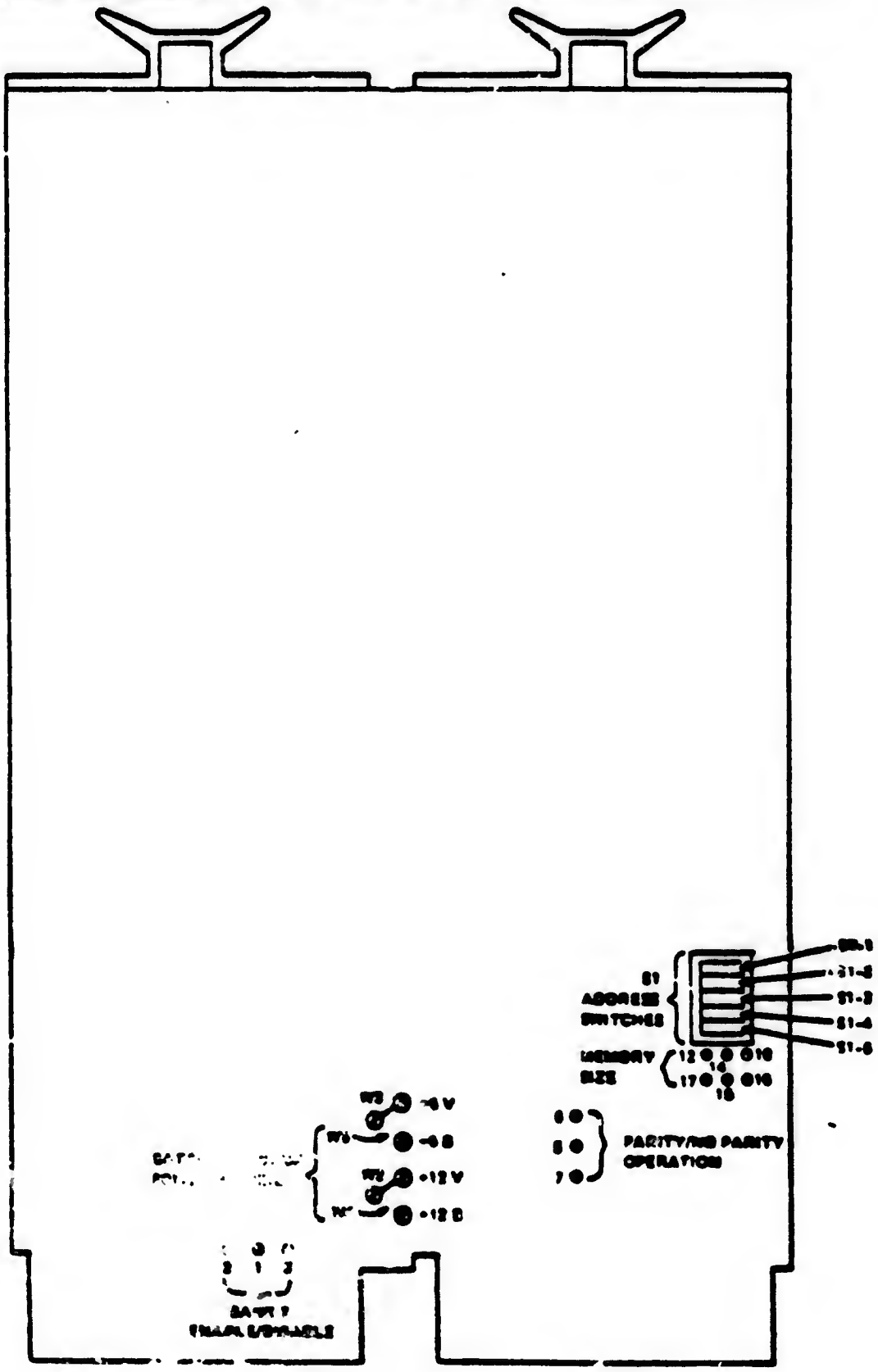
Power Supply Adjustments

FIGURE 3.2



Power Supply Assembly

FIGURE 3.1



MR 14-D?

Figure 4 MSV11-D, MSV11-E Switch and Jumper Locations

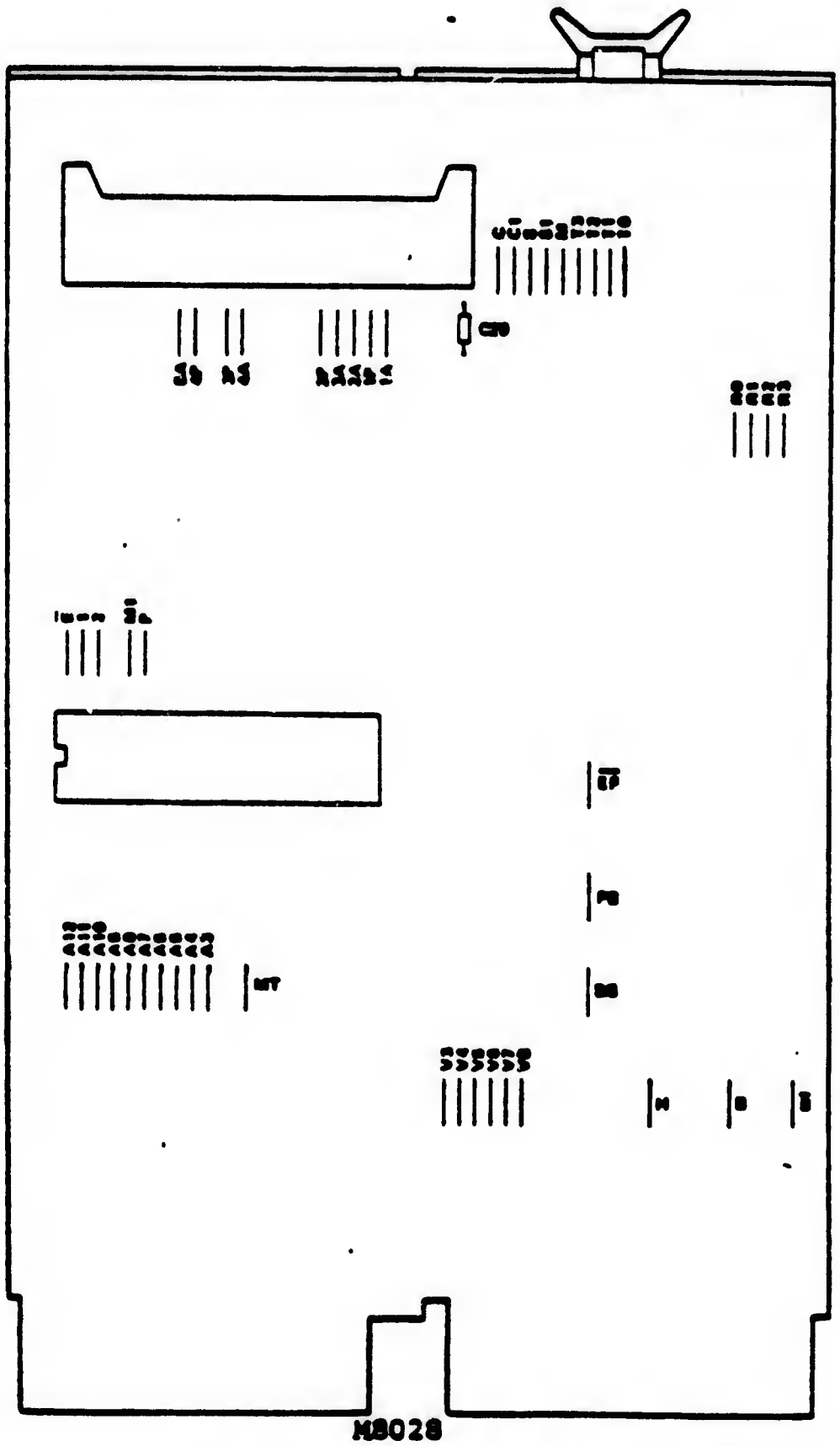
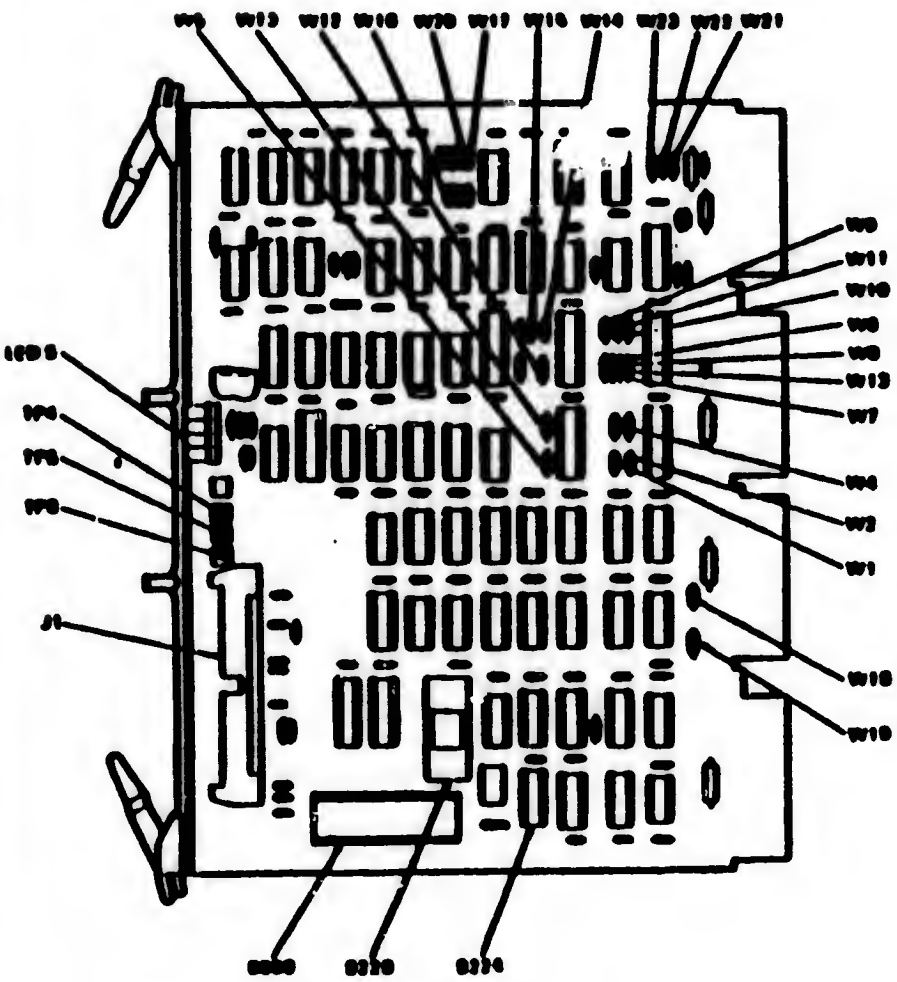


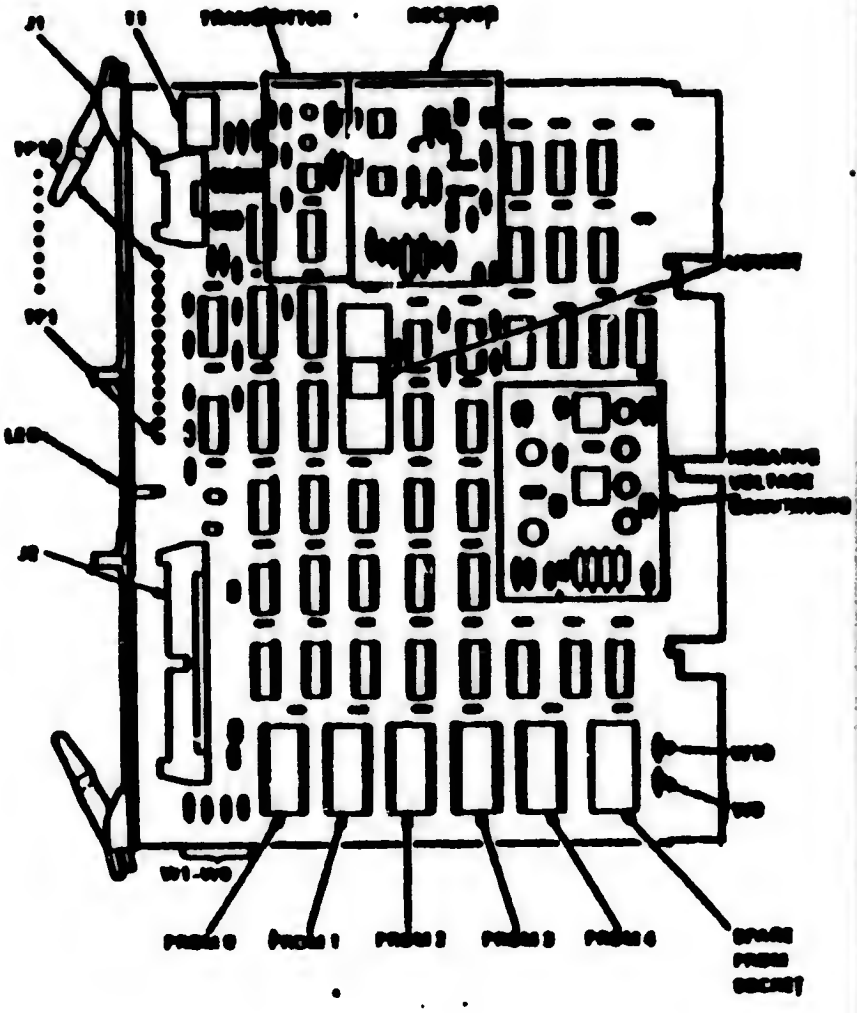
Figure 5 DLV11-F Jumper Locations



M8080

ISV11B

FIGURE 6.1



M8084

FIGURE 6.2

APPENDIX

MONITOR INTERACTION AT LOCAL TERMINAL

Prompts

	Operator may enter file name to call next diagnostic, or type control Z to put LSI-11 in ODT mode.
@	If following 157776 after a file name has been entered, indicates the diagnostic is in the LSI-11 and the operator may communicate with it via ODT.
	If following "End Pass" and the current PC, indicates the operator may give further instructions in ODT. Giving "760144" reestablishes communication with local monitor.

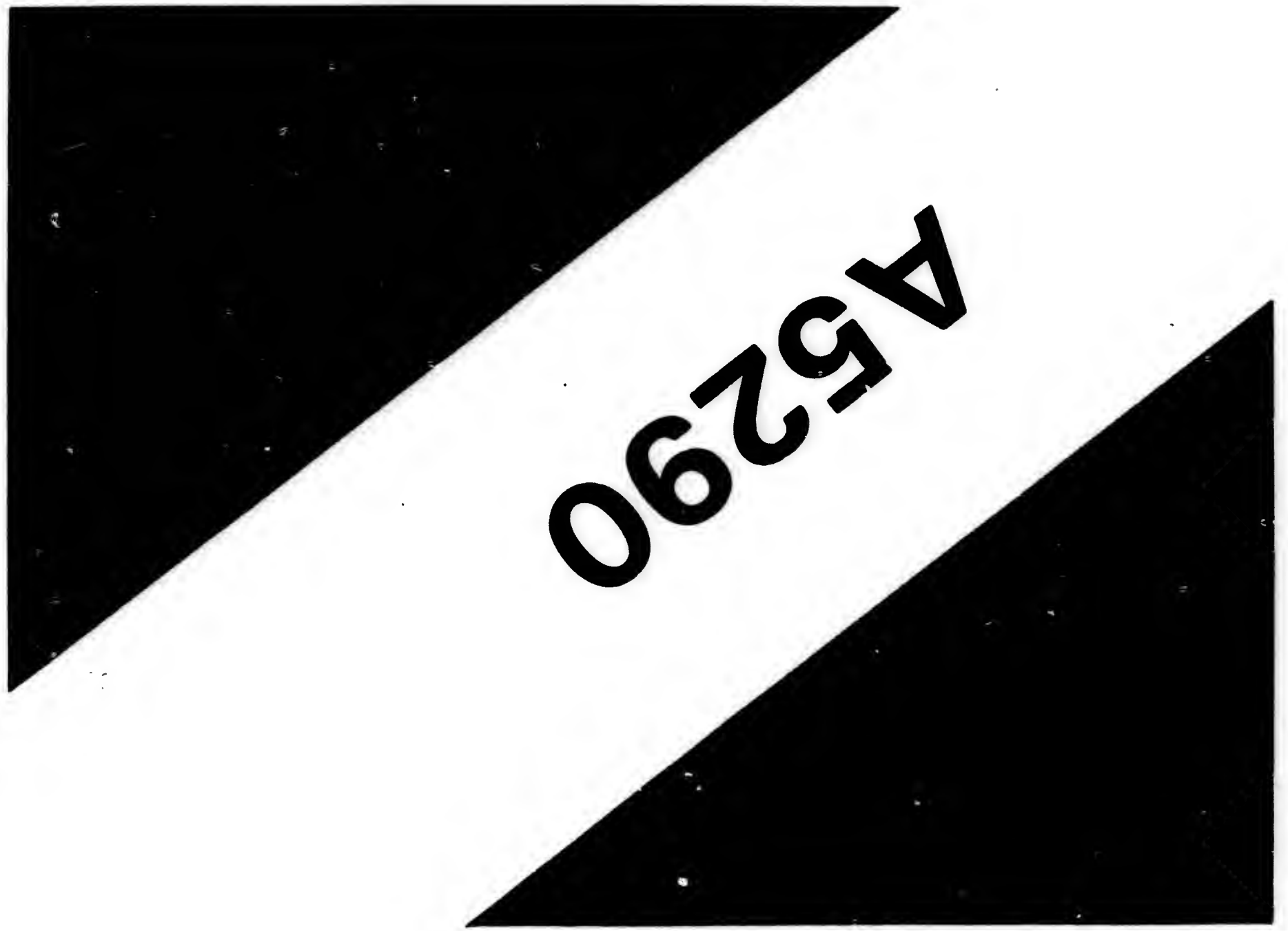
Inputs

File names	Used following " " to call diagnostics.
200G	Not to monitor - starts diagnostic if LSI-11 is in ODT.
Break	Not to monitor - stops diagnostic.
760144/	Reestablishes communication with local monitor if LSI-11 is in ODT.
Deposit 2	Following "000000" tells monitor that operator wishes to run another diagnostic.
Deposit 1	Follow "000000" aborts monitor in host. This is the last input by the operator.
Control Z	Following " " puts LSI-11 in ODT.

Outputs

157776	Following file name entry indicates the diagnostic has been downloaded.
NX	The requested file cannot be found.
BDLD	The attempt to download the diagnostic was unsuccessful.
END PASS	Diagnostic has completed a pass.
Current PC	Following break indicates diagnostic has stopped at address printed.
000000	Following "760144" indicates operator may input further instructions to local monitor (1 or 2).
EX	Monitor has terminated at host.

FIGURE 6


A52290

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DMC11 COMMUNICATIONS INTERFACE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	Prev. 7668001-0-5290					

ENG	APPD	SIZE	CODE	NUMBER	REV
Brent MacAlonpy	Tom Jalovecky	A	SP	MAA5290-0-0	C

EN-01083-16-NOV-(192)

DMC11 COMMUNICATIONS INTERFACE

1.0 INTRODUCTION

This procedure establishes the minimum test standards that a DMC11 must meet to be considered acceptable for customer shipment. The DMC11 consists of two (2) hex modules. The microprocessor modules: DMC11-AA, -AR, -AL execute communication protocol microcode held in CROM and interface with the Unibus, and the associated Line Unit module. The main function of the Line Unit modules: DMC11-DA, -FA, -MA, -MD is to perform parallel to serial data conversion to the external data communications line.

1.1 DMC11 kits consist of the following basic harware:

Microprocessor Modules

Option	Contents	Description	Prerequisite
DMC11-AA	M8200	Microprocessor without CROM	PDP-11
DMC11-AR	M8200-YA	Microprocessor module w/remote DDCMP CROM (use w/M8201 low speed line unit)	PDP-11
DMC11-AL	M8200-YB	Microprocessor module w/local DDCMP CROM (use w/M8202 high speed line unit)	PDP-11

Line Unit Modules

DMC11-DA	M8201 BC05-C BC08-S H325	Low speed line unit module w/EIA interface cable for remote connections	DMC11-AR
DMC11-FA	M8201 BC08-S BC05-Z H3250	Low speed line unit module w/ V.35/DDS interface cable for remote connection	DMC11-AR

1.1 cont.

Option	Contents	Description	Prerequisite
DMC11-MA	M8202-YA BC08-S 12-12528	1M baud line unit module w/integral modem for local connections	DMC11-AL
DMC11-MD	M8202-YD BC08-S 12-12528	56K baud line unit module w/integral modem for local connections	DMC11-AL

2.0 REFERENCE DOCUMENTATION

2.1 DMC[illegible]roprocessor Maintenance Manual - EK-DMCMP-MM-001 (for DMC11-AA, -A[illegible])

2.2 DMC11 Synchronous Line Unit Maintenance Manual - EK-DMCLU-MM-001 (for DMC11-DA, -FA, -MA, -MD)

2.3 DMC11 Field Maintenance Print Set MP00076

2.4 DMC11 Option/System Test Procedure A-SP-DMC11-O-5

2.5 Diagnostic Lib Kit ZJ216-RB

3.0 REQUIRED TEST EQUIPMENT

3.1 PDP11 with minimum of 8K and two or more hex SPC slots.

3.2 SPC must be DD11-C, DD11-D, DD11-B (Rev. "E" or later) or equivalent.

3.3 SPC must provide +5, +15, -15 volts and the power requirements will be:

Module	+5 (±5%)	+15 (±5%)	-15 (±5%)
M8200	5.0A	-	-
M8201	3.0A	0.03A	0.31A
M8202	3.0A	0.18A	0.46A

3.4 Oscilloscope and probe baud width 200 MHz or better.

3.5 Frequency counter (minimum range 25 KHz to 1100 KHz ± one percent)

4.0 AVAILABLE DIAGNOSTIC PROGRAMS - Kit ZJ216-RB

4.1 MAINDEC-11	Description
DZDMC	Basic Microprocessor test; i.e. for M8200. Does not test CROM or require a line unit.
DZDME	DDCMP Line Unit Test; i.e. for M8201, M8202. Requires an M8200 and should have a turnaround connector.
DZDMF	Bit-stuff line unit test; i.e. for M8201, M8202. Tests the Bitstuff mode of operation of the line unit. Requires an M8200 and should have a turnaround connector.
DZDMG	CROM microcode check, and jump test on M8200-YA, -YB microprocessors.
DZDMH	Free running DDCMP tests on microprocessors and corresponding line units.
DMCA	DECX/11 module.

5.0 INSTALLATION INSTRUCTIONS

5.1 M8200 Microprocessor - Before installing, remove the npr continuity wire that runs between pins CA1 and CB1 on the backplane for the slot that is going to accept the M8200. If a system change requires removal of the M8200, the wire must be replaced.

5.2 M8200 Microprocessor with local line units (DMC11-MA or DMC11-MD). This configuration must be placed on the unibus closest to the PDP11 processor and before the first bus buffer because of the high rate of npr transactions.

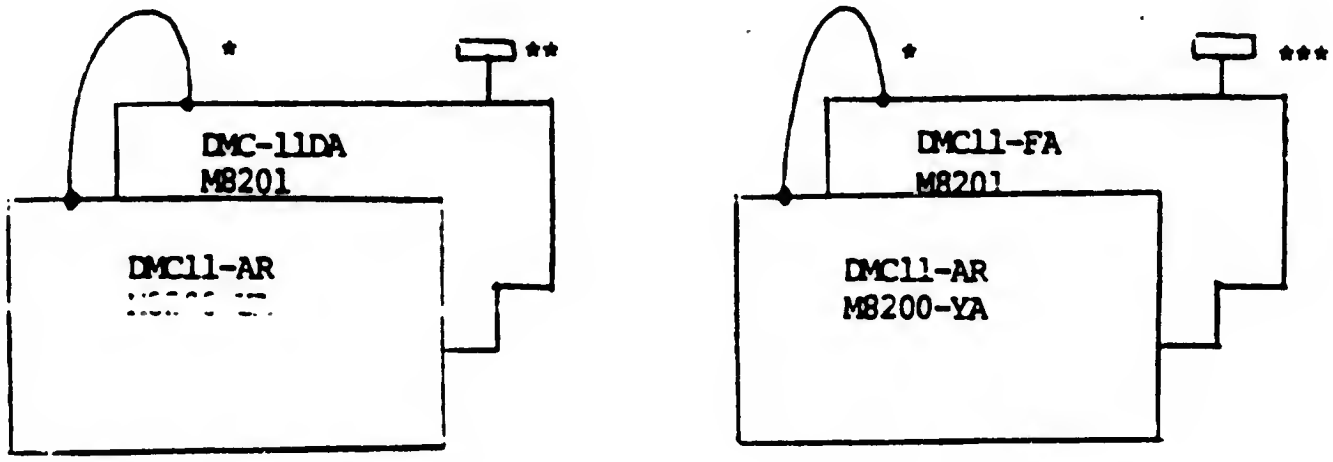
6.0 TEST SET UPS

6.1 A DMC11-AA cannot be tested until a verified set of CROM's from an -AR or -AL is temporarily inserted and then the -AR or -AL tests run.

6.2 A DMC11-AR or -AL can be tested by running DZDMC and DZDMG. Preferably, a line unit should be connected and DZDME, DZDMF and DZDMH run.

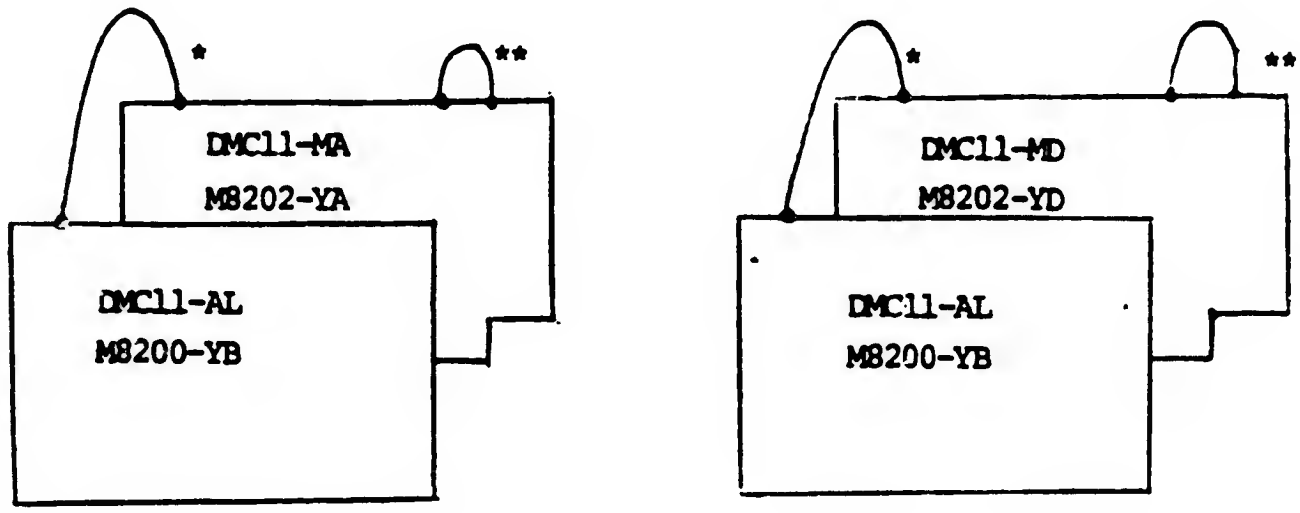
6.3 A DMC11-DA or DMC11-FA low speed line unit can only be tested via a fully operational DMC11-AR microprocessor. Diagnostics DZDME, DZDMF, DZDMH must be then run. See Figure 1.

Figure 1: Low Speed Line Unit Setup
* BC08Sconnector
** BC05C + H325
*** BC05Z + H3250



6.4 A DMC11-MA or DMC11-MD high speed line unit can only be tested via a fully operational DMC11-AL microprocessor. Diagnostics DZDME, DZDMF, and DZDMH must then be run. See Figure 2.

Figure 2: High Speed Line Unit Setup
* BC08S
** 12-12528



7.0 POWER CHECKS

7.1 Refer to Section 3.3 for power requirements.

7.2 Unibus loading - The M8200 microprocessor presents one unibus load. The M8201 and M8202 line units present no unibus loads.

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 As a general statement on the test procedure:

8.1.1 Determine which diagnostics to run from the test setup section.

8.1.2 Obtain switch, address and jumper settings from the diagnostic listing, or Option Test Procedure.

8.1.3 The MAST Checklist gives the count required.

8.1.4 No errors are acceptable.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KMC11-A GENERAL PURPOSE MICROPROCESSOR - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5296					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelavich		A	SP	MAA5296-0-0	A

KMC11-A GENERAL PURPOSE MICROPROCESSOR

INTRODUCTION

This procedure establishes the minimum test and electrical standards that a KMC11-A must meet to be considered acceptable for customer shipment. KMC11 kits consist of the following basic hardware:

Option	Designation	Contents
KMC11-A	general purpose micro processor	M8204

1.0 REFERENCE DOCUMENTATION

1.1 Print set MP00339

1.2 Maintenance Manual EK-KMC11-MM-REV

1.3 Users Manual A-KMC11-OP-REV

1.4 Test/Acceptance Procedure A-SP-KMC11-0-5

1.5 Lib Kit ZJ-234-RB

2.0 REQUIRED TEST EQUIPMENT

2.1 PDP11 with minimum of 8K and two or more slots

2.2 SPC must be DD11-C, DD11-D or equivalent

2.3 SPC should provide +5, +15, -15

2.4 Oscilliscope & probe band width 200MHz minimum or better.

NOTE: Refer to the KMC11 test and Acceptance Procedures for further information.

3.0 AVAILABLE DIAGNOSTIC PROGRAMS Kit #ZJ-234-RB

Maindec	Description
DZKCC	Static Test, M8204 Data Path Test
DZKCD	Static Cram & Branch Test (M8204)
DZKCA	Free run, M8204 Data Path Test
* DZKCE	DDCMP Line Unit Test
* DZKCF	Bit Stuff Line Unit Test
* DZKCG	M8204 Plus Line Unit Free Run Test
KMAA	DEC/X11 System Test

* NOTE: These diagnostics are only used when customer has ordered an optional DMC11 line unit cabled to the KMC11. (DA, FA, MD, MA)

4.0 INSTALLATION INSTRUCTIONS

4.1 M8204 Microprocessor

Before installing, remove the NPR grant continuity wire, that runs between pins CA1 and CB1 on the backplane, for the slot that is going to accept the M8204. If a system change requires removal of the M8204, this wire must be replaced.

4.2 M8204 Microprocessor with local line units (DMC11-MA or DMC11-MD).

In addition to item "A", the configuration must be placed on the Unibus closest to the PDP-11 processor and before the first bus buffer, because of the high rate of NPR transactions that are required.

5.0 TEST SET UP

5.1 No special test set-up is required.

6.0 POWER CHECKS

6.1 The KMC utilizes five amperes of plus five volts per M8204 module. Care should be exercised that any test stand or system installation considers the maximum current per regulator. If the DMC line units are used, their requirements are:

MODULE	+5	+15	-15
M8201	3.0A	0.03A	0.31A
M8202	3.0A	0.18A	0.46A

6.2 Unibus Loading

The M8204 presents one Unibus load if a DMC line unit is used. The Line Unit presents no load to the Unibus.

7.0 DIAGNOSTIC TEST PROCEDURE

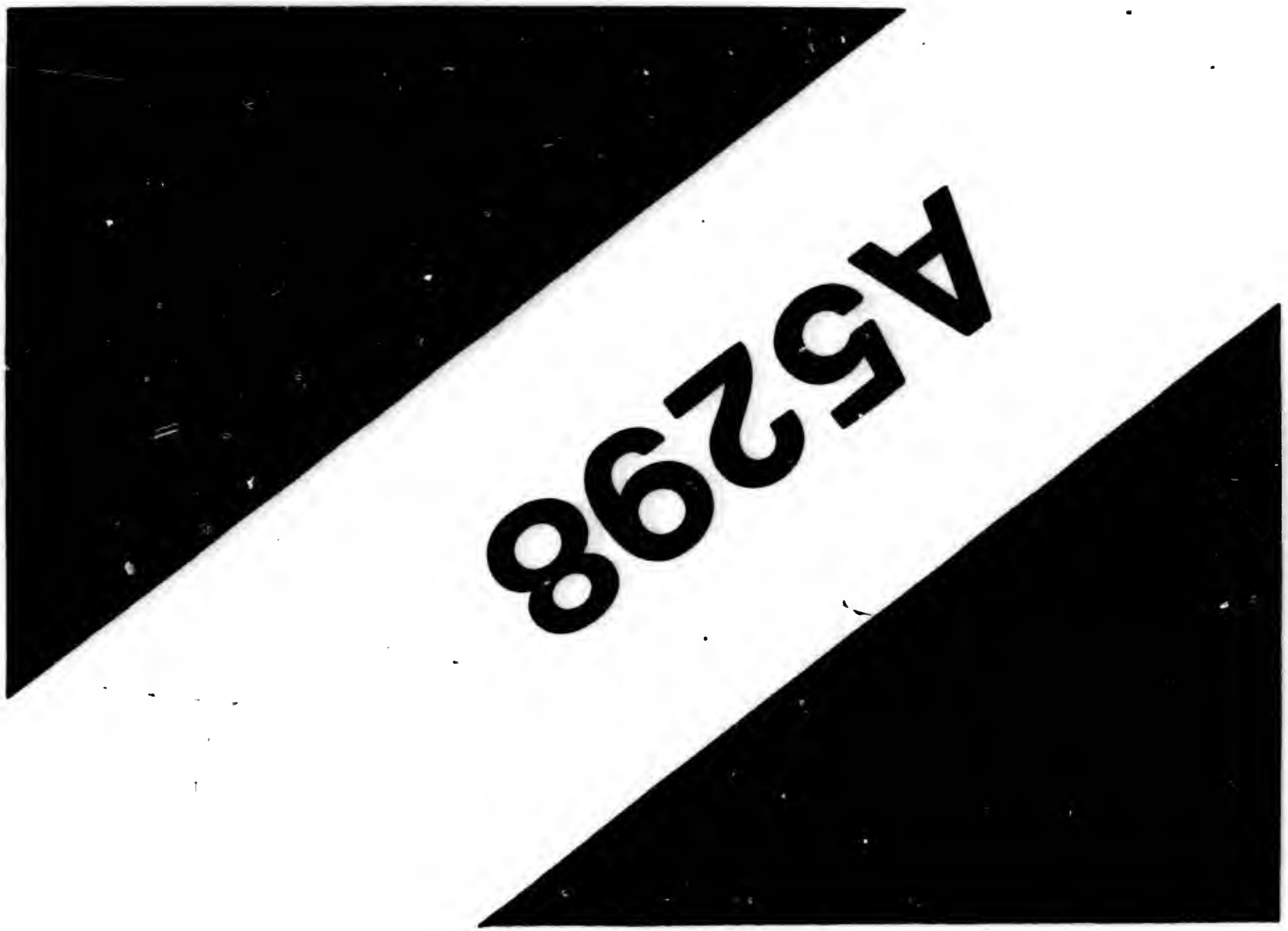
7.1 See Section 3.0 for order of diagnostics. The following procedure is used for all diagnostics.

7.1.1 Load diagnostic.

7.1.2 Load address at 200.

7.1.3 Set switch 15 up and all other switches down. Start program.

7.1.4 End of Pass will be shown by type out.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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 3/18/81

TITLE M.A.S.T. DMR11

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	GENERAL UPDATE TO INCLUDE H/E PRODUCIBILITY STUDY FINDINGS	1 ML013	D. Ayotte	3/18/8		

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Ayotte	Bob Beck	A	SP	MA-A5298-0-0	B

DMR11

1.0 INTRODUCTION

The DMR11 is a micro-processor based intelligent synchronous communications controller, which employs the Digital Data Communications Message Protocol (DDCMP). The DMR11 is designed to be used in a network link for high performance interconnection of VAX-11 or PDP-11 computers. The DMR11 is program compatible with the DMC11 and line compatible with either the DMC11 or any device that uses DDCMP version 4.0.

2.0 REFERENCE DOCUMENTATION

2.1 Manuals & Engineering Specifications

2.1.1	DMR Synch. Cont. Tech. Man.	EK-DMR11-TM
2.1.2	M8207 Microprocessor Manual	EK-M8207-TM
2.1.3	M8203 Line Unit Manual	EK-M8203-TM

2.2 Prints and Schematics

2.2.1	DMR11 Print Set	MP00911

3.0 REQUIRED TEST EQUIPMENT

3.1 Hardware and Media

3.1.1 PDP-11 CPU with a Console Terminal and a minimum of 16K bytes of memory.

3.1.2 Scope - stable at 1 microsecond on X10 scale, Tektronics 465 or equivalent

3.1.3 DVM - accurate to .1 volts at 15 volts

3.1.4 H3250 Cable Test Connector for BC05Z V.35 Cable.

3.1.5 H3254 Module Test Connector for J1 of M8203

3.1.6 H3255 Module Test Connector for J2 on the M8203.

3.1.7 H3251 Cable Test Connector for BC55B, BC55C, and BC55D Cables.

3.1.8 H325 Cable Test Connector for BC55C and BC05D Cables.

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 CZDMP .... M8207 STATIC DIAGNOSTIC I

4.2 CZDMQ .... M8207 STATIC DIAGNOSTIC II

4.3 CZDMR .... M8203 STATIC DIAGNOSTIC I

4.4 CZDMS .... M8203 STATIC DIAGNOSTIC II

4.5 CZDMI .... DMR11 FUNCTIONAL DIAGNOSTIC

4.6 DZFLA .... FLOAT PROGRAM

5.0 SPECIAL INSTRUCTIONS

The DMR11 basic unit consists of the M8207-RA microprocessor and the M8203 line unit. This line unit/microprocessor combination permits either remote or local computer applications. Refer to Figure 1 for a typical PDP-11 application.

The DMR11 basic subsystem has four options which allow it to accommodate standard and special interface configurations. With these options, DMR11 systems can operate with speeds ranging from 2.4K bits per second (B/S) to 1M B/S. Refer to Table 1.

TABLE 1 ---- DMR11 OPTIONS

OPTION	INTERFACE	LINE SPEED
DMR11-AA	EIA RS232C	UP TO 19.2K B/S
	EIA RS423	UP TO 56K B/S
DMR11-AB	ISO/CCITT V.35	UP TO 1M B/S
DMR11-AC	INTEGRAL MODEM	56K, 250K, 500K, 1M B/S
DMR11-AD	BASIC	***** SEE BELOW FOR DETAILS ****
DMR11-AE	EIA RS422	UP TO 1M B/S

***** DMR11-AD *****

The Basic Subsystem is designated DMR11-AD and consists of an M8203 Line Unit, an M8207-RA Microprocessor, a BC08S-1 Interconnect Cable, an H3254 Interface Module Test Connector, and an H3255 Interface module Test Connector. The M8203 Line Unit has an Integral Modem which is switch selectable to operate at speeds of 56K, 250K, 500K, and 1M B/S.

5.1 Special Switch Considerations

5.1.1 If the DMR11 is to be used in conjunction with a DMC11 or with DMC11 software, ensure that Switch Pack E121 switch 9 on the M8203 Line Unit module is in the "OFF" position. Refer to Figure 3.

5.1.2 If the DMR11 is operating at a speed of 56K or greater, ensure that Switch Pack E121 switch 10 of the M8203 Line Unit module is in the "OFF" position. Refer to Figure 3.

5.1.3 If Micro-diagnostics are desired on initialization of the device, set Switch Pack E134 switch 10 on the M8203 Line Unit module to the "OFF" position. Note: This switch should be in the ON position (MICROs DISABLED) so device will be compatible with DMC11 software. Refer to Figure 3.

6.0 INSTALLATION AND TEST SET-UP INSTRUCTIONS

6.1 M8207-RA Module Set-Up

6.1.1 Run the FLOAT PROGRAM (DZFLA) on a PDP11 system to determine the Address and Vector assignment of the M8207-RA Microprocessor. Refer to MA-A3000 for additional information.

6.1.2 The Address of the DMR11 can be set via Switch Pack E127 on the M8207-RA module. (See Figure 2 for module lay-out) Refer to Table 2 for the correlation between switch number and address bit. Note that a switch in the "OFF" position will respond to a logical "ONE" on the Unibus.

6.1.3 The Vector of the DMR11 can be set-up via Switch Pack E28 on the M8207-RA module. (See Figure 2 for module lay-out) Refer to Table 3 for the correlation between switch number and vector bit. Note that a switch "ON", responds to a logical "ONE" on the Unibus.

6.1.4 Ensure that the following switches on the M8207 module are in the correct position: (Refer to Figure 2)

A. RUN INHIBIT - M8207 SWITCH E28-7 -- always ON

B. CSR INHIBIT - M8207 SWITCH E28-8 -- always OFF

C. BYTE SELECT/LOCKOUT (BST) - M8207 SWITCH E85-1 Normally ON

6.1.5 Verify that the M8207-RA Priority Plug is a BR5 and is installed correctly in location E77.

6.1.6 Verify that M8207-RA Jumpers W1 and W3 are installed. Reference Figure 2 for Jumper location.

SWITCH PACK E127 - DEVICE ADDRESS SELECTION

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	SWITCH PACK E127										0	0	0

SWITCH NUMBER	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	DEVICE ADDRESS
										off	760010
									off		760020
									off	off	760030
								off			760040
								off		off	760050
								off	off		760060
								off	off	off	760070
							off				760100
											------
						off					760200
											------
						off	off				760300
											------
					off						760400
											------
					off		off				760500
											------
					off	off					760600

NOTE: SWITCH OFF RESPONDS TO A LOGICAL ONE ON THE UNIBUS

SWITCH PACK E127
DEVICE ADDRESS
SELECTION

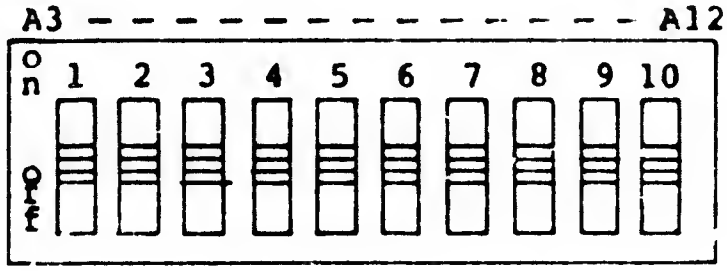


TABLE 2

SWITCH PACK E28 - VECTOR ADDRESS SELECTION

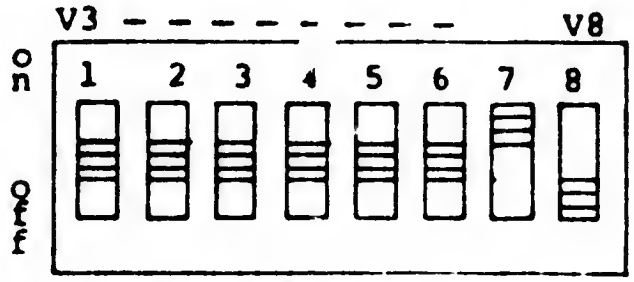
MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SWITCH PACK E28						0/1	0	0

NOTE: Switch "ON" produces a logical ONE on the Unibus.

SWITCH #	S6	S5	S4	S3	S2	S1	Vector address
		on	on				300
		on	on			on	310
		on	on		on		320
		on	on		on	on	330
		on	on	on			340
		on	on	on		on	350
		on	on	on	on		360
		on	on	on	on	on	370
	on						400
							---
	on		on				500
							---
	on	on					600

SWITCH PACK E28



vector address selection
*run inhibit
*csr disable

TABLE 3

6.1.7 Carefully insert the M8207-RA module into the selected SPC slot as per configuration sheets.

6.1.8 Remove the NPR GRANT wire (NPG) from the selected SPC backplane slot. (Wire CA1 to CB1)

6.2 M8203 Line Unit Set-Up

6.2.1 Ensure that Switch Packs E39, E121 and E134 on the M8203 module are set-up for the appropriate variation. Refer to Figure 3.

SWITCH PACK E39

SW1-4 ..... OFF
SW5-7 ..... see Table 4
SW8-10 ..... see Table 5

TABLE 4

	INTERFACE TYPE	5	6	7
AA	423/232C	OFF	OFF	OFF
AB	V.35	ON	OFF	OFF
AC	MODEM	OFF	OFF	OFF
AD	BASIC	OFF	OFF	OFF
AE	422	OFF	OFF	ON

NOTE - To select INTEGRAL MODEM, plug the BC55A in J1 (J2 is empty).

TABLE 5

SPEED SELECT

INTERFACE TYPE		8	9	10	SPEED
AA	423/232C	OFF	OFF	ON	56KB
AB	V.35	ON	ON	ON	1MB
AC	MODEM	ON	ON	ON	1MB
AD	BASIC	ON	ON	ON	1MB
AE	422	ON	ON	ON	1MB

SWITCH PACK E121 - Refer to Figure 3.

SW1-8 .... ON ..... BOOTSTRAP OFFSET
SW9 ..... OFF ..... DMC LINE COMPATIBLE
SW10 ..... OFF* .... HIGH SPEED

* - "ON" only for speeds less than 56KB

SWITCH PACK E134

SW1-8 ..... OFF ..... BOOTSTRAP PASSWORD
SW9 ..... OFF ..... AUTO ANSWER
SW10 ..... ON ..... DISABLE MICRO'S

6.2.2 Carefully insert the M8203 Line Unit module into the proper backplane slot (adjacent to the M8207-RA Microprocessor).

6.2.3 Connect the Line Unit to the Microprocessor using a BC08S-1 cable. One end of the cable is connected to J1 of the M8207-RA microprocessor module and the other end to J3 of the M8203 line unit module. Fold the cable back to the right, tightly against the component side of either the microprocessor or line unit module, so as to fit it into the mounting box. Refer to Figure 4.

6.2.4 Insert the module test connectors into J1 and J2 of the line unit as shown in Figure 4. Be sure to insert them with "SIDE 1" (etched on the test connector) visible from the component side of the line unit.

6.2.5 NOTE - FOR CZDMI FUNCTIONAL DIAGNOSTIC ONLY. Connect the appropriate Interface Cable and Test Connector to the correct Line Unit Connector as specified in Table 6. Reference Figures 5 thru 8.

TABLE 6

INTERFACE	CABLE	LINE UNIT CONNECTOR	TEST CONNECTOR
RS-232-C	BC55C-10	J2	H325
	BC05D-25		H325
RS-422	BC55B-10	J2	H3251
RS-422	BC55D-33		H3251
RS-423 (SEE NOTE)	BC55C-10	J2	H3251
	BC55D-33		H3251
V.35	BC05Z-25	J1	H3250
INTEGRAL MODEM	BC55A-10	J1	PANEL SWITCHED TO HDX POSITION

NOTE: The normal F.A.& T. set-up of the DMR11-AA is to use the RS423 interface and the H3251 test connector.

7.0 POWER CHECKS

7.1 Ensure that the following voltages exist:

MODULE	VOLTAGE	MAX VOLT.	MIN VOLT.	BACKPLANE PIN
M8207-RA	+5 VDC	+5.25V	+5.0V	C1A2
M8203	+5 VDC	+5.25V	+5.0V	C1A2
	+15 VDC	+15.75V	+14.25V	C1U1
	-15 VDC	-15.75V	-14.25V	C1B2

*** CAUTION ***

Each DMR11 requires approximately 8 amperes from the +5 volt source. Check the power supply before and after installation to avoid overloading.

8.0 DIAGNOSTIC TEST PROCEDURE

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria, e.g.: Pass Counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the "CHECKLIST".

NOTE - When running all diagnostics, except CZDMI, the Line Unit TURN-AROUND CONNECTORS should be used. When running CZDMI, the Line Unit Cable and CABLE TURN-AROUND should be used.

8.1 CZDMP ..... M8207 STATIC DIAGNOSTIC I

8.1.1 Load diagnostic and supervisor through available load media.

8.1.2 Load address 200 and start.

8.1.3 Enter STA <CR>.

8.1.4 Answer hardware and software questions. The following questions will be asked on a start command. The value located to the left of the question mark is the default value that will be taken on a carriage return response.

1. WHICH MICRO-CPU: (0) 7? <CR>

2. MICRO-CPU CSR ADDRESS: (0) 160070? <CR>

3. MICRO-PROCESSOR VECTOR ADDRESS: (0) 300? <CR>

4. MICRO-PROCESSOR PRIORITY LEVEL: (0) 5? <CR>

NO SOFTWARE PARAMETER QUESTIONS ARE ASKED BY PART 1 OF THE STATIC LOGIC TESTS.

8.1.5 End of pass message will be printed. No errors allowed.

8.2 CZDMQ ..... M8207 STATIC DIAGNOSTIC 2

8.2.1 Load diagnostic and supervisor through available load media.

8.2.2 Load address 200 and start.

8.2.3 Enter STA <CR>.

8.2.4 Answer hardware and software questions. The following questions will be asked on a start command. The value located to the left of the question mark is the default value that will be taken on a carriage return response.

1. WHICH MICRO-CPU? (0=M8200, 4=M8204, 7=M8207) (0) 7? <CR>

2. MICRO-CPU CSR ADDRESS: (0) 160070? <CR>

3. MICRO-PROCESSOR RUN SWITCH-TYPE 0 IF OFF, 1 IF ON: (0) 1? <CR>

NO SOFTWARE PARAMETER QUESTIONS ARE ASKED BY PART 2 OF THE STATIC LOGIC TESTS.

8.2.5 End of pass message will be printed. No errors allowed.

8.3 CZDMR ..... M8203 STATIC DIAGNOSTIC 1

8.3.1 Load diagnostic and supervisor through available load media.

8.3.2 Load address 200 and start.

8.3.3 Enter STA <CR>.

8.3.4 Answer hardware and software questions. The following questions will be asked on a start command. The value located to the left of the question mark is the default value that will be taken on a carriage return response.

1. DEVICE CSR ADDRESS: (0) 160070? <CR>

2. DEVICE VECTOR ADDRESS: (0) 300? <CR>

3. DEVICE PRIORITY LEVEL: (0) 5? <CR>

4. (M8207-E27,SW7) RUN SWITCH - TYPE 0 IF OFF, 1 IF ON: 1? <CR>

NO SOFTWARE PARAMETER QUESTIONS ARE ASKED BY PART 1 OF THE STATIC LOGIC TESTS.

8.3.5 End of pass message will be printed. No errors allowed.

8.4 CZDMS ..... M8203 STATIC DIAGNOSTIC 2

8.4.1 Load diagnostic and supervisor through available load media.

8.4.2 Load address 200 and start.

8.4.3 Enter STA <CR>.

8.4.4 Answer hardware and software questions. The following questions will be asked on a start command. The value located to the left of the question mark is the default value that will be taken on a carriage return response.

1. DEVICE CSR ADDRESS: (O) 160070? <CR>

2. DEVICE VECTOR ADDRESS: (O) 300? <CR>

3. DEVICE PRIORITY LEVEL: (O) 5? <CR>

4. M8203 REG 11 (E121 SW10,9 E134 SW9,10) : (O) 6? <CR>

5. M8203 REG 15 (E134 SW1-8) : (O) 377? <CR>

6. M8203 REG 16 (E121 SW1-8) : (O) 0? <CR>

7. TURN AROUND TYPE-: (O) 0? <CR>
(0=H3254 & H3255, 1=CABLE, 2=MOD LOC, 3=MOD REM, 4=NONE)

0 SHOULD BE SELECTED SO ALL TESTS WILL BE RUN, AND IF 1-4 IS SELECTED, CERTAIN TESTS CANNOT BE RUN, AND THE PROGRAM WILL TYPE THE NUMBER(S) OF TEST(S) TO BE SKIPPED.

8. PLEASE SELECT BAUD RATE: TYPE '0' FOR 2.4K; '1' FOR 4.8K; '2' FOR 9.6K; '3' FOR 19.2K; '4' FOR 56K; '5' FOR 250K; '6' FOR 500K; '7' FOR 1 MEG BAUD: (O) 4? <CR>

NOTE - Insure that the Baud rate selected corresponds to the module set-up. See Table 5.

(THE DEFAULT IS 4 FOR 56K BAUD)

NOTE - Steps 9 thru 12 are examples of software parameter questions which need not be invoked.

9. IS MAN. INTERVEN. DESIRED TO MOUNT TEST CONNECTOR(S) (L) N? <CR>

10. SHOULD SWITCH PACK AND AX3-15 PRINTOUT BE ALLOWED (L) N? <CR>

11. SHOULD SWITCH PACK TESTS BE ALLOWED (L) N? <CR>

12. MSG TIMER VALUE (0-177777), 0 = LONGEST TIME OUT: (O) 0? <CR> (THE DEFAULT SHOULD BE USED OR ERRORS MAY RESULT)

8.4.5 End of pass message will be printed. No errors allowed.

8.5 CZDMI .... DMR11 FUNCTIONAL DIAGNOSTIC

NOTE - Install Cable & Turn-around Connector. Refer to section 6.2.5 for details.

8.5.1 Load diagnostic and supervisor through available load media.

8.5.2 Load address 200 and start.

8.5.3 Enter STA <CR>.

8.5.4 Answer hardware and software questions. The following questions will be asked on a start command. The value located to the left of the question mark is the default value that will be taken on a carriage return response.

1. DEVICE CSR ADDRESS: (0) 160070? <CR>

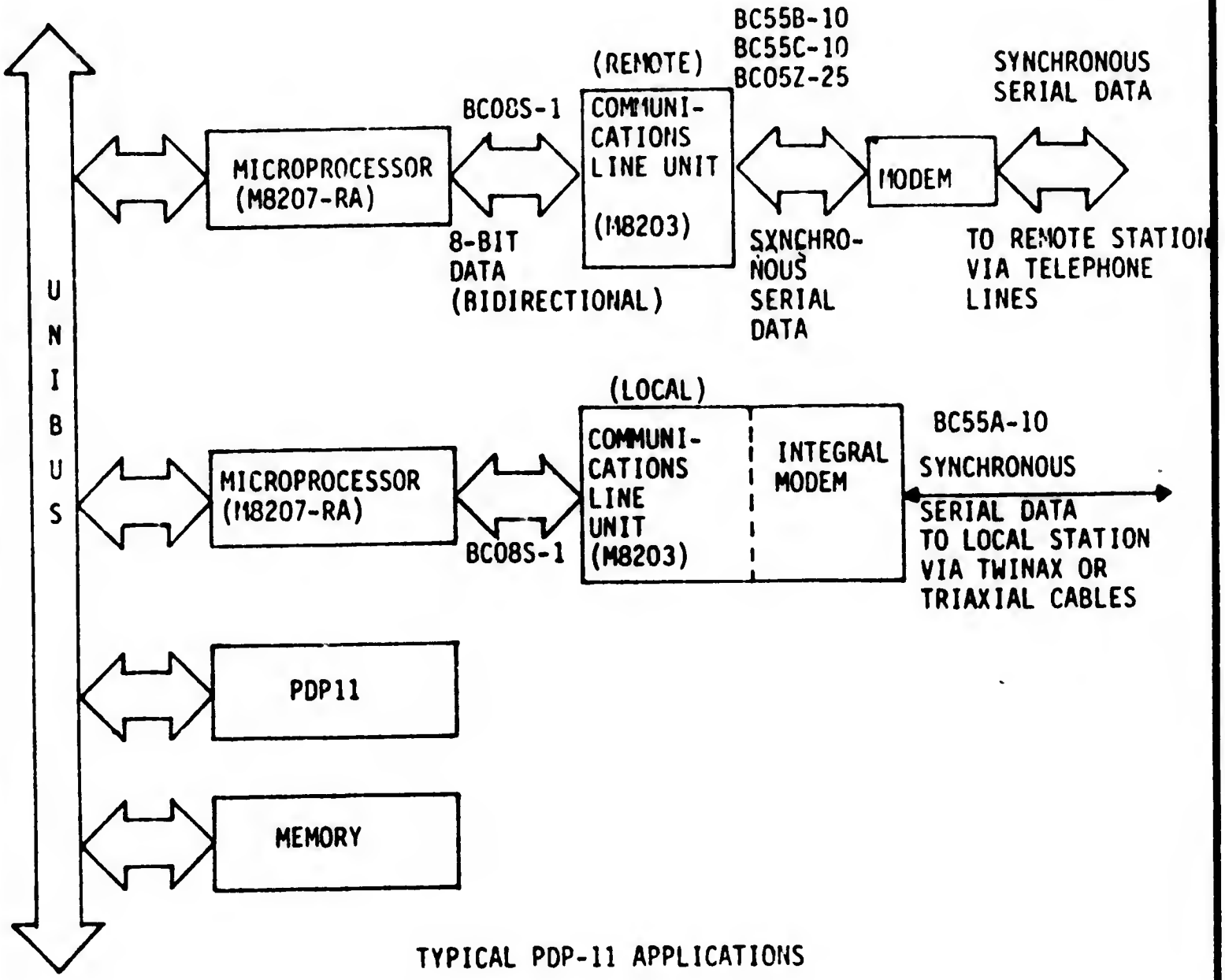
2. DEVICE VECTOR ADDRESS: (0) 300? <CR>

3. TEST CONFIGURATION =

0 = INTERNAL (NO CONNECTOR)
1 = H3254 - V.35
2 = H3254 - INTEGRAL
3 = H3255 - RS232C/423
4 = H3255 - RS422
5 = CABLE AND SW PACK INTERFACE SELECTED
****SELECT THE FOLLOWING IF THE MODEM SUPPORTS LOOPBACK****
6 = LOCAL LOOP
7 = REMOTE LOOP

(0) 5? <CR> (THE DEFAULT IS FOR ACTUAL CABLE LOOPBACK 5)

8.5.5 End of pass message will be printed. No errors allowed.



TYPICAL PDP-11 APPLICATIONS

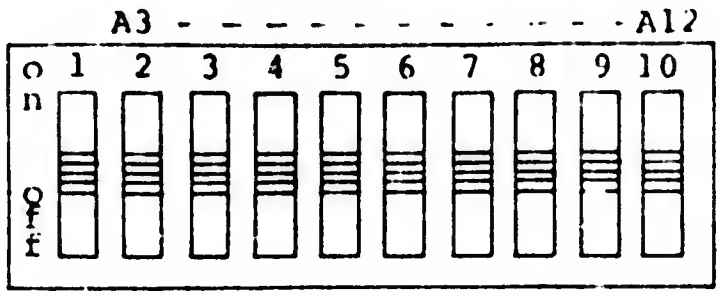
FIGURE 1

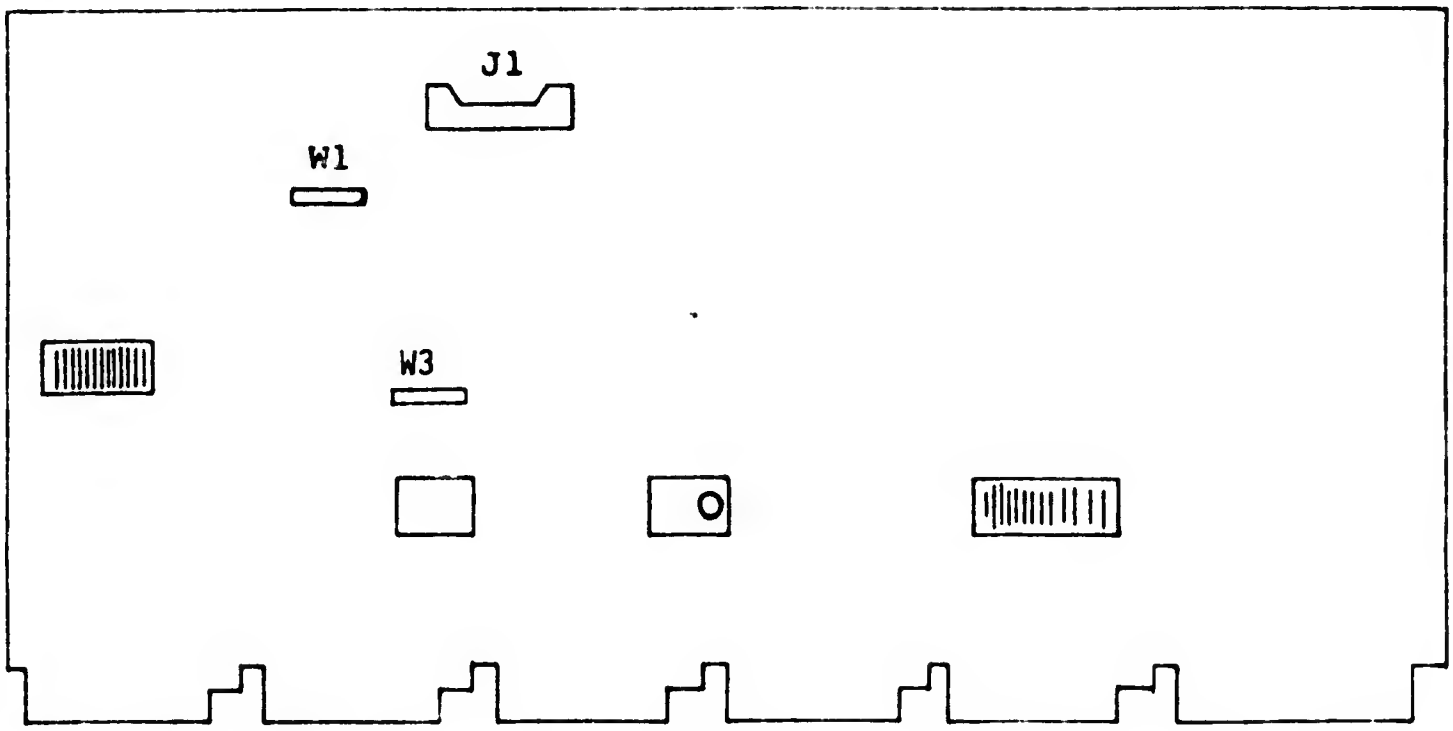
TITLE

MODULAR APPROACH TO SYSTEMS TEST

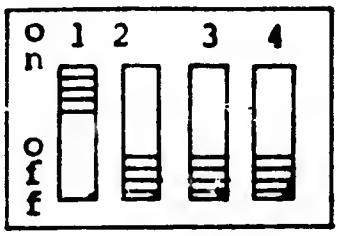
SWITCH PACK E127
DEVICE ADDRESS
SELECTION

M8207-RA MICROPROCESSOR
SWITCH/JUMPER LOCATIONS





SWITCH PACK
E85

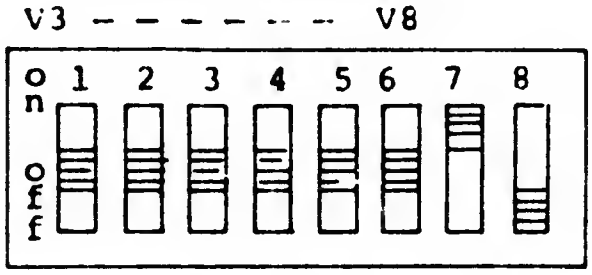


SPARES

BSEL 1 LOCKOUT

PRIORITY
PLUG

SWITCH PACK E28

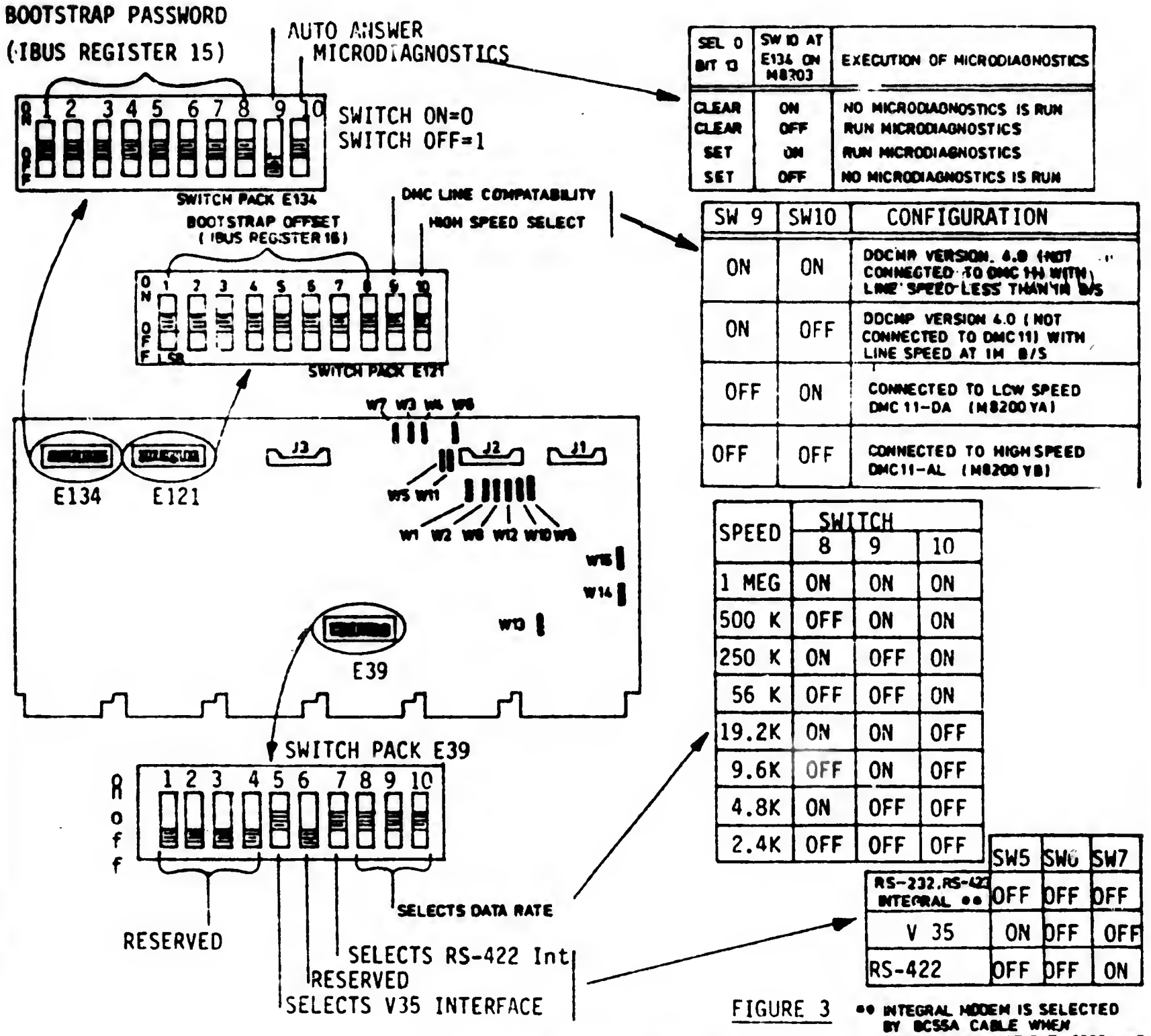


VECTOR ADDRESS
SELECTION

RUN INHIBIT
CSR DISABLE

FIGURE 2

	SIZE	CODE	NUMBER	REV
	A	SP	MA-A5298-0-0	B



SEL 0 BIT 13	SW 10 AT E134 ON M8203	EXECUTION OF MICRODIAGNOSTICS
CLEAR	ON	NO MICRODIAGNOSTICS IS RUN
CLEAR	OFF	RUN MICRODIAGNOSTICS
SET	ON	RUN MICRODIAGNOSTICS
SET	OFF	NO MICRODIAGNOSTICS IS RUN

SW 9	SW10	CONFIGURATION
ON	ON	DDCMP VERSION 4.0 (NOT CONNECTED TO DMC 11) WITH LINE SPEED LESS THAN 1M B/S
ON	OFF	DDCMP VERSION 4.0 (NOT CONNECTED TO DMC11) WITH LINE SPEED AT 1M B/S
OFF	ON	CONNECTED TO LOW SPEED DMC 11-DA (M8200 YA)
OFF	OFF	CONNECTED TO HIGH SPEED DMC11-AL (M8200 YB)

SPEED	SWITCH 8	9	10
1 MEG	ON	ON	ON
500 K	OFF	ON	ON
250 K	ON	OFF	ON
56 K	OFF	OFF	ON
19.2K	ON	ON	OFF
9.6K	OFF	ON	OFF
4.8K	ON	OFF	OFF
2.4K	OFF	OFF	OFF

	SW5	SW6	SW7
RS-232, RS-423 INTEGRAL ••	OFF	OFF	OFF
V 35	ON	OFF	OFF
RS-422	OFF	OFF	ON

FIGURE 3

• NORMAL SWITCH SETTING UNLESS THE INTEGRAL MODEM OR NULL MODEM CLOCK FEATURES ARE USED.

•• INTEGRAL MODEM IS SELECTED BY BCSSA CABLE WHEN INSTALLED IN J1 OF THE M8203 LINE UNIT. MODULE CONNECTOR J2 MUST NOT HAVE ANY CABLE OR TEST CONNECTOR INSTALLED

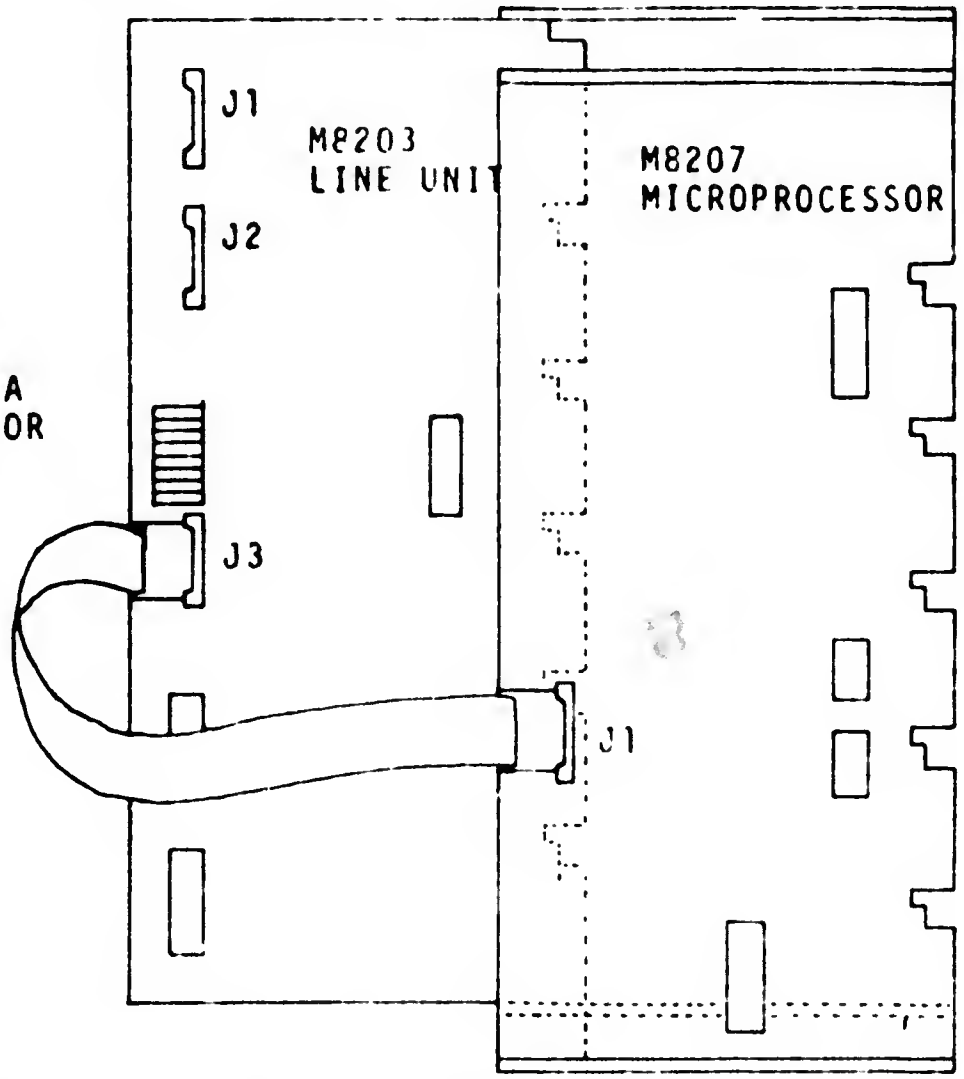
CONNECT CABLE BC05Z FOR V.35 INTERFACE OR
BC55A FOR INTEGRAL MODEM

H3254
TEST CONNECTOR SIDE 1

H3255
TEST CONNECTOR SIDE 2

CONNECT CABLE BC55C-10
FOR RS-232-C OR RS-423-A
INTERFACE OR BC55B-10 FOR
RS-422-A INTERFACE

BC08S-1
(no twist)



MICROPROCESSOR/LINE UNIT INSTALLATION

FIGURE 4

BC55C-10 (RS-232C-/RS423) INTERFACE PANEL CABLE

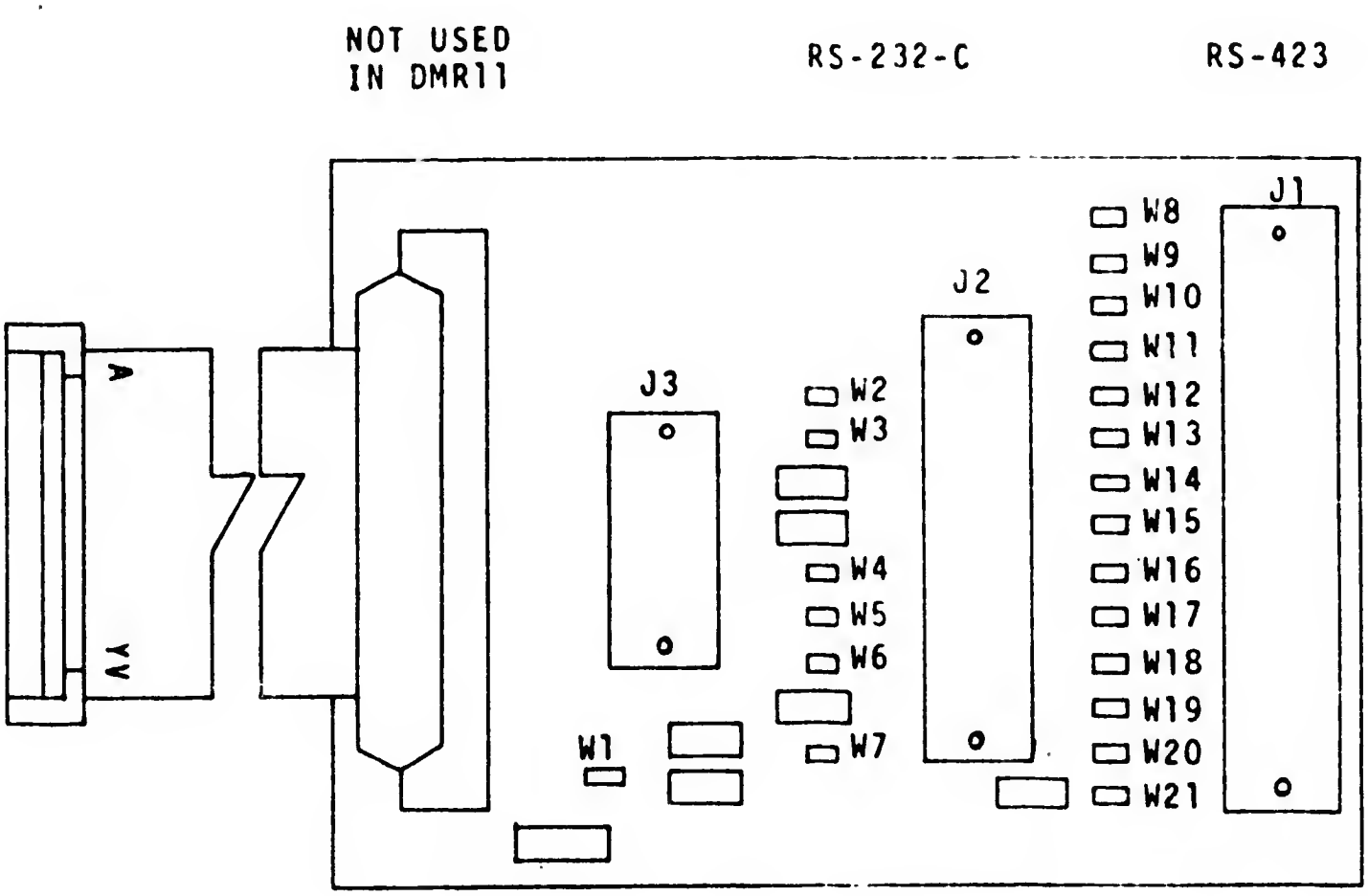
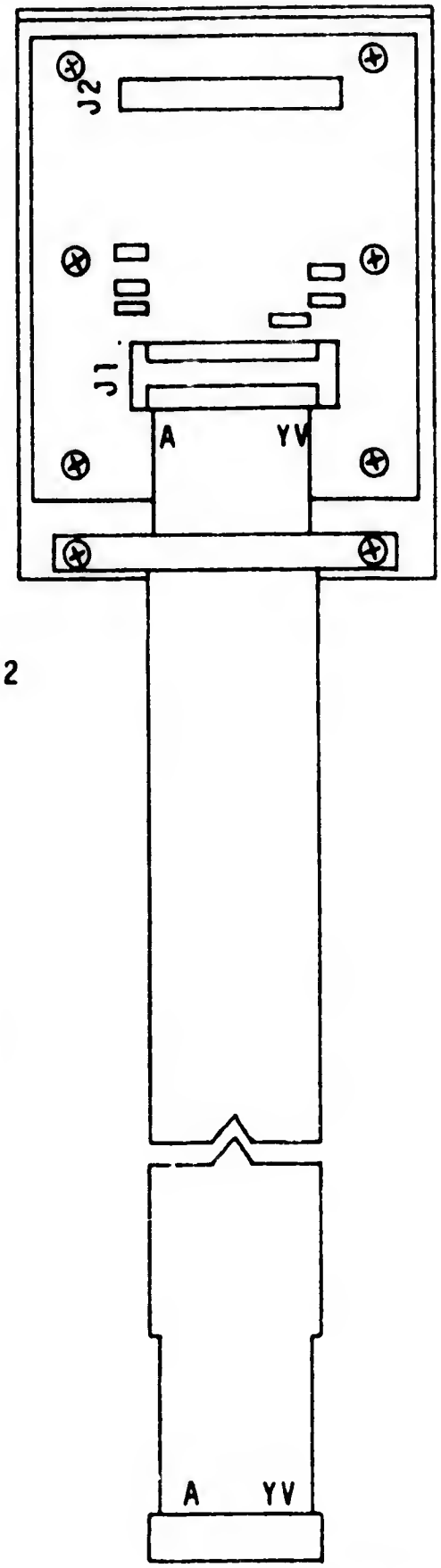


FIGURE 5

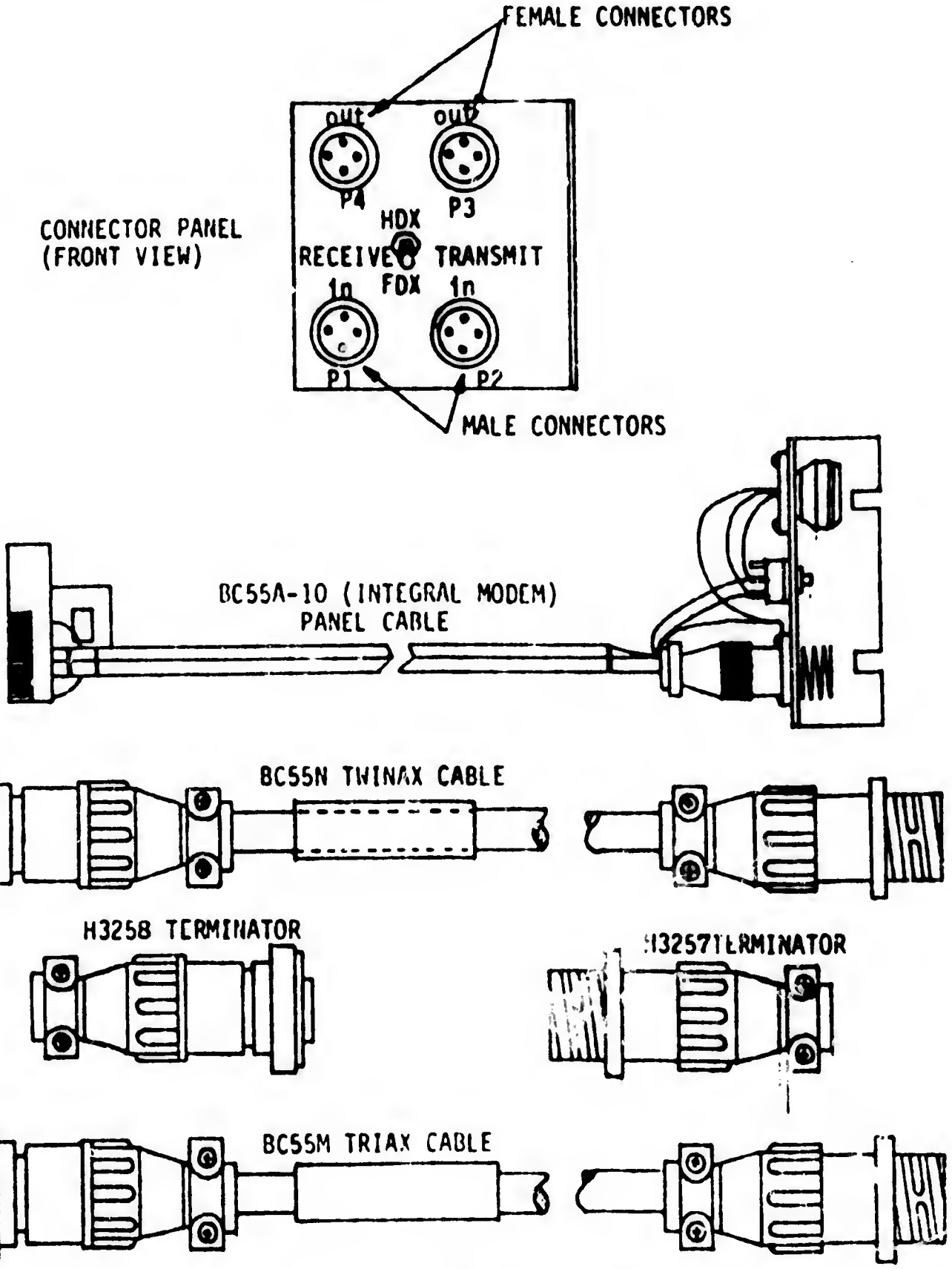


BC55B-10 (RS-422 INTERFACE)

PANEL CABLE

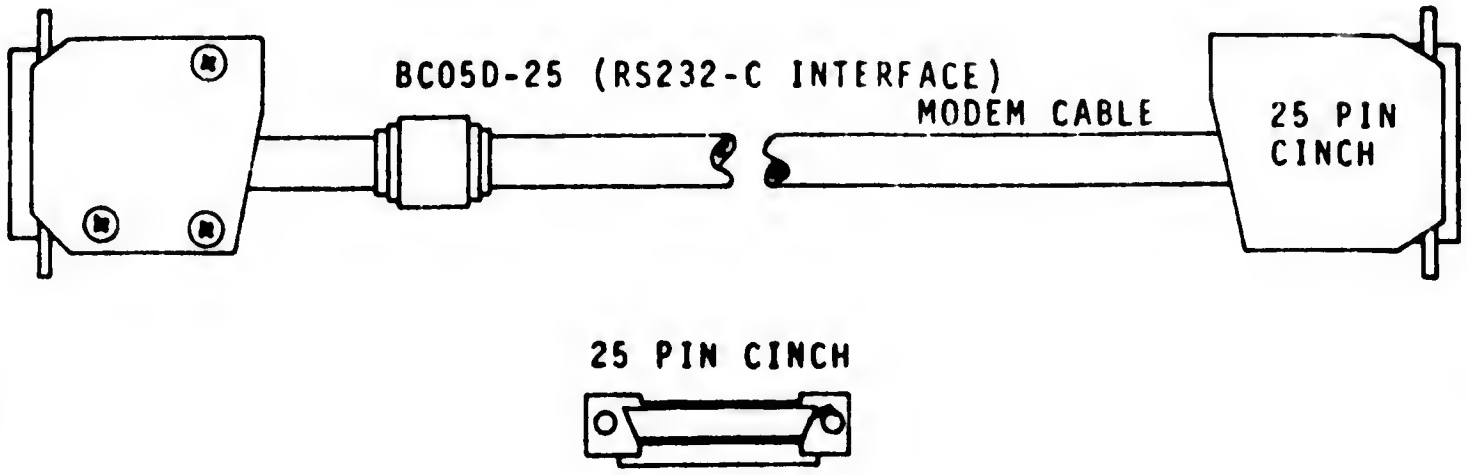
FIGURE 6[f]

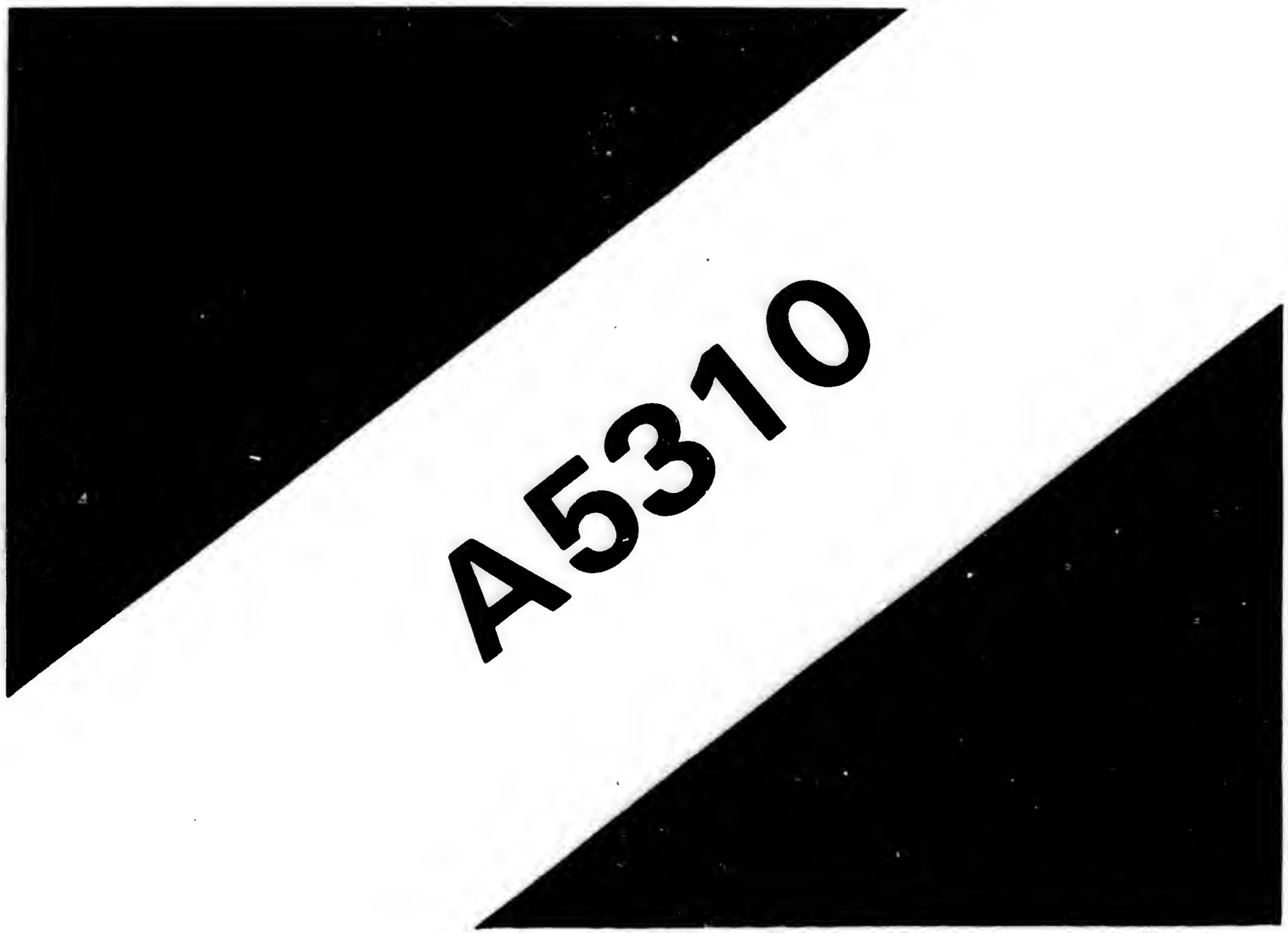
FIGURE 7



	SIZE	CODE	NUMBER	REV
	A	SP	MA-A5298-0-0	B

FIGURE 8


BC05D-25 (RS232-C INTERFACE)
MODEM CABLE
25 PIN
CINCH
25 PIN CINCH
BC55D-33 (RS-422/RS423 INTERFACE)
MODEM CABLE
37 PIN
CINCH
37 PIN CINCH
A
BC05Z-25 (V.35 INTERFACE) MODEM CABLE
B
C
A
E


A531610

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DLV11-A,B ASYNCHRONOUS INTERFACE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5310					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Lenienski		A	SP	MAA5310-0-0	A

EN-01083-1(N672-(302)

DL11-A,B ASYNCHRONOUS INTERFACE

1.0 ABSTRACT

The following describes the system test procedure for the DL11-A and B. Basically, a "finished" DL11 is taken from the stockroom consisting of an M7800 module and cable. According to customer specification, jumpers must be cut on the M7800 to select data format, the proper crystal must be installed, and address and vectors must be assigned. Details of this process are described in A-SP-DL11-0-2 "Installation Procedure".

2.0 REQUIREMENTS

The minimum equipment requirements are:

A. PDP-11 with 4K of core memory.

B. DL11 interface and associated cabling.

C. Some type of terminal

3.0 REFERENCE DOCUMENTS

MANUALS:	EK-DL11-TM-003 DL11 Eng. Drawings or later revisions B-DD-DL11-0
CHECKOUT & ACCEPTANCE PROCEDURES:	A-SP-DL11-0-3
INSTALLATION PROCEDURE:	A-SP-DL11-0-2

MAINDEC LISTINGS:

DZKLA	TELETYPE TEST
DZDLA	DL11-E/C/D OFF-LINE TEST
DZDLB	DL11-E ON-LINE TEST
DZVTB	VT05 DISPLAY TERM. TEST
DZLAC	LA36 DIAGNOSTIC
DZVTC	VT50 DISPLAY TERM. TEST

4.0 TEST PROCEDURE

The normal test procedure is to run the DL11 attached to the customer ordered DEC terminal such as LA30, VT05, VT50, LT33, LT35, or LA36. Refer to Section 3.0 for a list of Maindecs.

If the customer has not ordered a DL11 + terminal combination, then the DL11 should be attached to a VT05, if compatible. Any DL11 is "VT05 Compatible" if the DL11 conforms to the following format:

a. 8 data bits;
b. 1 or 2 stop bits;
c. parity off;
d. baud rate: 110,150, 300, 600, 1200, 2400, 2400/150, 1200/150;
e. EIA or current loop.

The jumpers on the M7800 should not be altered to conform to the above list; however, the baud rate should be adjusted by switch - as long as it is within the range of the crystal - in order to conform to a VT05 speed.

If the DL11 is neither a DL11 + terminal combination nor "VT05 Compatible", then only an off-line maintenance test can be used.

Details of the test procedure follow:

DL11-A,B:

Test the DL11-A or B using the first applicable method below:

1. DL11 + DEC terminal: run appropriate terminal test. See MAINDEC write-up for procedure.

2. Attach to VT05 if "VT05 Compatible" and run DZVTB, Program 2, "Keyboard Test."

3. If neither 1 or 2 apply, run in maintenance mode using DZKLA, Program 0 and 14.

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MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DL11-C, D, E ASYNCHRONOUS INTERFACE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5315					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Jeleniewski	Tom	A	SP	MAA5315-0-0	A

DL11-C,D,E ASYNCHRONOUS INTERFACE

1.0 ABSTRACT

The following describes the system test procedure for the DL11-C through DL11-E. Basically, a "finished" DL11 is taken from the stockroom consisting of an M7800 module and cable. According to customer specification, jumpers must be cut on the M7800 to select data format, the proper crystal must be installed, and address and vectors must be assigned. Details of this process are described in A-SP-DL11-0-2 "Installation Procedure".

2.0 REQUIREMENTS

The minimum equipment requirements are:

A. PDP-11 with 4K of core memory.

B. DL11 interface and associated cabling.

C. Some type of terminal.

3.0 REFERENCE DOCUMENTS

MANUALS:	EK-DL11-TM-003 DL11 Eng. Drawings or later Rev. B-DD-DL11-0
CHECKOUT & ACCEPTANCE PROCEDURES:	A-SP-DL11-0-3
INSTALLATION PROCEDURE:	A-SP-DL11-0-2

MAINDEC LISTINGS:

DZKLA	TELETYPE TEST
DZDLA	DL11-E/C/D OFF-LINE TEST
DZDLA	DL11-E ON-LINE TEST
DZVTB	VT05 DISPLAY TERM. TEST
DZLAC	LA36 DIAGNOSTIC
DZVTC	VT50 DISPLAY TERM. TEST

4.0 TEST PROCEDURE

The normal test procedure is to run DL11 attached to the customer ordered DEC terminal such as LA30, VT05, LT33, LT35, or LA36. Refer to Section 3.0 for the appropriate MAINDEC number.

If the customer has not ordered a DL11 + terminal combination, then the DL11 should be attached to a VT05, if compatible. Any DL11 is "VT05 Compatible" if the DL11 conforms to the following format:

a. 8 data bits;
b. 1 or 2 stop bits;
c. parity off;
d. baud rate: 110, 150, 300, 600, 1200, 2400, 2400/150, 1200/150;
e. EIA or current loop.

The jumpers on the M7800 should not be altered to conform to the above list; however, the baud rate should be adjusted by switch - as long as it is within the range of the cyrstal - in order to conform to a VT05 speed.

If the DL11 is neither a DL11 + terminal combination nor "VT05 Compatible", then only an off-line maintenance test can be used.

Details of the test procedure follow:

DL11-C,D,E:

First run DZDLA Off-Line Test, Program 0, for 2 complete passes DL11-E's must be run with H315 connector. Then run the first applicable method below:

1. DL11 + DEC terminal: run appropriate terminal test. See MAINDEC write-up for procedure.

2. Attach to VT05 if "VT05 Compatible" and run DZVTB, Program 2, "Keyboard Test".

3. If neither 1 or 2 applies, no further testing can be done for DL11-C's and E's. For DL11-D's jumper pins 2 and 3 on EIA connector and run DZDLA, Program 0, Test 56.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DLV11 SERIAL LINE UNIT FOR PDP-11/03 - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	Prev. 7668001-0-5320					

ENG	APPD	SIZE	CODE	NUMBER	REV
DM Sekerinski	Tom Leith	A	SP	MAA5320-0-0	B

DLV11 SERIAL LINE UNIT FOR PDP-11/03

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic write ups for the purpose of expediency. The procedure has been kept brief, and to the point, to keep from confusing the user. For additional information, it will be necessary to refer to the diagnostic write up.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD 116)

2.2 11/03 Printset

2.3 LSI11 PDP 11/03 Configuration and Installation Guide EK LSI11-IN-001

2.4 LSI11 PDP 11/03 Users Manual EK LSI11-TM-002

2.5 DLV11 Engineering Specifications A-SP-DLV11-0-0

2.6 Microcomputer Handbook

3.0 REQUIRED TEST EQUIPMENT

3.1 DLV11 module

3.2 Wraparound test connecter

3.3 Output terminal

3.4 LSI-11 standard computer

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC 11-DVKAE DLV11 Test Diagnostic and Writeup

4.2 MAINDEC 11-DXDLA DZC/X11 Exerciser and Writeup

5.0 SPECIAL INSTRUCTIONS AND CHECKS

5.1 Insure wraparound connecter is installed to run DECX11.

6.0 TEST SETUP

6.1 Set up jumpers for address, vector, baud rate as required.

6.2 Remove capacitor C44 .005UF if serial line device is not a tele-typewriter.

6.3 Install appropriate cable in J1 of module A-EIA interface BC05C-X modem cable B-20MA current loop - BC05M-X cable assy.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 DLV11 Test (DVKAE)

7.1.1 Load program through appropriate load media.

7.1.2 Program starting address

7.1.2.1 Load address 200
7.1.2.2 Start 000000, software SR default value (1000 for wrap test) or on alternate setting (see 7.1.3)

7.1.3 Alternate software SR settings (loc 122)

7.1.3.1 SW 15 = 1 Continue on error
7.1.3.2 SW 14 = 1 Loop on error
7.1.3.3 SW 10 = 1 Loop on test
7.1.3.4 SW 9 = 1 Run wrap test

7.1.4 Testing other than console DLV11's

Supply correct address and vector to the following locations:

7.1.4.1 Loc 220 - Address of receiver CSR
7.1.4.2 Loc 222 - Address of receiver buffer
7.1.4.3 Loc 224 - Address of transmitter CSR
7.1.4.4 Loc 226 - Address of transmitter buffer
7.1.4.5 Loc 230 - Address of receiver vector
7.1.4.6 Loc 232 - Address of associated PSW
7.1.4.7 Loc 234 - Address of transmitter vector
7.1.4.8 Loc 236 - Address of associated PSW

7.1.5 Operator Action

7.1.5.1 Install test connector in J1
7.1.5.2 Type 200G

7.1.6 Evidence of End of Pass andRun Time

7.1.6.1 Program will print "END OF PASS" time dependent on baud rate.

7.1.7 Acceptable errors:

None

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MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DLV11-E ASYNCHRONOUS SINGLE SERIAL LINE INTERFACE WITH MODEM

REVISIONS APPENDIX A CONTROL

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5321					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelenkowski		A	SP	MAA5321-0-0	A

EN-01083-10-N672-(392)

DLV11-E ASYNCHRONOUS SINGLE SERIAL LINE INTERFACE WITH MODEM CONTROL

INTRODUCTION

This procedure establishes the minimum test and electrical standards that a DLV11-E must meet to be considered acceptable for customer shipment.

DESCRIPTION

The DLV11-E is an asynchronous line interface module that interfaces the LSI-11 bus to a serial communications line. The DLV11-E receives serial data from a peripheral device and assembles it into parallel data for the LSI-11 Bus. In turn, the parallel data from the LSI-11 Bus is converted into serial data and is transmitted to a peripheral device. The DLV11-E is unique from other DLV11s in that it offers full modem control.

Option	Qty/Contents	Description
DLV11-E	1 - M8017	Module
	1 - H315	Modem Test Conn.

1.0 REFERENCE DOCUMENTATION

1.1 Print Set MP00460

1.2 Technical Manual EK-DLV11-TM-(Rev)

1.3 Users Guide EK-DLV11-OP-(Rev)

1.4 Lib Kit ZJ-243-RB

1.5 Ship List A-PL-DLV11-E

1.6 Packaging Inst. A-SP-3700297-40-0

2.0 REQUIRED TEST EQUIPMENT

2.1 PDP 11/03 with a minimum of 4K of memory and one available slot.

2.2 Scope: 465 or equivalent.

2.3 For power requirements, refer to Section 6.0.

2.4 Wire wrap gun (OK Speed Wrap Model #BW-515BF) or equivalent.

2.5 Unwrapping tool - hand type, unwraping tool.

2.6 Cable: (BC01V-X or BC05C-X) or turnaround connector. See page 10 for directions on making a turn around connector that will plug into the module.

3.0 AVAILABLE DIAGNOSTIC PROGRAMS

3.1 Kit # ZJ-243-RB

CVDVA - DLV11-E Off Line Tests paper tape and document

3.2 DECX11

DXDLA-H - DLV11 DECX11 Exerciser (Rev H or higher only)

4.0 INSTALLATION INSTRUCTIONS

4.1 If the DLV11-E is being tested as an option add-on, it is not necessary to change configured jumpers. See tables 4.1.1 and 4.1.2 for shipped configuration.

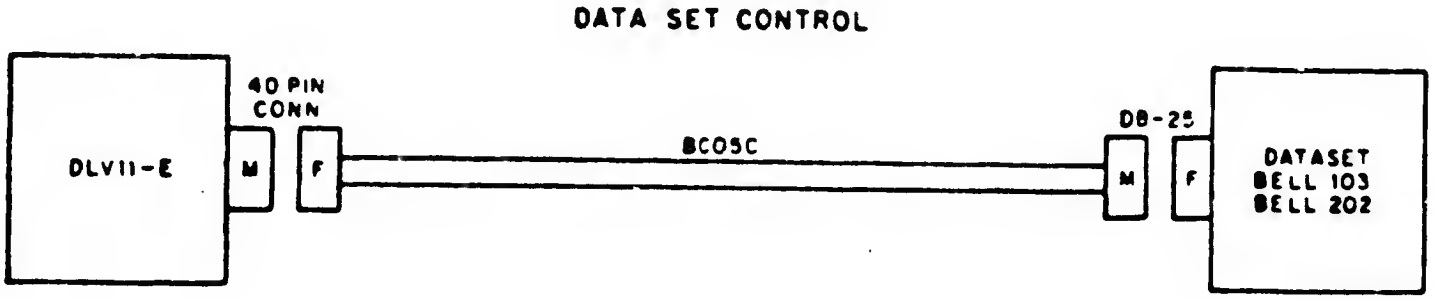
4.2 When being installed in a customer system, it may be necessary to change the jumpers as they are shipped. When configuring, refer to tables 4.1.1 and 4.1.2 for proper installation.

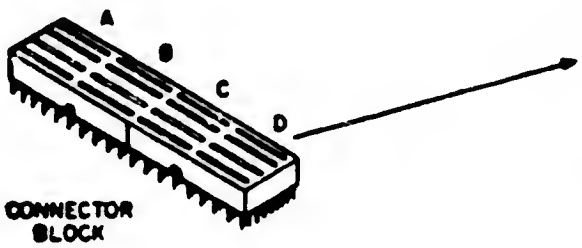
4.3 CAUTION #1 - When changing wire wrapings, always use equipment designed for that purpose, and calibrated. Note Sections 2.4 and 2.5 for type of equipment.

4.4 CAUTION #2 - All wire wraping must be done to Digital's workmanship standard; DEC Std 116. Reference should be made to Section 3. in that text.

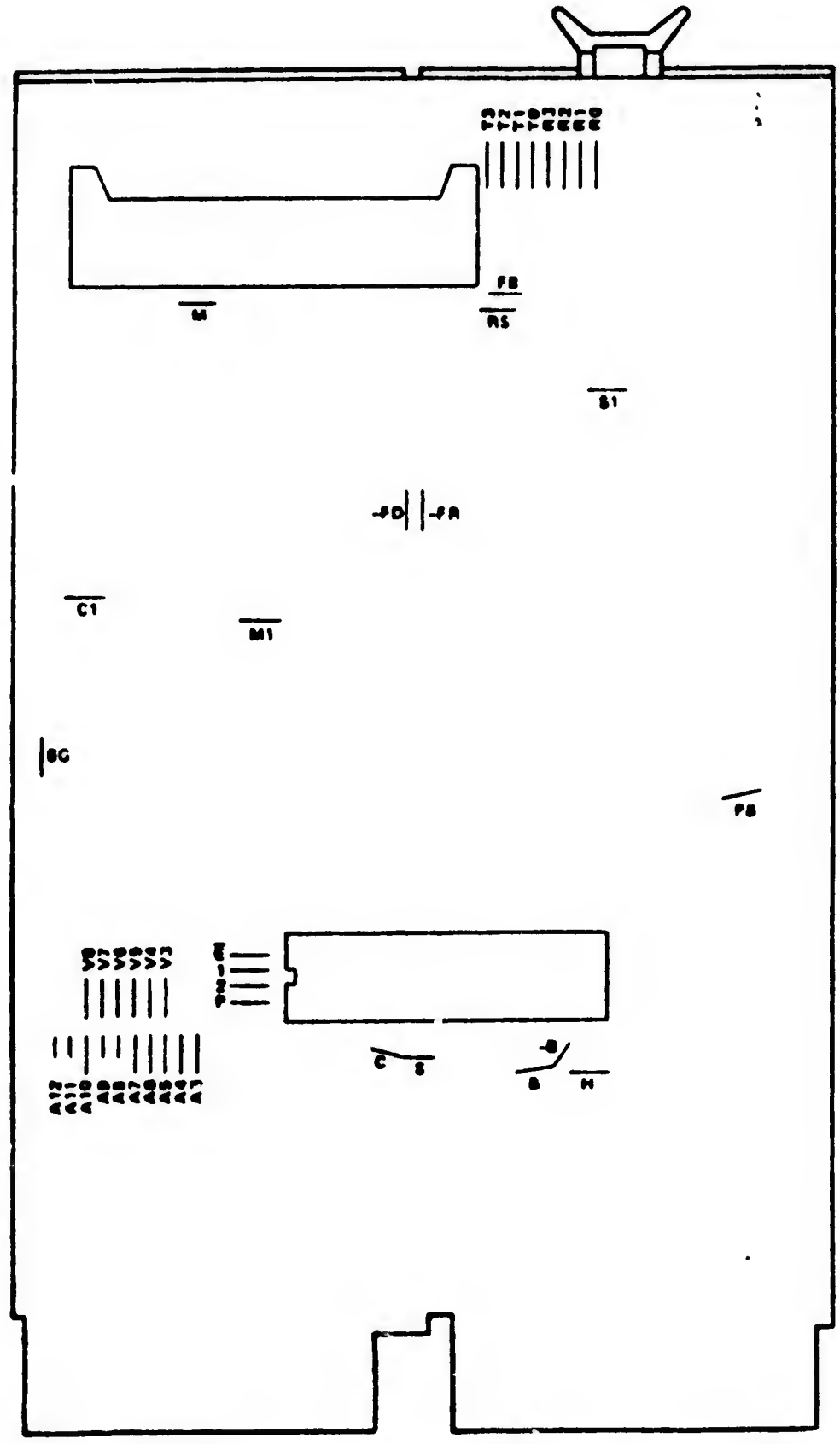
4.5 CAUTION #3 - All wire wraping should be done by a qualified person. Mistakes may cause damage to the wire wrap pin or printed circuit board.

4.6 The DLV11-E can be installed in any slot of the LSI-11 Backplane, except the first 4 slots that are reserved for the LSI-11 processor modules. When installing the DLV11-E, do not leave any open slots between the process modules and the DLV11-E. Note that priority for each option is determined by how close that option is installed to the processor modules. The closer to the processor you get, the higher priority the option has. A picture of a typical configuration is shown below:





4.1.1 DLV11-E Jumper Locations



4.1.2 Jumper Definitions

I = Jumper inserted = program bit cleared

R = Jumper removed = program bit set

NOTE: Jumpers are inserted to enable the function they control except for those jumpers that indicate negation (such as "-B") Negated jumpers are removed to enable the functions they control.

Jumper	Jumpers Installed when ship'd from Vol. Mfg.	Function
A3-A12		These jumpers correspond to bits 3-12 of the address word. When inserted, they will cause the bus interface to check for a True condition on the corresponding address bit.
A3	I	Jumpers A3 through A12 implement device address 17561X for the DLV11-E. The least significant octal digit is hard-wired on the module to address the four device registers as follows: X = 0 RCSR X = 2 RBUF X = 4 XCSR X = 6 XBUF
A4	R	
A5	R	
A6	R	
A7	I	
A8	I	
A9	I	
A10	R	
A11	I	
A12	I	
V3-V8		Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector address bit on the LSI-11 bus.
V3	R	This jumper selection implements interrupt vector address 300₈ for receiver interrupts and 304₈ for transmitter interrupts on the DLV11-E.
V4	R	
V5	R	
V6	I	
V7	I	
V8	R	

Jumper	Jumpers installed when ship'd from Vol. Mfg.	Function
R0 R1 R2 R3	I R I I	The module is configured to receive at 110 baud. Receiver and transmitter baud rate select jumpers, during common speed operation. See table 4.1.3
T0 T1 T2 T3	I R R R	The transmitter is configured for 9600 baud if split speed operation is used. Transmitter baud rate select jumpers during split spped operation. See table 4.1.3
BG	I	Jumper is inserted to enable Break generation.
P	R	Jumper is inserted for operation with parity.
E	R	Removed for even parity; inserted for odd parity. Receiver checks for appropriate parity and transmitter inserts appropriate parity.
1,2	R,R	These jumpers select the desired number of data bits (see Table 4.1.4)
PB	R	Jumper is inserted to enable the programmable baud rate capability.
C,C1	I,I	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted)
S,S1	R,R	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	R	This jumper is inserted to assert BHALT L when a framing error is received. This places the LSI-11 in the halt mode.

Jumper	Jumpers installed when ship'd	Function
B	R	Jumper B is inserted to negate BDCOK H when a BREAK signal or framing error is received. This causes the LSI-11 to reload the bootstrap. (Jumper -B must be removed when B is inserted.)
-B	I	
-FD	I	Jumper is removed to free DATA TERMINAL READY signal on.
-FR	I	Jumper is removed to force REQUEST TO SEND signal on.
RS	I	This jumper is inserted to enable normal transmission of the REQUEST TO SEND signal.
FB	R	Inserted to enable transmi ion of the FORCE BUSY signal (for Bell model 103E data sets)
M,M1	R,R	These are test jumpers used during the manufacture of the module. They are not defined for field use.

Table 4.1.3

Baud Rate Selections

	Bit	Bit	Bit	Bit	Bit	
Program Control	15	14	13	12	11*	
Receive Jumpers	R3	R2	R1	R0		Baud
Transmit Jumpers	T3	T2	T1	T0		Rate
	I	I	I	I		50
	I	I	I	R		75
	I	I	R	I		110
	I	I	R	R		134.5
	I	R	I	I		150
	I	R	I	R		300
	I	R	R	I		600
	I	R	R	R		1200
	R	I	I	I		1800
	R	I	I	R		2000
	R	I	R	I		2400
	R	I	R	R		3600
	R	R	I	I		4800
	R	R	I	R		7200
	R	R	R	I		9600

I = Jumper Inserted = Program Bit Cleared.

R = Jumper Removed = Program Bit Set.

*Bit 11 of the XCSR (Write Only Bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

Table 4.1.4

Data Bit Selections

Jumpers		Number of Data Bits
2	1	
I	I	5
I	R	6
R	I	7
R	R	8

5.0 TEST SET UP

5.1 No special test set up is required.

6.0 POWER CHECKS

6.1 Power requirements:

+5V ± 5% @ 1.0A (5.0 w)
+12V ± 5% @ 150 MA (1.8w)

NOTE: -12V is generated internally on the M8017 from the +12V supply.

6.2 Bus Loading

Each DLV11-E places one (1) bus load on the Q Bus as defined by the LSI-11 Q Bus Spec. (DEC STD 100).

7.0 DIAGNOSTIC TEST PROCEDURE

7.1 The DLV11-E can be tested in two (2) different turnaround configurations.

7.1.1 The first configuration for testing would be to plug a turnaround test connector directly into the DLV11-E. See Diagram 7.1 for view. This method should be used when it is impratical to work with the long modem cables or when the volume of DLV11-E's requires many cables. See Diagram 7.3 for information to make test connector.

NOTE: This test connector has no part # and cannot be ordered.

7.1.2 The second configuration for testing would be to plug a modem cable into the DLV11-E and plug the H315 turnaround connector; that is supplied, into the other end of the cable. See Diagram 7.2. The modem cable is not supplied on the DLV11-E. A cable may be supplied to the customer. If there is a cable going to the customer, use that one. If a cable is not going to be supplied, use a BC01V-X or BC05C-X.

7.2 Diagnostic Test

7.2.1 After configuring the DLV11-E to Section 7.1.1 or 7.1.2, load CVDVA through appropriate load media.

7.2.2 Starting program

7.2.2.1 Load address 200.

7.2.2.2 Start;check Section 7.2.3 for available switch settings.

7.2.3 Available test switch settings

7.2.3.1 Bit 15 - Halt on error
14 - Loop on test
13 - Inhibit error typeouts
12 - (unused)
11 - Inhibit iterations
10 - Bell on error
9 - Loop on error
8 - Loop on test in SWR 7:0
7 - Test number to loop on (used with Bit 8)

7.2.4 End of Pass is indicated by a type out

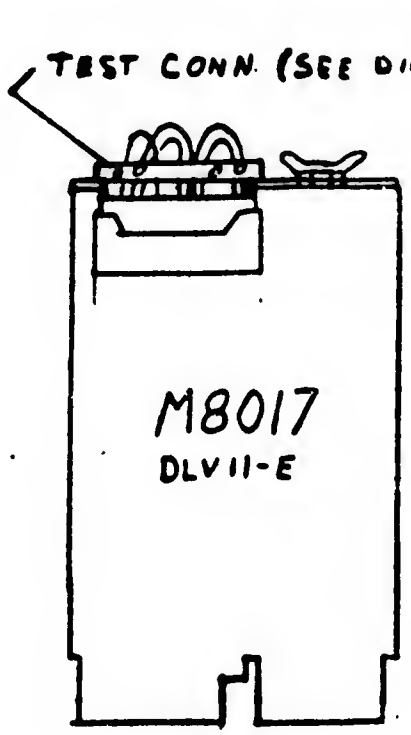


DIAGRAM 7.1

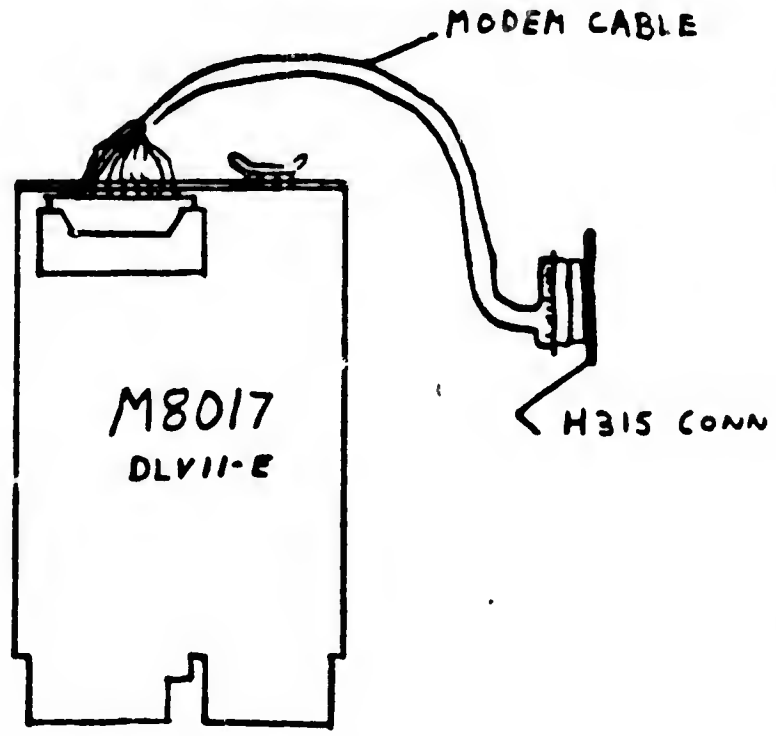


DIAGRAM 7.2

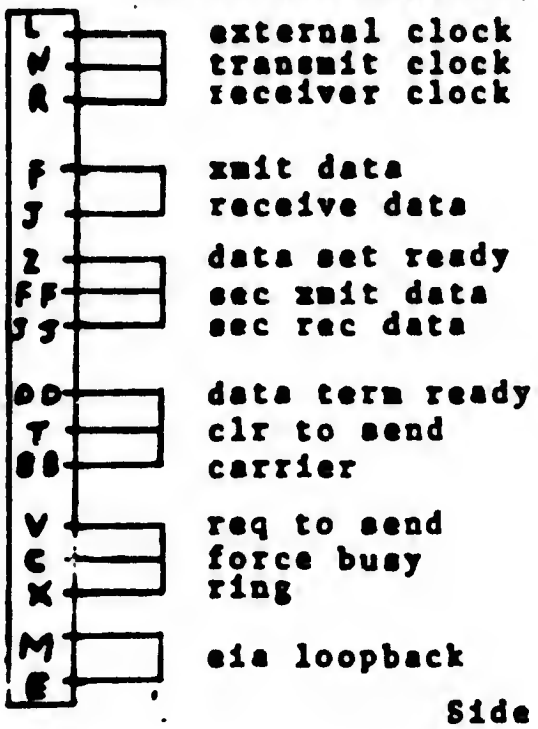
M8017 Test Connector

Diagram 7.3

Parts List

Part #	Description	Qty	Item #
12-10918-15	Conn, 44 Pos, HSG	1	1
12-10089-06	Socket, Crimp	16	2
91-07636-00	Wire, #26 Awg, Black	see notes	3
12-11166-00	Strain relief	1	4
36-11567-00	Label (this side up)	1	5

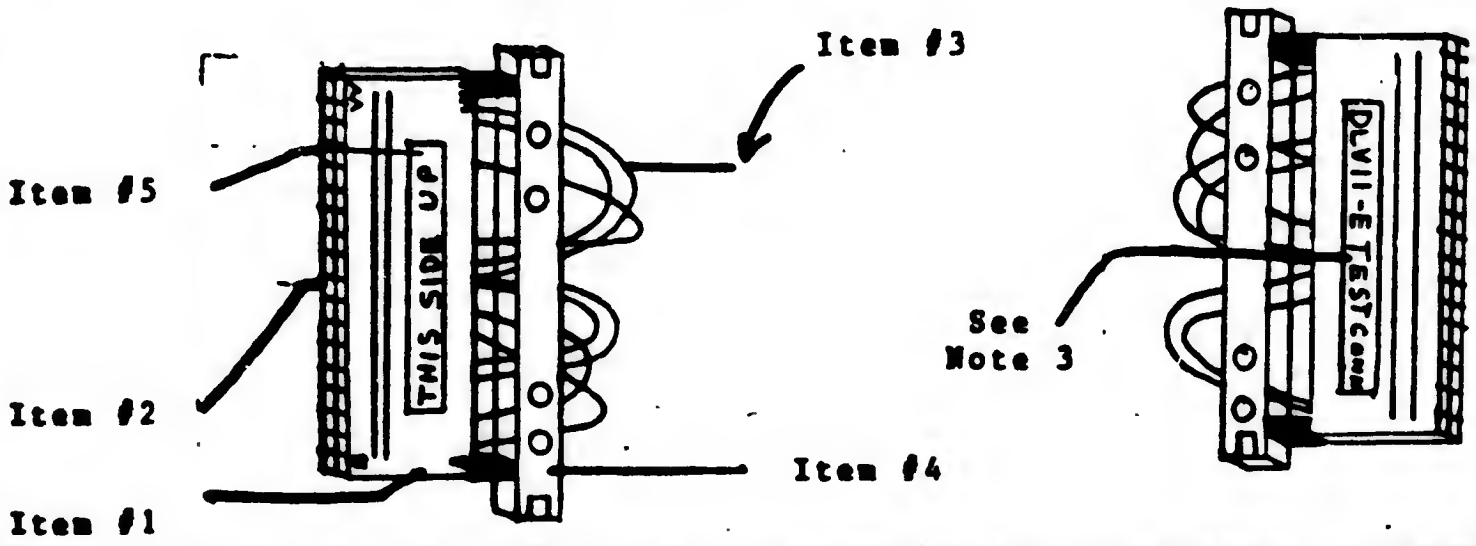
Circuit Schematic, Wire List



NOTES:

1. Suggested length of jumpers is ≈ 4 inches.
2. Actual jumper count is
   4 - double jumpers
   2 - single jumpers
3. On side 2 of Berg connector, attach label with identification "DLV11-E Test Conn". (no part # available for label)

Unit Assembly



	SIZE	CODE	NUMBER	REV
	A	SP	MAA5321-0-0	A


A53Z

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DLV11-F ASYNCHRONOUS SINGLE SERIAL LINE INTERFACE WITH 20ma

REVISIONS APPENDIX A

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5322					

ENG	APPD	SIZE	CODE	NUMBER	REV
Brent MacAloney		A	SP	MAA5322-0-0	A

DLV11-F ASYNCHRONOUS SINGLE SERIAL LINE INTERFACE WITH 20ma

INTRODUCTION

This procedure establishes the minimum test standards that a DLV11-F must meet to be considered acceptable for customer shipment.

DESCRIPTION

The DLV11-F is an asynchronous line interface module that interfaces the LSI-11 bus to a serial communications line. The DLV11-F receives serial data from a peripheral device and assembles it into parallel data for the LSI-11 bus. In turn, the parallel data from the LSI-11 bus is converted into serial data and is transmitted to a peripheral device. The DLV11-F is unique from the DLV11-E in that it supports 20ma current loop operation.

Option	Qty/contents	Description
DLV11-F	1 - M8028	module

1.0 REFERENCE DOCUMENTATION

1.1 Print Set MP00461

1.2 Technical Manual EK-DLV11-TM- (rev)

1.3 Users Guide EK-DLV11-OP-(rev)

1.4 Lib Kit ZJ-253-RB

1.5 Ship List A-PL-DLV11-F

1.6 Packaging Inst. A-SP-370029?-40-0

2.0 REQUIRED TEST EQUIPMENT

2.1 PDP11/03 with a minimum of 4K of memory and one available slot.

2.2 Scope: 465 or equivalent.

2.3 For power requirements, refer to Section 6.0.

2.4 Wire Wrap Gun (ok speed wrap model #BW-515BF) or equivalent.

2.5 Unwraping tool - hand type, unwraping tool.

3.0 AVAILABLE DIAGNOSTICS

3.1 LIB Kit # ZJ-253-RB
CVDVC - DLV11-F off line tests (paper tape and document)

3.2 DECX11 - DXDLA-H DLV11 Exerciser (Rev H or higher only)

4.0 INSTALLATION INSTRUCTIONS

4.1 If the DLV11-F is being tested as an option add-on, it is not necessary to change configured jumpers. See Tables 4.1.1 and 4.1.2 for configuration shipped from Volume Manufacturing.

4.2 When being installed in a customer system, it may be necessary to change the jumpers as they are shipped. When configuring, refer to Tables 4.1.1 and 4.1.2 for proper installation.

4.3 CAUTION #1:

When changing wire wrapings, always use equipment designed for that purpose and calibrated. Note sections 2.4 and 2.5 for type of equipment.

4.4 CAUTION #2:

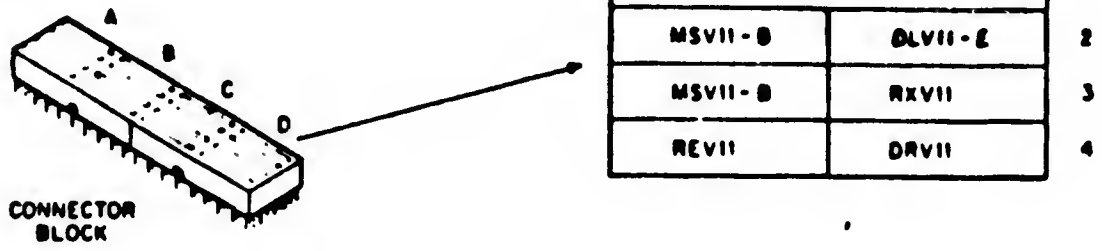
All wire wrapings must be done to Digital's workmanship standard; DEC STD 116. Reference should be made to Section 3 in that text.

4.5 The DLV11-F can be installed in any slot of the LSI-11 Backplane, except those occupied by the processor modules. When installing the DLV11-F, do not leave any open slots between the processor modules and the DLV11-F. An open slot would break the interrupt acknowledge daisy chain. Note: the priority for each option is determined by how close that option is installed to the processor modules. The closer to the processor you get, the higher priority the option. A picture of a typical configuration is shown on Page 3 and 4.

TYPICAL BACKPLANE CONFIGURATION

11/03

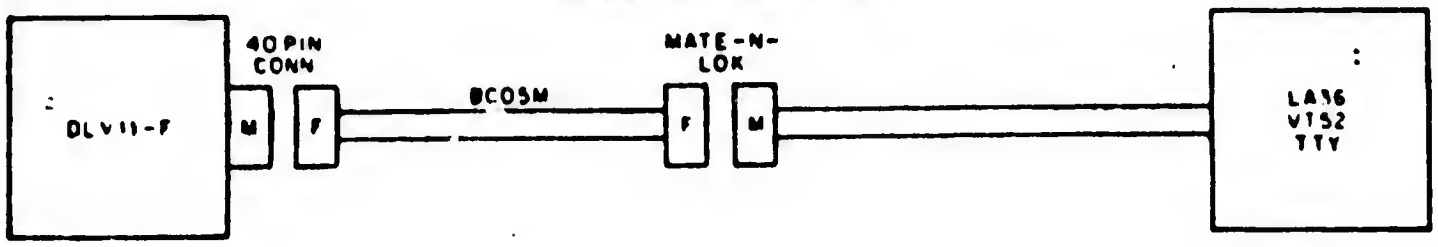
VIEW FROM MODULE SIDE OF BACKPLANE

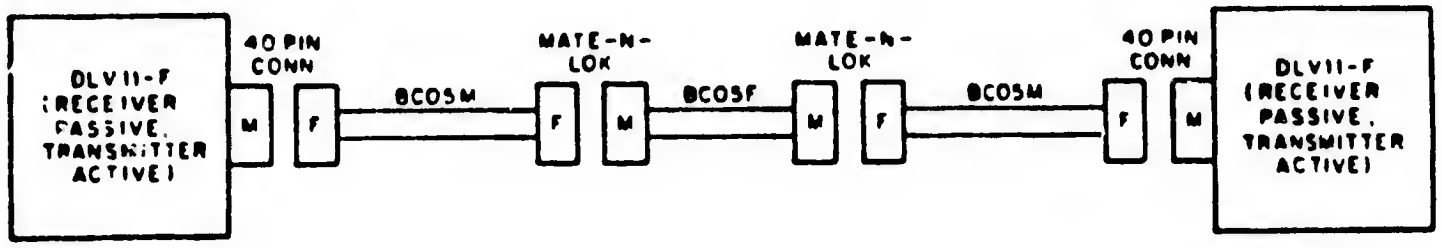


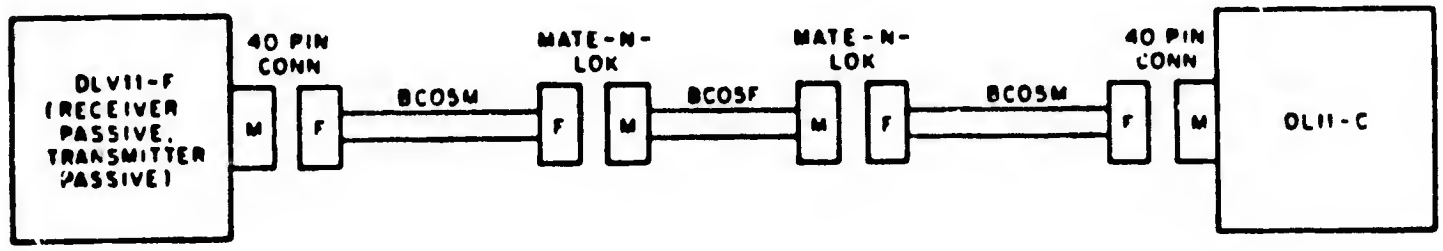
11/03

DLV11-F Cabling Examples

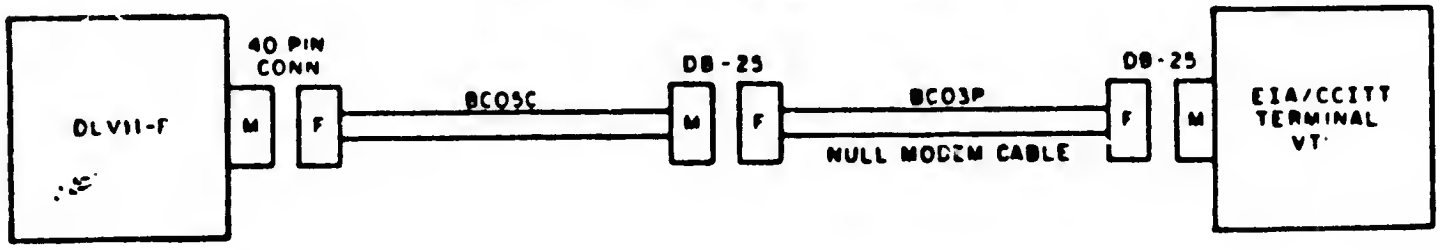
CURRENT LOOP MODE







EIA "DATA LEADS ONLY" MODE



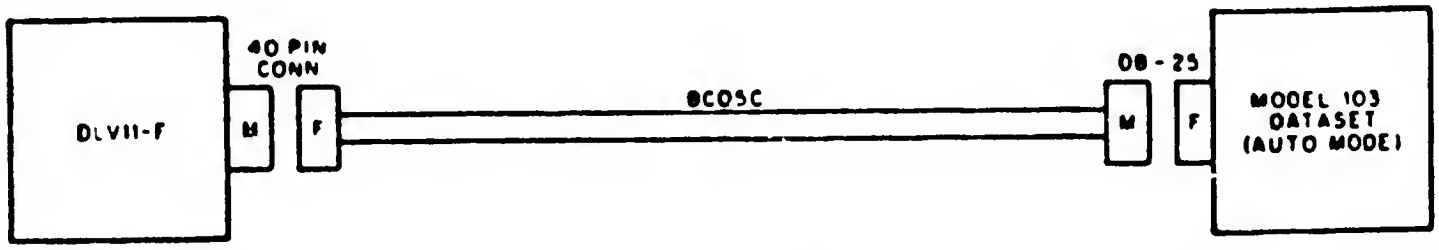


Table 4.1.1 DLV11-F JUMPER LOCATIONS

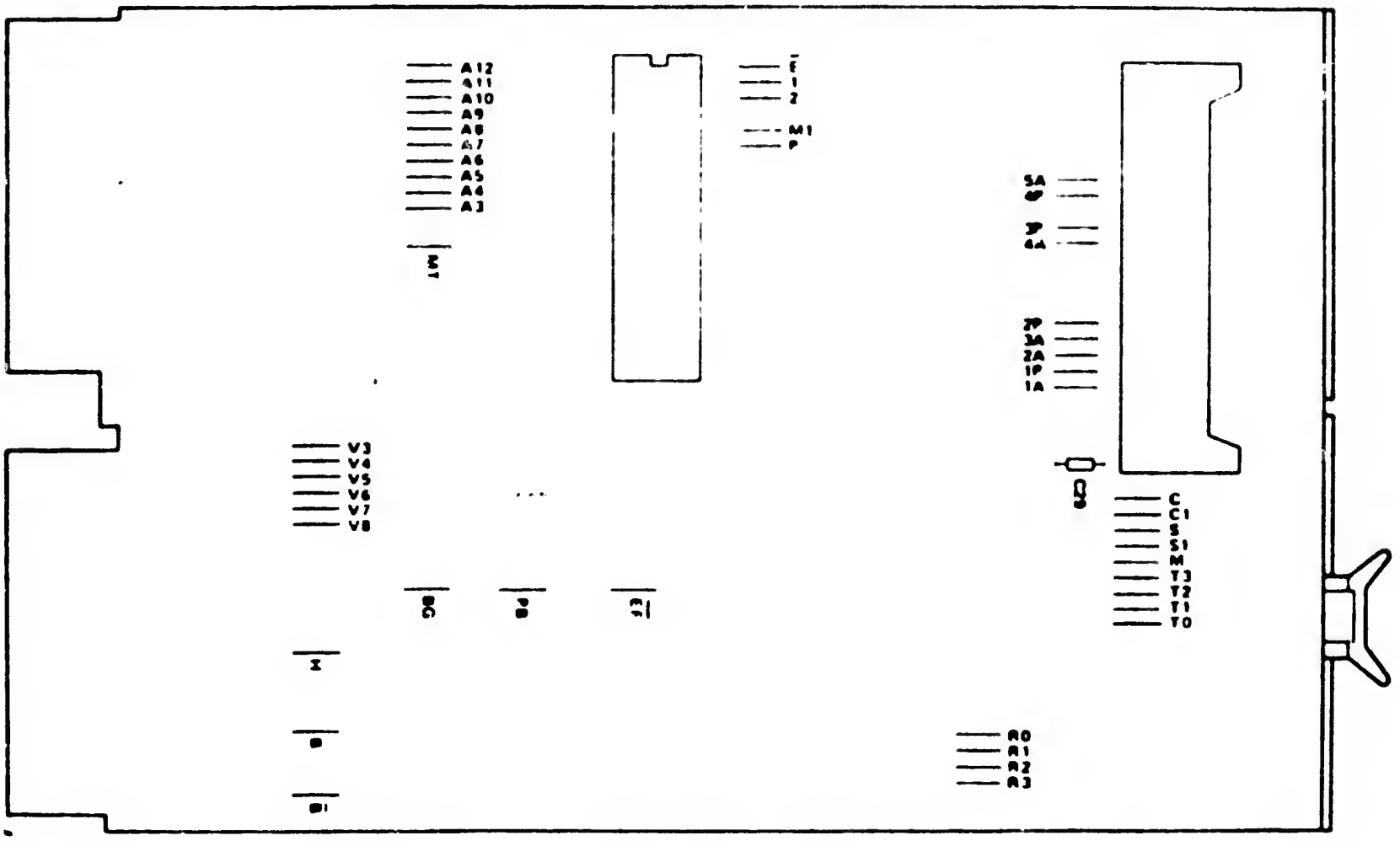


TABLE 4.1.2 JUMPER DEFINITIONS

I = Jumper inserted = program bit cleared

R = Jumper removed = program bit set

NOTE: Jumpers are inserted to enable the function they control except for those jumpers that indicate negation (such as "B") Negated jumpers are removed to enable the functions they control.

Jumper	Jumpers Installed when ship'd from Vol. Mfg.	Function
A3-A12		These jumpers correspond to bits 3-12 of the address word. When inserted, they will cause the bus interface to check for a True condition on the corresponding address bit.
A3	R	Jumpers A3 through A12 implement device address 17756X for the DLV11-F. The least significant octal digit is hard-wired on the module to address the four device registers as follows: (see table 4.1.4) X = 0 RCSR X = 2 RBUF X = 4 XCSR X = 6 XBUF
A4	I	
A5	I	
A6	I	
A7	R	
A8	I	
A9	I	
A10	I	
A11	I	
A12	I	
V3-V8		Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector address bit on the LSI-11 bus.
V3	R	This jumper selection implements interrupt vector address 60_8 for receiver interrupts and 64_8 for transmitter interrupts on the DLV11-F. See table 4.1.5.
V4	I	
V5	I	
V6	R	
V7	R	
V8	R	

Jumper	Jumpers installed when ship'd from Vol. Mfg.	Function
R0 R1 R2 R3	I R I I	The module is configured to receive at 110 baud. Receiver and transmitter baud rate select jumpers, during common speed operation. See table 4.1.3
T0 T1 T2 T3	I R R R	The transmitter is configured for 9600 baud if split speed operation is used. Transmitter baud rate select jumpers during split speed operation. See table 4.1.3
BG	I	Jumper is inserted to enable Break generation.
P	R	Jumper is inserted for operation with parity.
E	R	Removed for even parity; inserted for odd parity. Receiver checks for appropriate parity and transmitter inserts appropriate parity.
1,2	R,R	These jumpers select the desired number of data bits (see Table 4.1.4)
PB	R	Jumper is inserted to enable the programmable baud rate capability.
C,C1	I,I	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted)
S,S1	R,R	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	I	This jumper is inserted to assert BHALT L when a framing error is received. This places the LSI-11 in the halt mode.

Jumper	Jumpers Installed when Shipping from Vol. Manfg.	Function
B	R	Jumper B is inserted to negate BDCOK H when a BREAK signal framing error is received. This causes the LSI-11 to reload the bootstrap. (Jumper $\overline{B}$ must be removed when B is inserted.)
$\overline{B}$	I	
1A 2A 3A	I I I	These jumpers are inserted to make the 20MA current loop receiver active (jumpers 1P, 2P must be removed when 1A, 2A, and 3A are inserted).
1P 2P	R R	These are inserted to make the 20MA current loop receiver passive (jumpers 1A, 2A, and 3A must be removed when 1P and 2P are inserted).
4A 5A	I I	Inserted to make the 20MA current loop transmitter active (jumpers 3P and 4P must be removed when 4A and 5A are inserted).
3P 4P	R R	Inserted to make the 20MA current loop transmitter passive (jumpers 4A and 5A must be removed when 3P and 4P are inserted).
EF	I	Jumper is removed to enable the error flags to be read in the high byte of the receiver buffer.
MT	R	When inserted, enables maintenance bit.
M,M1	R,R	These are test jumpers used during the manufacture of the module. They are not defined for field use.

TABLE 4.1.3

Baud Rate Selections

	Bit	Bit	Bit	Bit	Bit	
Program Control	15	14	13	12	11*	
Receive Jumpers	R3	R2	R1	R0		Baud
Transmit Jumpers	T3	T2	T1	T0		Rate
	1	1	1	1		50
	1	1	1	R		75
	1	1	R	1		110
	1	1	R	R		134.5
	1	R	1	1		150
	1	R	1	R		300
	1	R	R	1		600
	1	R	R	R		1200
	R	1	1	1		1800
	R	1	1	R		2000
	R	1	R	1		2400
	R	1	R	R		3600
	R	R	1	1		4800
	R	R	1	R		7200
	R	R	R	1		9600

1 = Jumper Inserted = Program Bit Cleared.

R = Jumper Removed = Program Bit Set.

* Bit 11 of the XCSR (Write Only Bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

TABLE 4.1.4

Data Bit Selections

Jumpers		Number of Data Bits
2	1	
1	1	5
1	R	6
R	1	7
R	R	8

4.1.4 Address Selections

Jumpers: - inserted
R removed

Address	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
160000	-	-	-	-	-	-	-	-	-	-
160010	-	-	-	-	-	-	-	-	-	R
160020	-	-	-	-	-	-	-	-	R	-
160030	-	-	-	-	-	-	-	-	R	R
160040	-	-	-	-	-	-	-	R	-	-
160050	-	-	-	-	-	-	-	R	-	R
160060	-	-	-	-	-	-	-	R	R	-
160070	-	-	-	-	-	-	-	R	R	R
160100	-	-	-	-	-	-	R	-	-	-

4.1.5 Vector Selections

Jumpers: - inserted
R removed

Vector	V08	V07	V06	V05	V04	V03
300	-	R	R	-	-	-
310	-	R	R	-	-	R
320	-	R	R	-	R	-
330	-	R	R	-	R	R
340	-	R	R	R	-	-
350	-	R	R	R	-	R
360	-	R	R	R	R	-
370	-	R	R	R	R	R
400	R	-	-	-	-	-

5.0 TEST SET UP

5.1 No special test set up is required.

6.0 POWER CHECKS

6.1 Power Requirements

+5V ± 5% @ 1.0A (.0W)
+12V ± 5% @ 150 ma (5.0W)

NOTE: -12V is generated internally on the M8028 from +12V supply.

6.2 Bus Loading

Each DLV11-F places one (1) Bus load on the Q Bus as defined by the LSI-11 Q Bus spec. (DEC STD 160).

7.0 DIAGNOSTIC TEST PROCEDURE

7.1 The DLV11-F does not come with a turnaround connector as does the DLV11-E. Because of this, the DLV11-F will only be tested in the internal maintenance mode.

7.2 Diagnostic Test

7.2.1 After the DLV11-F has been checked for proper jumper configuration load CVDVC through appropriate load media.

7.2.2 Starting program

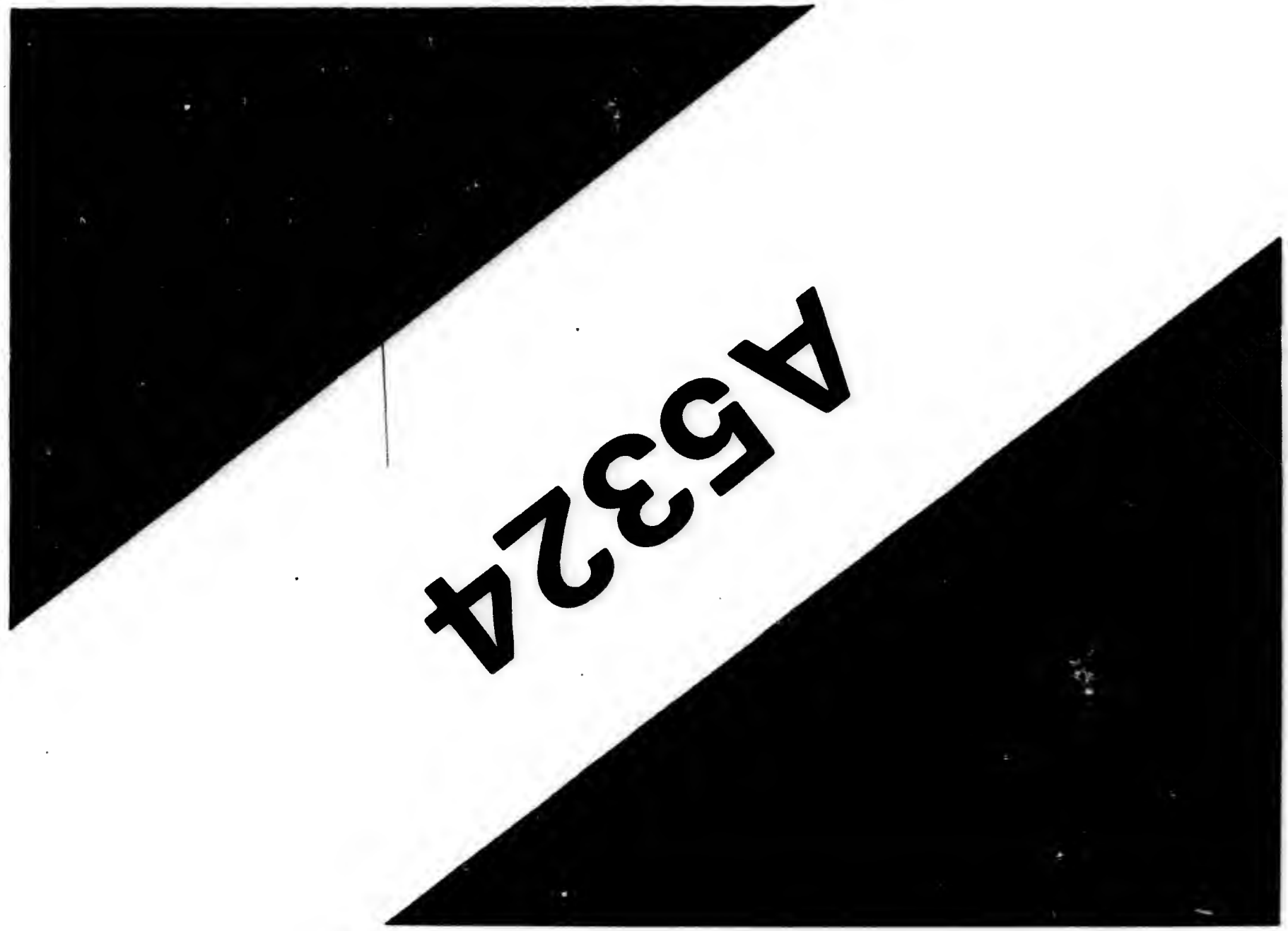
7.2.2.1 After checking available switch settings (7.2.3), start the program.

7.2.2.2 200G

7.2.3 Available switch settings

Bit 15 - Halt on error
14 - Loop on test
13 - Inhibit error
12 - (unused)
11 - Inhibit iterations
10 - Bell on error
9 - Loop on error
8 - Loop on test in SW (7:0)
7-0 - Test number to loop on (used with Bit 8)

7.2.4 End of pass is indicated by a type out.


A53
=324

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 9/4/79

TITLE M.A.S.T. DLV11-J Four Line Serial Interface

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	Added Appendix A (pp. 15-16) to include the H3171 Distribution Panel ECO CHANGE	MA-MA0000 ML006	T. JELENIEWSKI	9-79	Tom Jeleniewski (Test)	10-1-80

4

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Ayotte	Tom Edwards	A	SP	MA-A5324-0-0	C

DLV11-J FOUR LINE SERIAL INTERFACE

1.0 INTRODUCTION

This procedure establishes the minimum test requirements that a DLV11-J must meet to be considered acceptable for customer shipments from Systems Manufacturing.

1.1 Description

The DLV11-J is an asynchronous line interface module that interfaces the LSI-11 Bus to 4 serial communications lines. The DLV11-J is a dual-height module with E.I.A. operation. 20MA operation is available when the DLV11-KA is used in conjunction with the DLV11-J. Although each line can be configured to operate at different baud rates, no split baud rates are possible.

Option	Qty/Contents	Description
DLV11-J	1-M8043	Module

2.0 REFERENCE DOCUMENTATION

2.1 Print Set MP00586

2.2 Users Guide EK-DLV1J-UG-???

2.3 Lib Kit ZJ-269-RB

2.4 Ship List - Reference should be made to System Manufacturing Ship List, not Engineering Ship List.

2.5 Packaging - A - PS-9905622-0-0

3.0 REQUIRED TEST EQUIPMENT

3.1 PDP 11/03 with a minimum of 4K of memory and one available slot.

3.2 Scope: 465 or equivalent

3.3 For power requirements, refer to Section 7.0 D.V.M. with 3 digits

3.4 Wire wrap gun (OK speed wrap model #BW-515BF) or equivalent.

3.5 Unwrapping tool - hand type, unwrapping tool

3.6 H3270-A (turnaround connectors) are needed for device testing. (See Section 6.1)

4.0 AVAILABLE DIAGNOSTIC PROGRAMS

4.1 Kit # ZJ269-RB CVDLA - DLV11-J Test, paper tape and listing

5.0 SPECIAL INSTRUCTIONS

5.1 Caution #1 - When changing wire wrappings, always use equipment designed for that purpose, and that is calibrated. Note Section 2.4 and 2.5 for type of equipment.

5.2 Caution #2 - All wire wrapping must be done to Digital's workmanship standard; DEC Std 116. Reference should be made to Section 3. in that text.

6.0 INSTALLATION INSTRUCTIONS

6.1 Option Add-On

The DLV11-J may not require changes to the jumpers as it was configured from Volume Manufacturing. (Refer to Diagram 6.1.1 for jumper configuration). The DLV11-J Line 3 is configured for console device addresses 177560 - 177566 and vectors 60 and 64. For jumper definitions, refer to Table 6.1.2. DLV11-J is capable of being tested with Channel 3 in console mode. No changes will be required to the module when Channel 3 is console. This requires an EIA terminal or a DLV11-KA (EIA-20ma) option/20ma terminal to be used. This configuration will require the turn-around connectors mentioned in Section 3.6 to be used in Channels 0, 1, 2. Refer to Section 6.6 for addition of 2-DLV11-J.

If the above terminal equipment is not available, the DLV11-J is to be run with all 4 lines turned around using the turn around connectors mentioned in Section 3.6. This will require the DLV11-J be configured so all lines will be consecutively addressed and no console selected. Refer to Diagram 6.1.1. Table 6.1.2. and Section 8 for proper diagnostic setup when in this configuration. The following is a list of changes required to the DLV11-J so it may be run with 4 lines wrap-around:

V5 = Removed

C1 = X to 0

C2 = X to 0

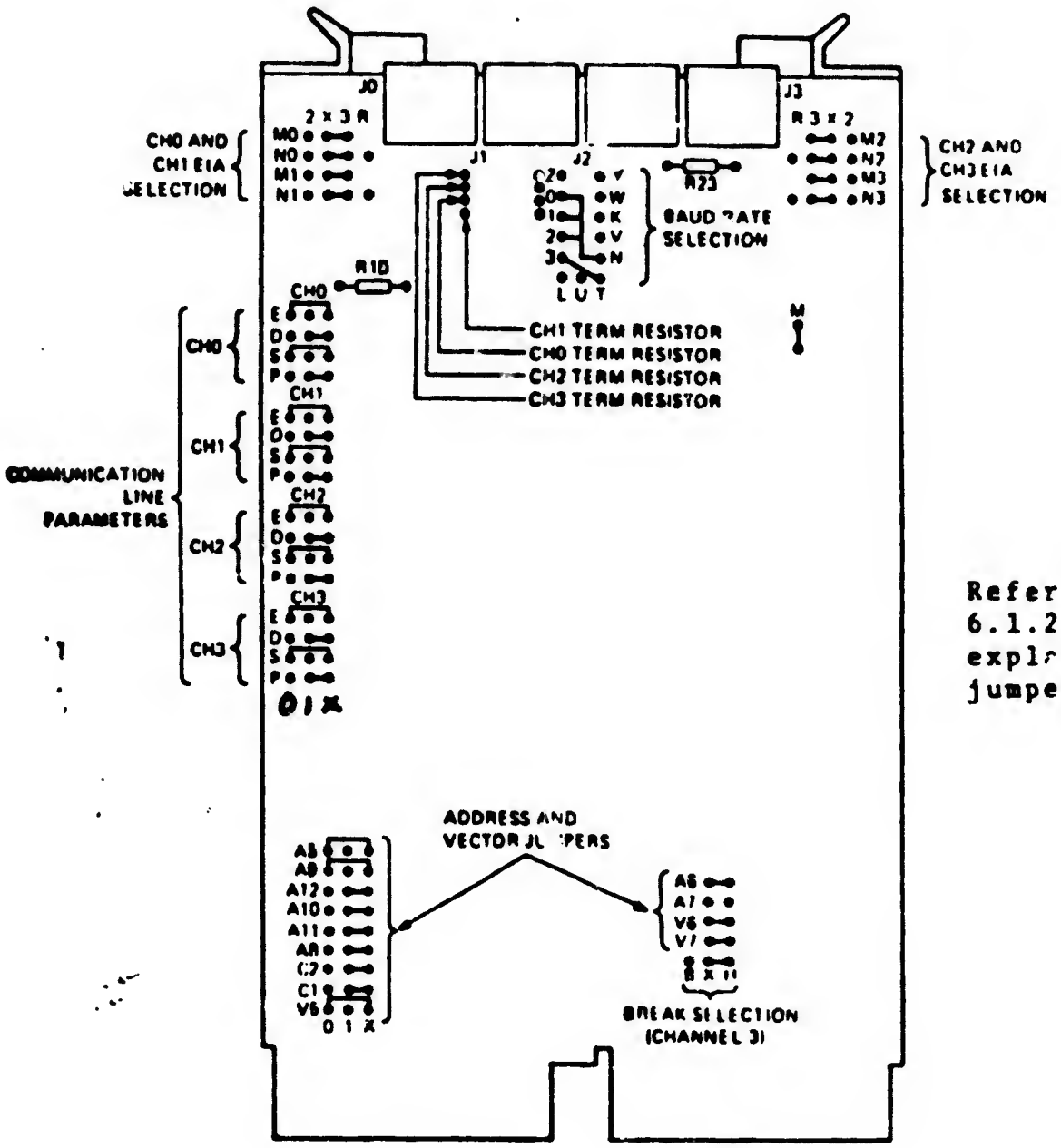
X to H = Removed

Diagnostic location 1220 must be 21 as defined in Section 8.2.4.2.

X - Base Pin for function

0 - Logical 0 Pin

1 - Logical 1 Pin



Refer to Table 6.1.2 for pin explanations & jumper definitions.

Diagram 6.1.1
DLV11-J Jumper Configuration
When Supplied By Volume Manufacturing

6.1.2 Jumper Definitions

R = Removed

I = Inserted

JUMPER	CONF. SHIP'D FROM VOL MFG.	FUNCTION
		Address
A5-A12		These jumpers correspond to Bits 5-12 of the address word for Channel C. The least significant digit is decoded on the module during operation to address one of four serial line units device registers as follows: X = 0 RCSR X = 2 RBUF X = 4 XCSR X = 6 XBUF
A12	X to 1	This arrangement of jumpers implements the octal base device address 176500 for Channel 0 from which Channels 1 and 2 are automatically determined on the module.
A11	X to 1	
A10	X to 1	
A9	X to 0	
A8	X to 1	
A7	R	
A6	I	
A5	X to 0	
		Console Address Selection
C1 and C2		These jumpers allow the configuration of the last four addresses used on Channel 3 to be assigned to the console addresses 177560-177566. The preceding addresses of Channels 0, 1, and 2 are not affected.
C1	X to 1	C1 and C2 set to enable Channel 3 for console operation. The base address must be 176500, 176540, or 177500. If not set, Channel 3 will default to next consecutive address from Channel 2. (X to 0)
C2	X to 1	

6.1.2 Jumper Definitions cont.

JUMPER	CONF. SHIP'D FROM VOL MFG.	FUNCTION
Break		This can enable the use of a break response while Channel 3 is in console mode, or for bootstrap response.
Halt	X to H	Jumper set to enable break generation.
Boot	B to X	Jumper has to be disabled when break is set. Remove jumpers when Channel 3 is not console.
		Vectors
V5 - V7		Used to generate the vector during an interrupt transaction. V6 and V7 designate the base vector address and V5 determines the console vector for Channel 3.
V7	I	This arrangement implements the octal base vector of 300 and Channel 3 at 60 and 64. With V5 removed, the vector addresses for Channel 3 will be 330 and 334.
V6	I	
V5	X to 0	
		Parity, Data Bits, Stop Bits, Odd/Even Parity
P,D,E,S		Each channel (communication line) is capable of being set for individual line operation. D enables 7 or 8 data bits, E allows even or odd parity, P allows parity generation or no parity generation, S enables one or 2 stop bits.
D	X to 1	This allows 8 data bits to be used. For 7 data bits, insert Jumper X to 1.
S	X to 0	Jumper inserted for 1 stop bit. For 2 stop bits, insert Jumper X to 1.
P	X to 1	With this jumper inserted, parity generation and detection is disabled. For parity operation, insert jumper X to 0.

6.1.2 Jumper Definitions cont.

JUMPER	CONF. SHIP'D FROM VOL MFG.	FUNCTION
E	X to 0	Selects odd parity or even parity. Insert Jumper X to 1. NOTE: P Jumper must be X to 0 for selection of odd/even parity, and E must always be in odd or even state; never removed.
0,1,2,3		**Baud Rates** One baud rate wire wrap pin is provided for each channel. These numbers correspond to the respective lines. Both transmitter and receiver operate at the selected speed. To determine the baud rate for a channel, connect the jumper to the channel desired, and the other end to the desired baud rate pin (reference list below). Wire Wrap Pin Label / Baud Rate Bits/Sec. U 150 T 300 V 600 W 1200 Y 2400 L 4800 N 9600 K 19200 Z 38400 NOTE: If more than one channel requires the same baud rate, wire wrap jumpers may be daisy chained.
	Effective	Actual
0	0 to N	Configured for 9.6K baud 0 to 1
1	1 to N	Configured for 9.6K baud 2 to N
2	2 to N	Configured for 9.6K baud 1 to 2
3	3 to T	Configured for 300 baud

6.1.2 Jumper Definitions cont.

JUMPER	CONF. SHIP'D FROM VOL MFG.	FUNCTION
M	I	Maintenance Bit (not for Systems Manufacturing usage)
NO-N3 MO-M3		These jumpers determine if EIA (RS-422, RS423/RS232C]) or 20ma operation will be used.
NO-N3 MO-M3	X to 3 X to 3	These jumpers are inserted so the DLV11-J will be compatible for both EIA RS-423 and RS-232C simultaneously. For other configurations, see below: NOTE: When EIA RS-423 and RS-232C configuration is used, no termination resistors are to be installed. R10 and R23 must be installed. EIA RS-422 Operation 1) NO-N3 connect X to 2 2) MO-M3 connect X to 3 3) R10 and R23 are not required. 4) Terminating resistors R33 (CH3), R32 (CH2), R30 (CH0), R31 (CH1) are required to be 100 OHM ¼ watt, non-wire wound fusible resistors. P/N 13-00229-00 20MA Current Loop (Requires operation with DLV11-KA option) 1) NO-N3 connect X to R.(for program controlled paper tape reader) 2) MO-M3 Connect X to 3. 3) No termination resistors required. 4) R10 and R23 must be installed.

6.1.2 Jumper Definitions cont.

JUMPER	CONF SHIP'D FROM VOL MFG	FUNCTION
R10,R23		The value of Resistor R10 determines the slew rate of both channels 0 and 1, which are simultaneously set to the same value. Similarly, R23 controls the slew (settling) rate of both channels 2 and 3. These resistors are not required for operation in EIA RS-422.
R10	22K OHM	Channels 0 and 1
R23	22K OHM	Channels 2 and 3
		For selecting the correct value ½" non-wire wound resistor. For R10 and R23, use list below:

Resistor	P/N	Baud Rate
22K	13-01808-00	38.4K
59K	13-00525-00	19.2K
120K	13-00539-00	9.6K
200K	13-14516-00	4.8K
430K	13-14649-00	2.4K
820K	12-03187-00	1.2K
1 MEG. OHM	13-09595-00	600 300 150 110

NOTE: If channels 0 and 1 are split baud rates the resistor value defalts to the higher baud rate. This holds true for channels 2 and 3.

6.2 System Installation

When the DLV11-J is being installed in a customer system, it may be necessary to change the jumpers as they were shipped from Volume Manufacturing. When configuring, refer to Diagram 6.1.1 and Table 6.1.2 to assure proper installation. Reference 6.1 for proper test set up.

6.3 The DLV11-J has many possible cabling configurations. Diagram 6.3.1 is an example of EIA interfacing and Diagram 6.3.2 is an example of 20MA interfacing.

NOTE: Remember that these are only examples, and are not necessarily all the possible combinations.

6.4 When installing the DLV11-J, do not leave any open slots between the processor module or memory and the DLV11-J. The priority for each option is determined by how close that option is installed to the processor modules. The closer to the processor you get, the higher priority the option has.

6.5 20MA Operation

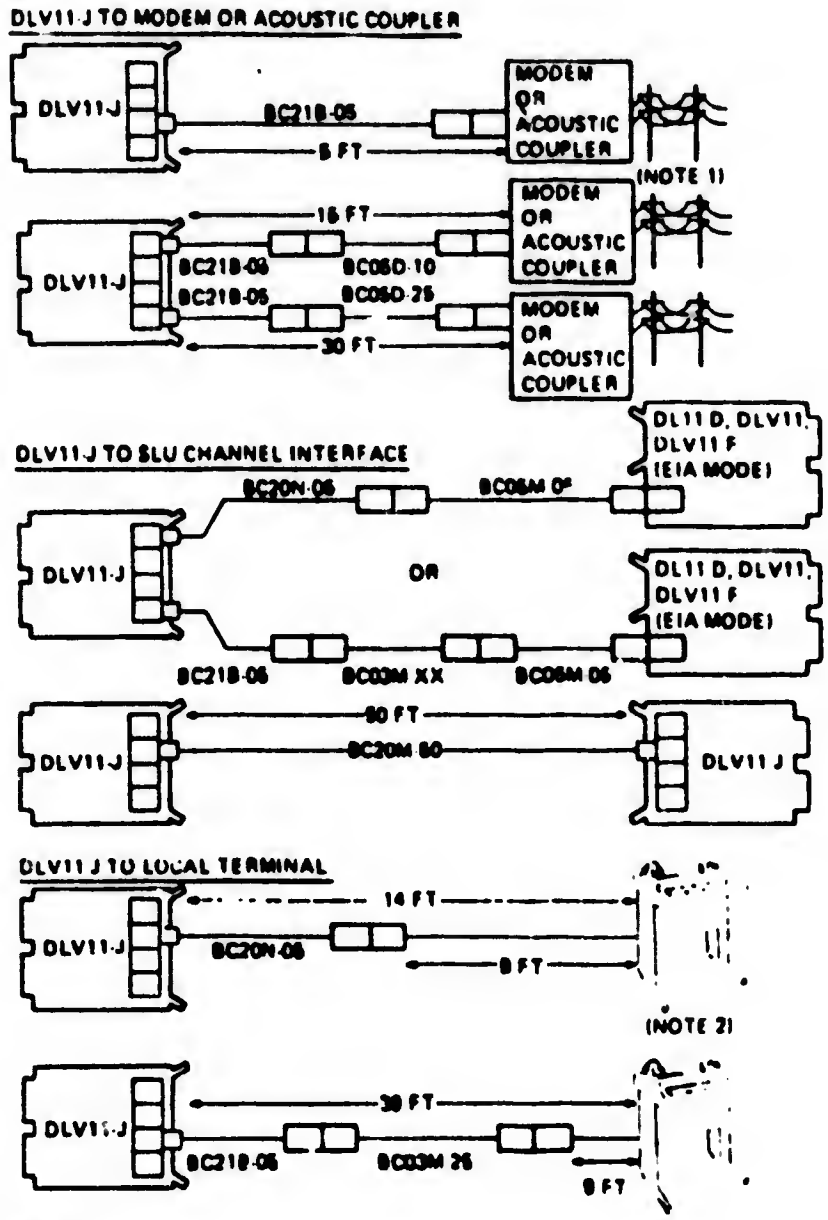
The DLV11-J is capable of interfacing with 20MA when used with a DLV11-KA option.

Option	Qty/Contents	Description
DLV11-KA	1-BC21A-03	Cable
	1-DLV11-KB	EIA to 20MA converter
DLV11-KB	1-EIA to 20MA Converter	

Configure the DLV11-J for 20MA operation as described in Section 6, using Diagrams 6.1.1, 6.1.2, and 6.3.2.

A 110 baud rate clock generator circuit is contained on the optional DLV11-KA 20 MA option. When 110 baud operation is desired, do not connect the baud rate jumper on the DLV11-J module for that particular channel. The 110 baud clock will be supplied by the DLV11-KA option through the interface connector.

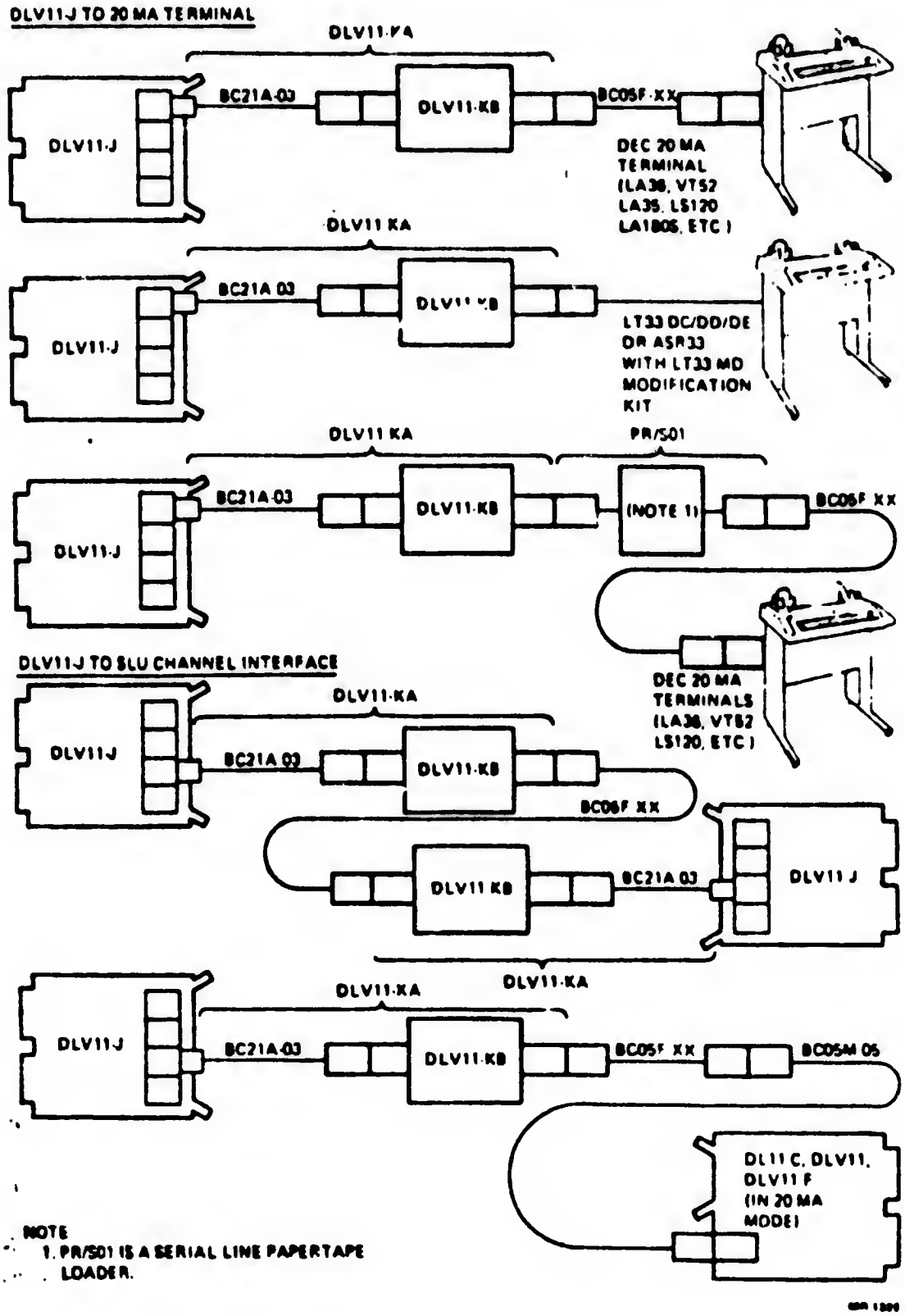
6.6 Additional DLV11-J
When the first DLV11-J is used as console and another DLV11-J is to be used as 4-additional lines the starting address is the Base Address of the first module plus 30 and the Vector is the Base Address of the first module plus 30.



NOTES
1. MODEM USED IS A "MANUAL TYPE" SUCH AS BELL 103A WITH 8048.
2. DEC EIA RS-232C TERMINALS (VT52, LA36, LS120, ETC.) COME EQUIPPED WITH A 8 FT CABLE. NON-DEC EIA RS-232C TERMINALS ARE CONNECTED SIMILARLY EXCEPT 8 FT OF LENGTH MUST BE DEDUCTED FROM THE TOTAL CABLE LENGTH.

Diagram
6,3,1

TITLE MODULAR APPROACH TO SYSTEMS TEST - APPENDIX A



NOTE
1. PR/501 IS A SERIAL LINE PAPERTAPE LOADER.

Diagram
6.3.2

	SIZE	CODE	NUMBER	REV
	A	SP	MAA5324-0-0	C

7.0 POWER CHECKS

7.1 Power Requirements

+5V ± .25V@ 1.0A typ. (1.25A max.)

+12V ± .36V@ 0.15A typ. (0.2A max.)

7.2 +12V is present on Pin 10 of each channel. This line is provided for the DLV11-KA option operation.

7.3 Bus Loading

Each DLV11-J places (1) AC and (1) DC Bus load on the Q Bus as defined by the LSI-11 Q Bus Spec. (DEC Std 160).

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 The DLV11-J can be tested 3 different ways as specified in Section 6.1. Reference should be made to that section for proper installation and configuration before diagnostics are run.

NOTE: If the DLV11-J is configured for 4 additional lines, the diagnostic must be loaded with another device as console. Diagnostic program must be modified at Loc 1220 ($USWR).

8.2 Starting Program

8.2.1 Load (CVDLA) diagnostic through appropriate load media. When running under APT loc 1220 ($USWR) must be 31 as defined in Section 8.2.4.2

8.2.2 Start: Refer to Section 8.2.4.1 for available switch register settings. Refer to Section 8.2.4.2 for configuration options program changes.

8.2.3 Initial system type 200 G.

8.2.4.1 Software Switch Register Options

Bit 15 set = 100000 = Halt on Error
14 set = 40000 = Loop on test (when testing in process)
13 set = 20000 = Inhibit error type outs
12 set = 10000 = Enable performance reports
11 set = 4000 = Inhibit iterations
10 set = 2000 = Bell on error
9 set = 1000 = Loop on error
8 set = 400 = Loop on test in SWR <7:0>
7:0 = Number of test to loop on (used with bit 8). All tests previous to the selected test are executed first with one iteration only.

8.2.4.2 Options

$USWR is at location 1220 in the program. Location $USWR contains all the user selectable options. The values in this word must conform to the actual board configuration.

BIT POSITION	DEFINITION	$USWR DEFAULT VALUE
0	# of data bits transmitted 0 - 7 bits, 1 = 8 bits	1 = 8 Bits
1	Parity enabled	0 = NO
2	Even odd parity	0 = ODD
3	Break generation enabled	1 = YES
4	Run data wrap around tests	1 = YES
<11:9>	Console Device	1 = YES = console on module 1 Channel 3
<11:9> = 0	= No console selected	
<11:9> = 1	= Console on Module 1	
<11:9> = 2	= Console on Module 2	

IMPORTANT NOTE: For diagnostic purposes, all channels must be configured the same, either 7 or 8 bits.

8.3 End of Pass is indicated by a type out with no errors.

APPENDIX A

H3171 DISTRIBUTION PANEL

The H3171 Distrbution panel relinquishes the need to use four separate BC21B cables with the DLV11-J. It occupies 1.75 inches of panel space in a standard 19 inch rack. The H3171 incorporates an H7004 static filter to improve the R.F. integrity of the system. There are two mechanical configurations available. They are as follows:

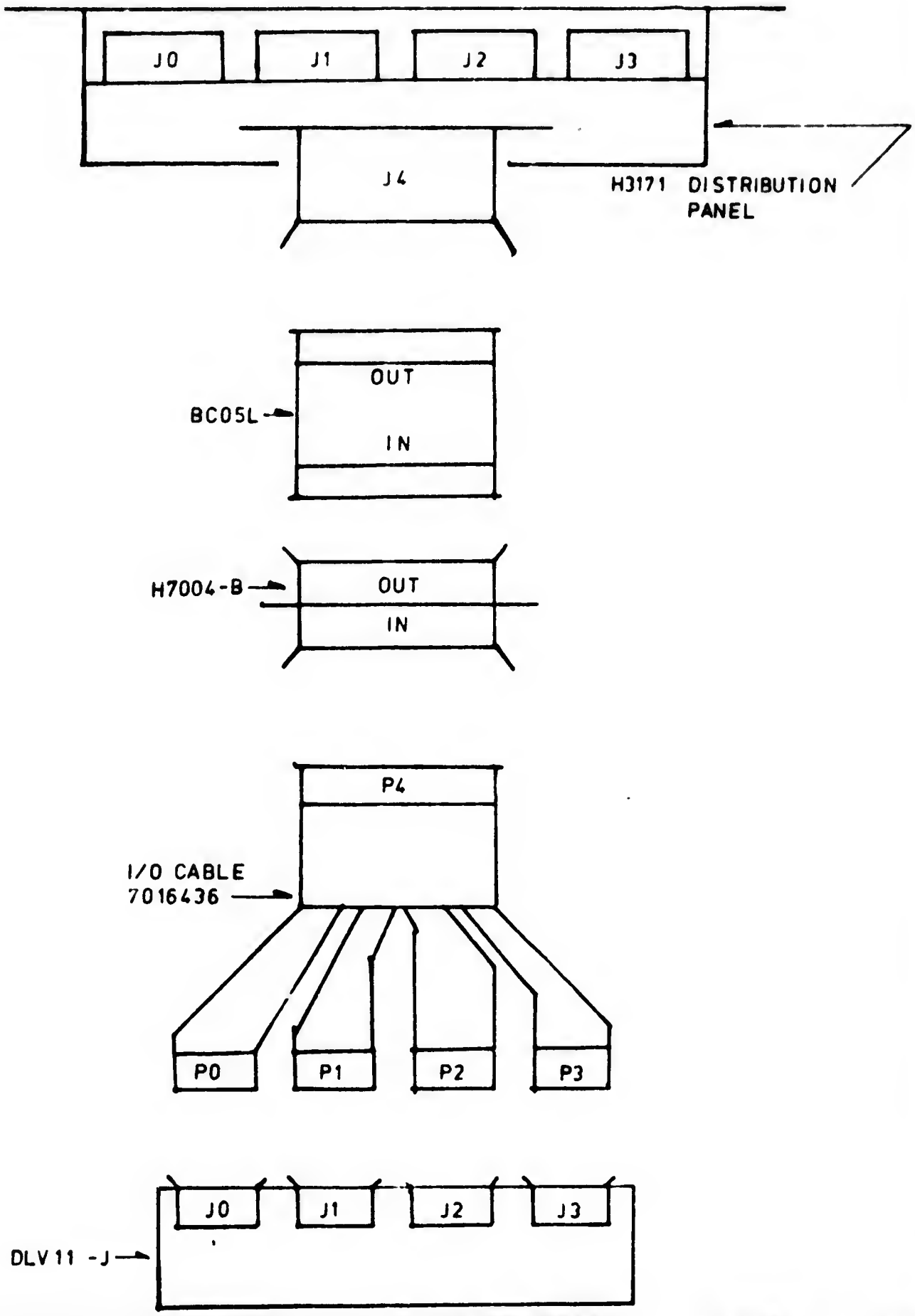
A) H3171-A (Separate Filter)
This configuration is used in conjunction with CPU boxes that have a mounting bracket for static filters built directly into them. In this case the H3171 distribution panel itself contains no filter. The filter is located on the CPU bracket.

B) H3171-B (Integral Filter)
This configuration is used in conjunction with CPU boxes that do not contain a bracket for static filters. In this case the H3171 chassis is elongated to accept the static filter directly onto the distibution panel.

Each H3171 consists of 4 major assemblies. (See figure 1 in Appendix A)

1) Distribution Panel / Chassis (includes output connectors)
2) BC05L Cable
3) H7004-B Filter
4) I/O Cable (7016436)

FIG 1


J0
J1
J2
J3
J4
H3171 DISTRIBUTION PANEL
OUT
BC05L
IN
OUT
H7004-B
IN
P4
I/O CABLE
7016436
P0
P1
P2
P3
J0
J1
J2
J3
DLV11 -J

A5330

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 3/10/80

TITLE M.A.S.T. DL11-W

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	Update old Back-up	MA-A0000-ML009	L. ELCLERC	8-80	S. ESTES	8-80

3

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Ayotte	Stan Estes	A	SP	MA-A5330-0-0	B

DL11-W

1.0 INTRODUCTION

The DL11-W is a single line asynchronous communication interface to the PDP11 Unibus. The DL11-W contains the functionality of the DL11-A, -B, -C, and -D options. The DL11-W also contains a line frequency real time clock (RTC) used for timed interrupts and software timekeeping.

The serial line unit (SLU) portion of the DL11-W has such features as split speed, odd/even/no parity select, active/passive 20 ma. interface, EIA RS232C (data only) interface, and a 5 to 8 bit character length. These parameters and features are switch selectable.

2.0 REFERENCE DOCUMENTATION

2.1 Manuals & Engineering Specifications

2.1.1 DL11-W SLU/RTC Maint. Manual EK-DL11W-MM

2.2 Prints & Schematics

2.2.1 Field Maintenance Print Set MP00106

3.0 REQUIRED TEST EQUIPMENT

3.1 Hardware and Media

3.1.1 PDP11 system with 8K of memory
3.1.2 Quad SPC slot
3.1.3 DVM accurate to .01V at 15VDC
3.1.4 EIA or 20 ma. terminal

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 FLOAT PROGRAM ..... DZFLA
4.2 DL11-W DIAGNOSTIC ..... CZDLD

5.0 SPECIAL INSTRUCTIONS

The DL11-W is comprised of a quad height module (M7856), which plugs into a PDP11 SPC slot. The four option variations are listed below:

OPTION	DESCRIPTION
DL11-W	M7856 SLU/RTC Module
DL11-WA	DL11-W, 70-08360-01 20 ma. Cable
DL11-WB	DL11-W, BC05C-25 EIA Cable
DL11-WC	DL11-W, BC03L-10 filtered panel mount EIA Cable.

6.0 INSTALLATION AND TEST SET-UP INSTRUCTIONS

The M7856 Module has many features and several operating modes which must be configured via the 5 switch packs prior to installation. Refer to FIGURE 1 for switch location.

6.1 FLOAT PROGRAM

6.1.1 Run the FLOAT program (DZFLA) to determine the correct address and vector settings for the DL11-W(s). Note that this only applies to DL11-W's that are not used for consoles.

6.2 MODE & ADDRESS SELECTION

6.2.1 The M7856 Module may be run in one of 3 modes:

MODE 1 - As a console interface with the RTC enabled. The SLU address is 777560 and the RTC address is 777546.

MODE 2 - As a SLU ONLY with the RTC DISABLED. The SLU address range is 774000 to 777770.

MODE 3 - As a RTC ONLY with the SLU DISABLED. The RTC address is 777546.

*** NOTE ***

For DL11-W's which will NOT use the RTC logic, remove R63. See FIGURE 1 for location.

Refer to TABLE 1 for switch selection of ADDRESS and MODE.

6.3 VECTOR ADDRESS SELECTION

6.3.1 Vector address selection is accomplished by setting the switch pack S2. The DL11-W uses three vectors: one for the receiver, one for the X-mitter, and one for the real time clock. The X-mitter vector (XX4) is automatically selected when the receiver vector (XX0) is set. If the DL11-W is being used as a console, the receiver vector should be set to 60. The vector for the RTC is fixed at 100. Refer to TABLE 2 for switch settings.

6.4 BAUD RATE SELECTION

6.4.1 Split speed on the M7856 may be attained by setting the transmit and receive speed select switches to their desired values. If split speed is not desired, set the transmit and receive select switches to the same speed settings. Refer to TABLE4 for the switch settings.

6.5 20 ma. ACTIVE/PASSIVE OPERATION

6.5.1 If the DL11-W is to be used as a 20 ma. interface, the X-mitter, receiver, and paper tape reader enable functions must be set as either ACTIVE or PASSIVE. The normal setting is for active transmitter, active receiver, and active paper tape reader enable. Refer to TABLE 5 for these switch settings.

6.6 MISCELLANEOUS SWITCH FUNCTIONS

6.6.1 The BREAK ENABLE function is selected by setting SW4-1 ON. The normal setting is OFF.

6.6.2 ODD PARITY is selected by setting SW4-2 ON. (See 6.6.5) The normal setting is ON.

6.6.3 CHARACTER LENGTH is selected by SW4-3 and -4 (Refer to TABLE 3). The normal settings are OFF.

6.6.4 STOP BITS are selected by SW4-5. ON=1 stop bit, OFF=2 stop bits. (1.5 stop bits if 5 bits per character) The normal setting is OFF

6.6.5 PARITY is enabled if SW4-6 is ON. The normal setting is ON.

6.7 Install the M7856 Module in a Quad SPC slot and connect the cable to the berg connector on the module.

6.8 Connect an appropriate terminal (EIA or 20 ma.) to the DL11-W.

7.0 POWER CHECKS

7.1 Verify the presence of the following voltages at the module pins indicated:

VOLTAGE	MODULE PIN
+5VDC +/- .25V	CA2
+15VDC +/- .75V	CU1

8.0 DIAGNOSTIC TEST PROCEDURE

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria, e.g.: Pass Counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the "CHECKLIST".

The DL11-W diagnostic contains three separate tests which are to be run on the serial line unit. Testing of the real time clock is done in the DATA TEST.

8.1 DL11-W DATA TESTS ..... CZDLD

8.1.1 The DATA TEST is capable of testing the console interface and up to 15 consecutively addressed and vectored SLU's. The diagnostic assumes the following parameters: the console address is 777560 and the vector is 60. The first of any additional SLU's is addressed at 776500 and vectored at 300. The diagnostic will autosize any DL11-W's which fall within this range.

8.1.2 Start the DATA TESTS at address 200 and set the switch register for the desired functions.

SWITCH	FUNCTION
15	Set to halt on error
14	Set for scope loop
13	Set to inhibit error typeout
12	Unused
11	Unused
10	Set to enable error flag tests
9	Set to loop on error
8	Set to enable break function tests
7	Set to enable data tests with turnaround (H315)
6	Set to inhibit RTC tests (console only)
5	Set to set-up device map (inhibit auto-size)
4	Set to inhibit SLU tests

8.1.3 The console will report the number of units being tested and an END-OF-PASS message will be printed after all units have been tested.

8.2 DL11-W ECHO TEST ..... CZDLD

8.2.1 To run the ECHO TEST on the console terminal, start at address 204. An asterisk (*) will be printed at the terminal to indicate that the test has started. Type a few printable characters at the terminal and verify that they are echoed back to the terminal correctly.

8.2.2 If the unit under test is not the console interface, it will be necessary to modify the following program locations to reflect the parameters of the unit under test. Make sure a terminal is connected to the DL11-W.

NAME	LOCATION	CONTENTS
CRCSR	2654 *	Address of receiver status register
CRBUF	2656	Address of receiver buffer register
CTCSR	2660	Address of transmitter status register
CTBUF	2662	Address of transmitter buffer register
CRVECT	2664	Receiver vector
CRPSW	2666	Receiver vector plus 2 (PSW)
CTVECT	2670	Transmitter vector
CTPSW	2672	Transmitter vector plus 2 (PSW)

* - CZDLD REV D

8.2.3 Run the ECHO TEST as described in step 8.2.1. Repeat step 8.2.2 for every DL11-W to be tested.

8.3 CHARACTER TEST ..... CZDLD

8.3.1 To run the CHARACTER TEST on the console terminal, start at address 210. The terminal will print 32 characters per line and will repeat every third line. Typing any character at the terminal will halt the test. A typical pattern is shown below:

```
!"#$%&'()*+,-./0123456789:;<=>?
@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_
`abcdefghijklmnopqrstuvwxyz{|}~
```

8.3.2 If the unit under test is not the console interface, it will be necessary to modify the following program locations to reflect the parameters of the unit under test. Make sure a terminal is connected to the DL11-W.

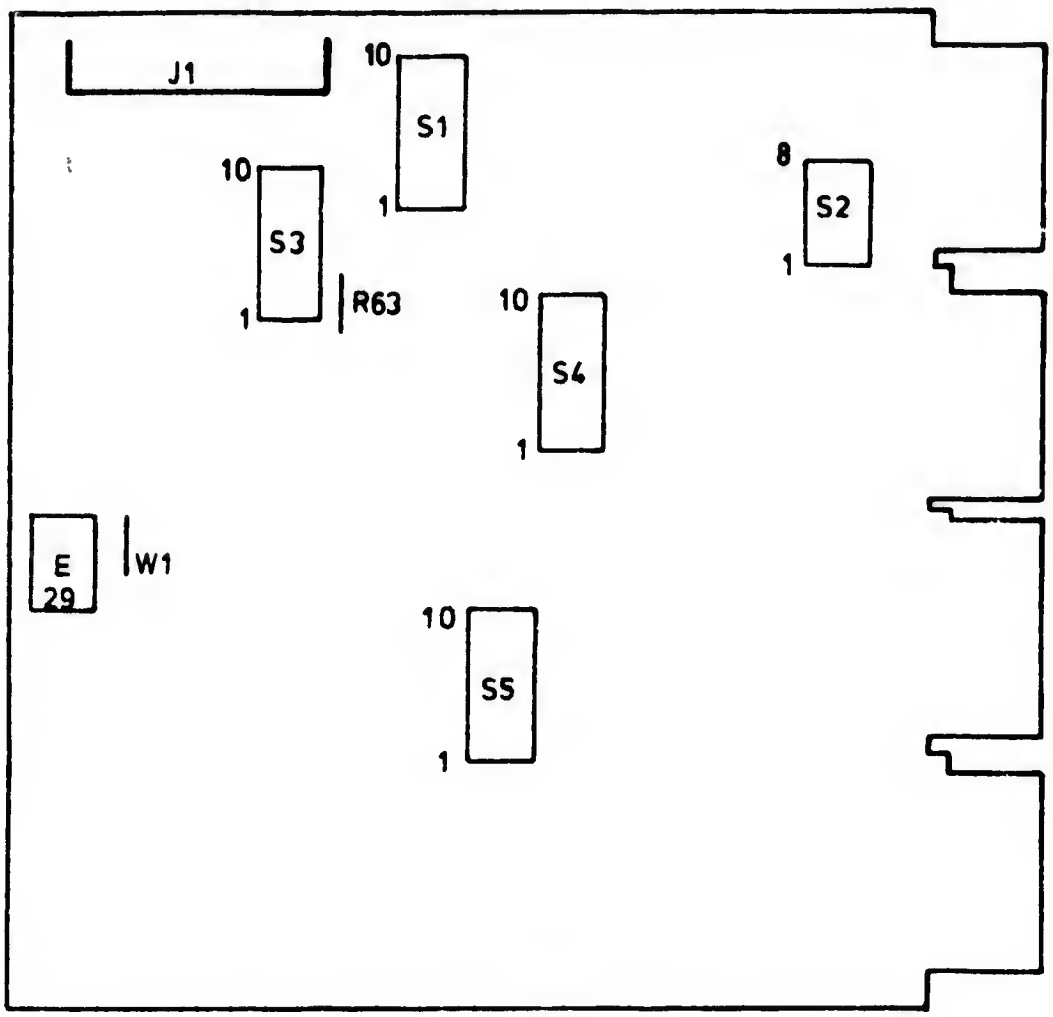
NAME	LOCATION	CONTENTS
CRCSR...	2654 *	Address of receiver status register
CRBUF...	2656	Address of receiver buffer register
CTCSR...	2660	Address of transmitter status register
CTBUF...	2662	Address of transmitter buffer register
CRVECT..	2664	Receiver vector
CRPSW...	2666	Receiver vector plus 2 (PSW)
CTVECT..	2670	Transmitter vector
CTPSW...	2672	Transmitter vector plus 2 (PSW)

* - CZDLD REV D

8.3.3 Run the CHARACTER TEST as described in step 8.3.1. Repeat step 8.3.2 for every DL11-W to be tested.

FIGURE 1

M7856 MODULE LAYOUT



NOTES -

R63 must be removed if the RTC is disabled.

The Berg connector, J1, contains a 70-0860 cable for the DL11-WA option; a BC05C-25 for the DL11-WB option and a BC03L-10 for the DL11-WC option.

Jumper W1 must always be installed.

TABLE 1

ADDRESS AND MODE SELECTION TABLE

ADRS BIT	A10	A09	A08	A07	A06	A05	A04	A03	LTC	LTC
SW S5	-3	-2	-1	-4	-5	-6	-8	-7	-9	-10
MODE 1	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
MODE 2	--	--	--	--	--	--	--	--	ON	OFF
MODE 3	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON

NOTES - A switch set to ON equals a logical 0 and a switch set to OFF is equal to a logical 1.

The switch settings for mode 1 selector an address of 777560 (console) and the RTC (or LTC) address is 777546.

The address switch settings for mode 2 are user defined to select any address from 774000 to 777770. The RTC is disabled.

The switch settings for mode 3 select the RTC (or LTC) address as 777546 and the SLU is disabled.

TABLE 2

VECTOR ADDRESS SELECTION TABLE

SWITCH	IS	TO SELECT VECT BIT
S2-4	ON	3
S2-6	ON	4
S2-3	ON	5
S2-5	ON	6
S2-7	ON	7
S2-8	ON	8

TABLE 3

CHARACTER LENGTH TABLE

LENGTH	S4-4	S4-3
5 BITS	ON	ON
6 BITS	ON	OFF
7 BITS	OFF	ON
8 BITS	OFF	OFF

TABLE 4

SPEED SELECTION TABLE

BAUD	RECEIVER			TRANSMITTER		
	S3-2	S3-3	S3-5	S4-10	S3-1	S3-4
110	OFF	OFF	OFF	ON	ON	ON
150	ON	OFF	OFF	OFF	ON	ON
300	OFF	ON	ON	ON	OFF	OFF
600	OFF	ON	OFF	ON	OFF	ON
1200	OFF	OFF	ON	ON	ON	OFF
2400	ON	ON	ON	OFF	OFF	OFF
4800	ON	ON	OFF	OFF	OFF	ON
9600	ON	OFF	ON	OFF	ON	OFF

TABLE 5

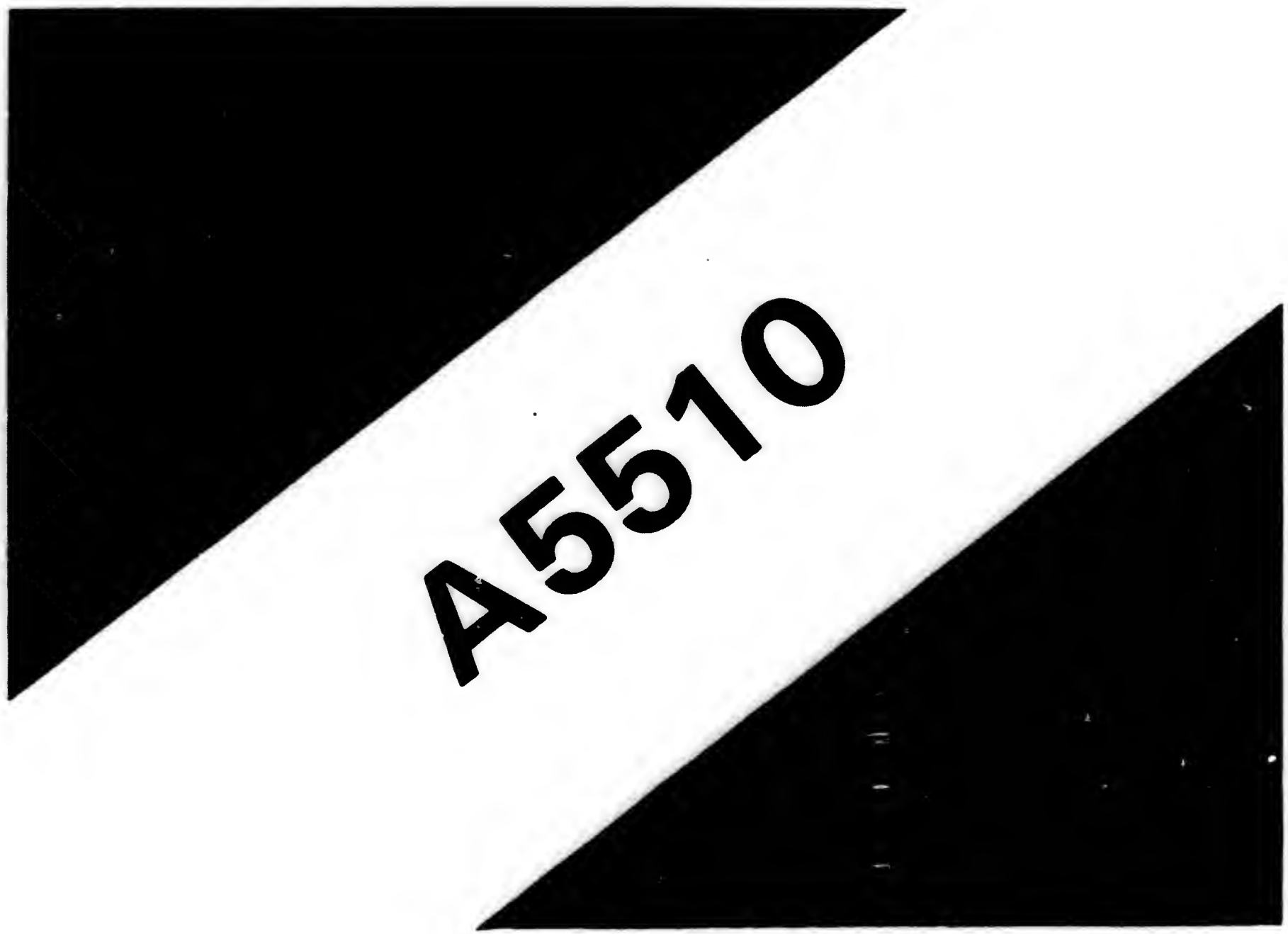
20 MA. ACTIVE/PASSIVE SELECTION TABLE

TRANSMIT	S1-1	S1-2	S1-3	S1-6	S1-7
ACTIVE	ON	ON	OFF	OFF	ON
PASSIVE	OFF	OFF	ON	ON	OFF

RECEIVE	S3-6	S3-7	S3-8	S3-9	S3-10
ACTIVE	ON	OFF	ON	OFF	ON
PASSIVE	OFF	ON	OFF	ON	OFF

PT RDR ENA	S1-4	S1-5	S1-8	S1-9	S1-10
ACTIVE	ON	OFF	ON	OFF	ON
PASSIVE	OFF	ON	OFF	ON	OFF

NOTE - Normal operation is to select active transmit, active receive, and active paper tape reader enable.


A55110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KW11-L - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5510					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sobieniewski	Tom	A	SP	MAA5510-0-0	A

KW11-L

Line Frequency Clock Test

ABSTRACT

This program tests the KW11L line frequency clock. It validates proper operation under both interrupt and non-interrupt modes. It requires the operator to monitor its operation with a clock capable of measuring time in seconds.

REQUIREMENTS

PDP-11 with KW11L

STORAGE 0 - 2000

[redacted] lute Loader

EXECUTION TIME 1 minute

STARTING PROCEDURE 200 = 60 HZ, Line Frequency
202 = 50 HZ, Line Frequency
Load appropriate address to switch register and depress start switch

PRINTOUTS Yes

SWITCH REGISTER OPTIONS No

REFERENCE DOCUMENTS

Printset KW11-L Drawing Directory
Manual DEC-11-HKWB-D
MainDEC-11-DZKWA-A-D
MainDEC-11-DZKWA-A-PB

The device address is 777546 and vector address is 100. It's on bus request level 6. It is also rated at one (1) bus load.

To be mounted in an 11/35 or 11/40

The module location is slot F-3. Remove wrie F3R2 to F3V2.

To be mounted in an 11/45 or 11/50

The module location is slot C1. Remove write C1R2 to C1V2.

End of pass

This test rings the teletype bell at the completion of several different time intervals over a period of one minute. From the time this test beigns, the bell will ring at the end of 1,2,3,4,5,10,20,30,40,50, and 60 seconds, it will then repeat this sequence as long as desired. For verification of this option the test should 15 minutes.

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KW11P - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5520					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Jeknewski		A	SP	MAA5520-0-0	A

KW11P

ABSTRACT

This program tests the KW11-P Real Time Clock. It contains a series of incremented routines that test the control and status register, count set buffer, counter, and interrupt vector address using 100KHZ, 10KHZ, and 60 or 50HZ using the external input with a temporary jumper on the backplane to the LTCL pin (50 or 60HZ). There is also a provision for running two KW11P's simultaneously (one a "COW" or Known Good) and comparing the two.

REQUIREMENTS

PDP-11
KW11-P

STORAGE

This program occupies memory from 0 to 4664.

LOADING

Absolute Loader

EXECUTION TIME

Basic test requires 15 sec. per pass.

STARTING PROCEDURE

200 Basic Test
204 Restart Address Primarily Used by XOR Tester
210 Timing Test
214 Double or Single Real Time Clock Test 100KHZ
220 Double or Single Real Time Clock Test 10KHZ
224 Double or Single Real Time Clock Test 60HZ
230 Double or Single Real Time Clock Test 50HZ

PRINT OUTS

With switches 12 thru 15 equal to "0" (Down) the program will print on errors and continue in test. Bell will ring at completion of a pass.

SWITCH REGISTER OPTIONS

SW15 = 1 or UP ... Halt on Error
SW14 = 1 or UP ... Scope Loop
SW13 = 1 or UP ... Inhibit Printout
SW02 = 1 or UP ... Clock 2 (cow) Present - execute repeatability tests (T25 + T26)
SW00 = 1 or UP ... Suppress Tests using external frequency

DOUBLE REAL TIME CLOCK TESTING

Using the same diagnostic as before, double real time clock testing may be accomplished. One clock is the one under test and the other is a "Known Good" or COW board.

To convert a standard P clock to a "COW" Module:

1. Remove jumper A4
   CSR = 772560
   CSB = 772562
   CTR = 772564

2. Add jumper V8
   Vector Location is 504
   PSW Location is 506

NOTE: This vector is in floating vector space, caution is advised with respect to allowing vector conflicts with other devices on the system.

PROCEDURE FOR DUAL CLOCK REAL TIME CLOCK TEST

1. Load address 214, depress start (100KHZ Test).

2. Enter the time via the TTY keyboard.

3. Set the switches in the switch register to 000005. The TTY will print the time at 5 second intervals.

4. Consecutive printout will be written 5.00 plus or minus .01 seconds of each other. Allow the test to run for at least 10 printouts. If the tolerance is exceeded, the clock under test is defective.

5. Load address 220, depress start (10KHZ Test).

6. Repeat steps 2-4.

7. Load address 224, if 60HZ; or 230 if 50HZ; depress start (line frequency test).

8. Repeat steps 2 and 3.

9. Consecutive printouts will be within 5.00 plus or minus .04 seconds of each other. Typically, and 5.00 plus or minus .2 seconds worst case due to possible AC line frequency variations allow the test to run for at least 10 printouts. If the tolerance is exceeded the clock "Under Test" is defective.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KW11W ACCEPTANCE PROCEDURE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-5530					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekeniewski	Tom	A	SP	MAA5530-0-0	A

KW11W ACCEPTANCE PROCEDURE

I. TEST EQUIPMENT REQUIRED

1. PDP-11 Computer
2. 453 Tektronix Scope or Equivalent
3. KW11-W Option & Print Set
4. M7823 (Watchdog timer)
5. M105 (Address selector)
6. M7821 (vector address selector)
7. TTY

II. MAINDECS REQUIRED

1. DZKWC-C-PB/D

III. EQUIPMENT SET-UP

1. To exercise the KW11-W option, all jumpers mu . be installed on M7823. The test connector 7009463 must be used on KW11-W logic test.

IV. OPERATOR ACTION

1. Load MAINDEC-11-DZKWG-C into PDP11 using absolute loader. Refer to program write-up, MAINDEC-11 DZKWC-C-D.

2. Load and start 200. The TTY will respond as follows:
   First device address:
   The operator responds by inputting 6 characters plus a carriage return on the keyboard.
   Example: First device address 772400 CR

   2.1 The TTY responds as follows:
   First Int. Vector =
   The operator must respond by inputting 3 characters plus a carriage return on the keyboard.
   Example: First int. Vector = 350 CR

   2.2 The TTY will respond as follows:
   Priority int. Level =
   The operator responds by inputting 1 character & CR (using Floating Vector, refer to system configuration, should be between DQ11 & DU11.)
   Example: Priority int. Level = 7 CR

IV. OPERATOR ACTION (Continued)

3. Running the Logic Test:
The TTY will respond with the following:
Logic Test (1), Delay Test (2)*, Dynamic (3)
The operator responds by inputting on the keyboard "1" with a carriage return for Logic test,
The TTY will respond:
1
Logic Test
This test, upon completion, will type out "pass" this test should run for a minimum of 5 minutes.

* Delay test (2) is part of adjustment procedure.

Note: To run the Logic test, the supplied test plug must be connected to the module connector. The T 3 delay must exceed T 2 by 50 microseconds. The adjustment of T 1 must be set to a minimum. For details on other adjustments see KW11-W adjustment procedure - A-SP-KW11-W-3.

4. Running the Dynamic Test
Put bit 00 in the switch register to get back into the monitor or halt machine and load and start 240. If the operator has gone back into the monitor, a keyboard input must be used. Type in "3", carriage return (CR). Dynamic test begins.

On every 100 completions of Dynamic Test, the TTY will type "pass". This test should run for a minimum of 15 minutes.

Acceptable Errors

1. None

5. Procedure for Restart After Error or Fix
1. If an incorrect character is typed while inputting on the TTY, the operator may type a run out and repeat the entire line.

2. Starting address 1000 - direct start or restart of Logic test.

3. Starting address 220 - direct start or restart of delay adjustment test.


A5540

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 17 Dec. 81

TITLE MAST BACKUP PROCEDURE FOR KW11-K DUAL PROGRAMMABLE CLOCK

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Original Release					
B	Complete Re-write.	ML016	A. Richar	12/17/81	Bob Beck.	3/11/82

ENG	APPD	SIZE	CODE	NUMBER	REV
Arthur Richard	Bob Beck	A	SP	MA-A5540-0-0	B

TABLE OF CONTENTS

KW11-K (M7025) DUAL PROGRAMMABLE CLOCK

1.0 SCOPE:

1.1 The KW11-K is a dual programmable real-time clock option used in PDP-11 Unibus computers. The option has Clock A and Clock B and is described as follows:

1.1.1 Clock A is a 16-bit programmable real-time clock, which can accurately measure and count intervals of time and events. It can be used for processor synchronization to external events; generate events, such as an A/D conversion at programmed intervals; and generate events synchronized to an external event input.

1.1.2 Clock B is a 8-bit programmable real-time clock which can accurately time intervals or events. It can be used for generating interrupts at programmed intervals, for generating events (such as an A/D conversion) at programed intervals, or to provide an input frequency to Clock A.

1.2 This procedure establishes the minimum test and electrical standards that a KW11-K must meet to be considered acceptable for customer shipment.

2.0 RESPONSIBILITY:

2.1 It is the responsibility of the originator to maintain this document. Changes should be requested through the originator if possible, or his/her group (if originator is no longer available), or through MAST Administration in Salem (NI).

TITLE MAST BACKUP PROCEDURE FOR KW11-K DUAL PROGAMMABLE CLOCK

3.0 REFERENCE DOCUMENTATION:

3.1 Manuals & Engineering Specifications:

3.1.1	KW11-K System Checkout and Acceptance Specification	SP-KW11-K-2
3.1.2	KW11-K User's Manual	EK-DRV1J-UG
3.1.3	M7025 Circuit Description	SP-KW11-K-5

3.2 Prints and Schematics:

3.2.1	KW11-K Field Maintenance Print Set	MP00048

4.0 REQUIRED TEST EQUIPMENT:

4.1 Hardware & Media:

4.1.1 Unibus CPU with a console device (LA36 or equivalent).

4.1.2 At least 16K words of memory.

4.1.3 Digital voltmeter accurate to .01V @ 15V.

5.0 REQUIRED DIAGNOSTIC PROCRAMS:

5.1 DZKWK KW11-K Diagnostic

6.0 SPECIAL INSTRUCTIONS:

6.1 If a AD11-K option is in the system, it's DEC/X11 module is to exercise the KW11-K during the normal run of DEC/X11. However, the KW11-K's DEC/X11 module must be included when building the DEC/X11 and is run for 15 minutes prior to the normal run of DEC/X11. Be aware that running two DEC/X11 exerciser modules for the same device at the same time will cause errors. Refer to Appendix A of this document for further details.

7.0 INSTALLATION & TEST SET-UP INSTRUCTIONS:

7.1 Module Jumper Configurations:

7.1.1 Refer to Figure 1 and Table A for proper address and vector selection.

7.1.2 The jumpers on the M7025 module should be configured as follows:

W1 = IN - NPR-Remove only if PDP-11/20 or 11/15 without a KH11 option.

W2 = IN - This jumper allows Clock "A" Overflow to generate interrupts in all modes and to set "A Overflow". If LPS11 Compatability is desired, remove it.

W3 = OUT - If in, allows ST1 to accept TTL inputs.

W4 = OUT - If in, allows ST2 to accept TTL inputs.

W5 = OUT - If in, allows ST3 to accept TTL inputs.

TABLE A

Address Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S2 Switch No.				1	2	3	4	5	6	7	8					
Device Address = 770404				Off	On	On	On	Off	On	On	On					

S2 = Switch off for a logical 1.

S2 switches 9 and 10 are unused and is normally left in the off position.

Address 770404 is the base address for Clock A. Address 770432 is the base address for Clock B. Address bits 3 and 4 are hard wired and are not selectable.

TABLE B

Vector Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S1 Switch No.								1	2	3	4	*	5			
Device Vector = 344								Off	On	On	On		Off			

S1 = Switch on for a logical 1.

* = Bit 04 is hard wired and is not selectable. Vector 344 is for Clock A. Vector 364 is for Clock B.

8.0 POWER CHECKS:

8.1 The following voltage must be present and within tolerance on the backplane containing the KW11-K:

VOLTAGE	TOLERANCE	MEASURED AT PIN
+5VDC	+4.75 VDC to +5.25 VDC	AA2

9.0 DIAGNOSTIC TEST PROCEDURE:

For the specific sequence of diagnostics to be run in any particular situation, and for current MAST minimum test criteria (e.g. pass-counts, etc.), refer to the appropriate MAST CHECKLIST. The following is a list of step-by-step instructions for executing each individual diagnostic contained in the CHECKLIST. No errors are allowed.

9.1 Run the KW11-K Diagnostic, DZKWK

9.1.1 The starting location is 200 and the switch register should = 000000.

9.1.2 Only the message "END PASS" will be printed on the console terminal, unless an error occurs.

9.1.3 No errors are allowed.

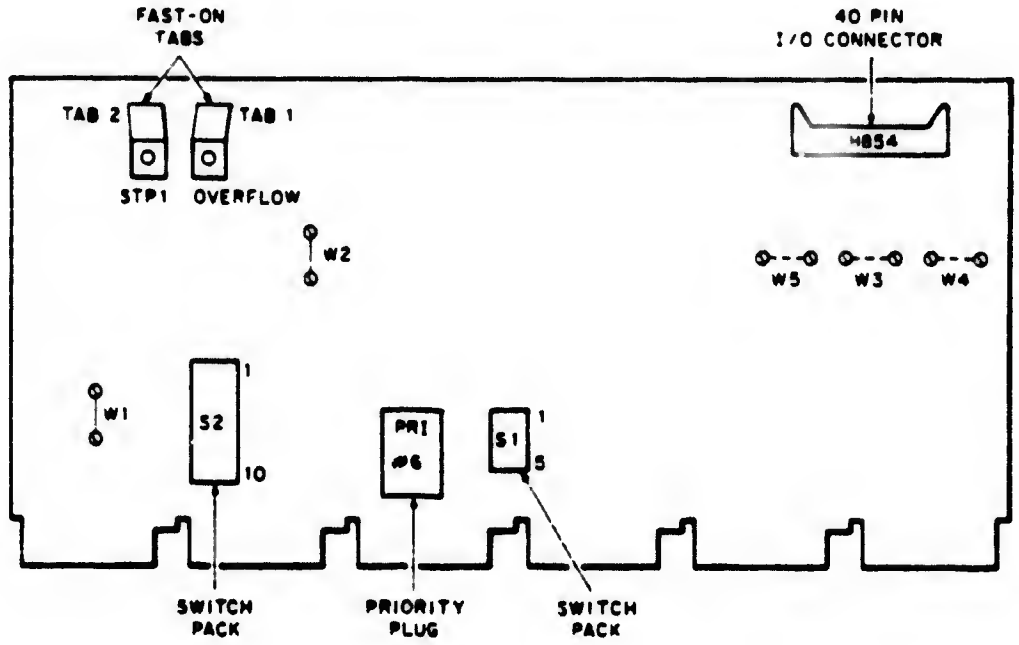

Figure 1 KW11-K M7025 Module

APPENDIX A

This section was provided to give a comprehensive method of DEC/X11 interactive testing the KW11-K and AD11-K. Complete diagnostic testing of both the KW11-K and AD11-K is required prior to DEC/X11 testing.

1.0 The DEC/X11 is built with the modules KWD? and ADB?. (KWD? is for the KW11-K and ADB? is for the AD11-K.)

2.0 Run the DEC/X11 for a minimum of 15 minutes with KWD? and ADB? selected and without error.

3.0 Install a fast-on jumper from tab 2 of the AD11-K to tab 2 of the KW11-K.

4.0 Set the AD11-K's DEC/X11 module ACB? SR0 = 000001 and de-select the KW11-K's DEC/X11 module KWD?. Failure to de-select the KW11-K's DEC/X11 module will cause errors.

5.0 Run the DEC/X11 for the normal run time (minimum 8 hours) without error.

A555

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE KWV11-A REAL TIME CLOCK (11/03) - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	Prev. 7668001-0-5550					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Jeberiewicz	Tom	A	SP	MAA5550-0-0	B

KWV11-A REAL TIME CLOCK (11/Ø3)

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeup for the purpose of expediency. The procedure has been kept brief, and to the point, to keep from confusing the user. For additional information, it will be necessary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD 116)

2.2 A-SP-KWV11-A-2 Engineering Specification

2.3 EK-ADV11-OP-ØØ1 ADV11-A, KWV11-A, AAV11-A, DRV11 Users Manual

2.4 11LO3 Manufacturing Specifications

2.5 Microcomputer Handbook EB-07948

3.0 REQUIRED TEST EQUIPMENT

3.1 LSI11 Standard Computer

3.2 KWV11-A Module

3.3 Output terminal/DLV11

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC-11 - DVKWA KWV11-A Diagnostic and Writeup

4.2 MAINDEC-11 - DXKWF DEC/X11 Exerciser and Writeup

5.0 SPECIAL INSTRUCTIONS AND CHECKS

5.1 If the system contains an H322 signal distribution panel, connect the KWV11-A by means of a BCØ8R cable, J1 of module to J5 of the H322. (all 11LØ3 systems)

5.2 When an ADV11-A and a KWV11-A are both present in the system, module jumpers (DEC 7010771) are installed from the KW output tab (CLK) to the A/D clock overflow tab (C) and from the KW tab (STI) to the AD tab(s).

6.0 TEST SET UP

6.1 Insure switch packs S1 and S3 are set for a device address of 170420 and a vector address of 440 respectively.

6.2 Insure all switches of switch pack S2 are turned off.

6.3 Install module in CPU slots A thru DØ2 of all 11LØ3 systems.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 KWV11-A Test Diagnostic (DVKWA)

7.1.1 Load program through appropriate load media.

7.1.2 Program starting addresses.

	7.1.2.1	200 - Start of logic tests
	7.1.2.2	204 - Restart address for logic tests
*	7.1.2.3	210 - IO signal test #1
*	7.1.2.4	214 - IO signal test #2
*	7.1.2.5	220 - IO signal test #3
	7.1.2.6	230 - Production starting address
	7.1.2.7	240 - Tester starting address

* For Field use only.

7.1.3 Alternate software SR settings (176)

7.1.3.1	SWR15 = 1 Halt on error
7.1.3.2	SWR14 = 1 Loop on test
7.1.3.3	SWR13 = 1 Inhibit error typeout
7.1.3.4	SWR12 = 1 Enable line frequency rate testing
7.1.3.5	SWR11 = 1 Inhibit iterations (short pass)
7.1.3.6	SWR10 = 1 Bell on error
7.1.3.7	SWR 9 = 1 Loop on error
7.1.3.8	SWR 8 = 1 Loop on test in SWR <7:0>

NOTE: The software switch register may be changed at any time by typing Control C. If you wish to keep the current value, type <CR>. If you wish to change the value, type the new value followed by a <CR>.

7.1.4 Operator Action

7.1.4.1 Set all SWR bits as desired (default 000000)

7.1.4.2 Type 200G.

7.1.5 Evidence of End of Pass and Run Time at End of Pass typeout will resemble the following example:

"END PASS 1 - Total errors 0 - Good units 00000000 00000001" First Pass runs without iterations and takes 30 seconds, subsequent passes run with iterations and take 2.5 minutes.

7.1.6 Acceptable errors: None

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TITLE AA11 DIGITAL/ANALOG CONVERTER - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6110					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelenievski	Tom	A	SP	MAA6110-0-0	A

AA11 DIGITAL/ANALOG CONVERTER

1.0 AA11 SET-UP AND CALIBRATION

Refer to document A-SP-AA11-D-7

1.1 Diagnostic Package

(A) Calibration Test MainDEC-11-D6BA

(B) Scope Options Test MainDEC-11-D6CA

1.2 Other Related Documents

(A) AA11-D D/A Sub-System Manual DEC-11-HAAC-D

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AAV11-A 4 CHANNEL 12 BIT D/A FOR PDP-11/03 - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6115					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jekanowski		A	SP	MAA6115-0-0	A

AAV11-A 4 CHANNEL 12 BIT D/A FOR PDP-11/03

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeup. For the purpose of expediency, the procedure has been kept brief and to the point, to keep from confusing the user. For additional information, it will be necessary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD 116)

2.2 Engineering Specification A-SP-AAV11-A-3

2.3 User's Manual EK-ADV11-OP-001

2.4 AAV1 rint Set

3.0 REQUIRED T..T EQUIPMENT

3.1 LSI-11 Standard Computer

3.2 Oscilloscope 453 or equivalent

3.3 DVM - 5 digits or accurate null meter

3.4 AAV11-A module

3.5 Output terminal/DLV11

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC 11 - DVAAA AAV11-A Test Diagnostic and Write up

4.2 MAINDEC 11 - DXAAC DEC/X11 Exerciser and Write up

5.0 SPECIAL INSTRUCTIONS AND CHECKS

5.1 RF Shield provided with AAV11-A must be installed over Side 1 (component) of module.

5.2 If an H322 Distribution Panel is present, then connect AAV11-A by means of a BC08-06 cable from J1 of module to J10 of the H322 (all H and J variations of 11L03)

6.0 TEST SET UP

6.1 Insure switch pack S1 set up for a device address of 17Ø44Ø. No vector is set up since the AAV11-A is not capable of interrupting.

6.2 Install module in Expander Box (BA11-M) slot A thru DØ3 of all H and J variations of 11LØ3's.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 AAV11-A Test (DVAAA)

7.1.1 Load program through appropriate load media.

7.1.2 Available tests and their starting addresses:

ST. ADD	TEST
200	Manual Logic Test
204	Manual Ramp Test
210	Manual Static Calibration
214	Manual Dynamic Calibration

7.1.3 Alternate Software SR settings (loc 176)

7.1.3.1 SWR15 = 1 Halt on error
7.1.3.2 SWR14 = 1 Loop on test
7.1.3.3 SWR13 = 1 Inhibit error typeouts
7.1.3.4 SWR11 = 1 Inhibit iterations
7.1.3.5 SWR10 = 1 Bell on error
7.1.3.6 SWR 9 = 1 Loop on error
7.1.3.7 SWR 8 = 1 Loop on test in SWR<7:0>

7.1.4 Operator Action

7.1.4.1 Set SWR bits as desired
7.1.4.2 Type 200G (for logic test)

NOTE: For detailed information on manual ramp test, manual static calibration test, and manual dynamic calibration test, refer to engineering specifications SP-AAV11A-3

7.1.5 Evidence of End of Pass and Run Time

"END PASS #XXXXX" is typed in 5 seconds with no iterations and in 20 seconds with iterations.

7.1.6 Acceptable Errors: None

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TITLE ADO1-D A/D CONVERTER - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6120					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM JELENIEWSKI		A	SP	MAA6120-0-0	A

AD01-D A/D CONVERTER

1.0 AD01-D SET-UP AND CALIBRATION

Refer to document DEC-11-HADDA-C-D

1.1 AD01-D Acceptance Procedure

Refer to document A-SP-AD01-D-12

1.2 Diagnostic Package

(A) AD01-D Logic and Calibration Test
MainDEC-11-D6AB

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE LPA11-K LABORATORY PERIPHERAL ACCELERATOR - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6124					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelonianki	Tom Kelly	A	SP	MAA6124-0-0	A

LPA11-K LABORATORY PERIPHERAL ACCELERATOR

INTRODUCTION

This LPA11-K procedure establishes minimum checkout specifications for FA&T, along with configuration requirements.

1.0 TEST EQUIPMENT

1.1 Oscilloscope (100 MHz bandwidth min.)

1.2 Quad Extender Module (W984)

1.3 Hex Multilayer Extender Module (W9048)

1.4 Tektronix Model 7D01 Logic Analyzer with DFI Display Formatter (or equivalent) is recommended but not required.

2.0 TEST SOFTWARE

2.1 MP00479 LPA11-K Field Maintenance Print Set

2.2 MP00161 AA11-K Field Maintenance Print Set

2.3 MP00047 AD11-K Field Maintenance Print Set

2.4 MP00090 AM11-K Field Maintenance Print Set

2.5 B-DD-DR11-K DR11-K Customer Print Set

2.6 MP00048 KW11-K Field Maintenance Print Set

2.7 B-DD-AR11-0 AR11 Customer Print Set

2.8 B-DD-LPS11-S LPS11 Customer Print Set

2.9 EK-LPA11-SM-001 LPA11-K Installation and Maintenance Manual

2.10 EK-KMC11-OP-001 KMC11-A Maintenance Manual

2.11 ZJ252-RB LPA11-K Diagnostic Package

2.12 ZJ234-RB KMC11-A Diagnostic Package

2.13 MAINDEC-11-DXLPF DEC-X-11 Multiuser Mode Micro Code Loader

2.14 MAINDEC-11-DXLPG DEC-X-11 Dedicated Mode Micro Code Loader

2.15 MAINDEC-11-DXLPH DEC-X-11 LPA11-K Exerciser

2.16 A-SP-LPS11-14 LPS11 Acceptance Procedure

3.0 CHECKOUT OF AN LPA11-K WITH "K" OPTIONS

There are many possible configurations for the LPA11-K. Therefore, configuration of the system cannot be specifically given for all cases. The LPA11-K must be configured according to the guidelines given in the LPA11-K Installation and Maintenance Manual. Checkout of the LPA11-K can proceed as soon as configuration has been completed. Checkout of an LPA11-K with "K" options is as follows:

3.1 Make sure all device addresses, vector addresses and priority levels of the Basic LPA11-K and any additional options on the LPA11-K's I/O Bus are set according to Appendix A of this document.

3.2 Make sure that Switch 7 of E76 on the M8200-YC is set to the "OFF" position.

3.3 Make sure that Jumper W1 is installed on the M8254.

3.4 Make sure that the I/O Bus has at least an AD11-K and a KW11-K on it.

3.5 Load MAINDEC-11-DRLPA (LPA11-K System Test). Follow operating instructions contained in the write up for this diagnostic. Do not patch locations "SR1:" and "SR2:". Allow the program to run in its default condition (1 AD11-K and 1 KW11-K). This will be a quick check to see that the Basic LPA11-K is functioning properly. Allow at least four (4) non-erroring passes. If there is an error, refer to the trouble-shooting flowchart in Appendix B.

3.6 The following checkout instructions will assume a maximum LPA11 System (5 DR11-K's, 1 KW11-K, 2 AD11-K's, and 1 AA11-K). Omit the sections pertaining to any options that are not included in the configuration that is being tested.

3.7 Load MAINDEC-11-DRLPF (LPA/DR11-K Digital I/O Test). Follow operating instructions contained in the writeup for this diagnostic. All DR11-K's on the LPA11-K's I/O Bus will be checked by this diagnostic. If an error occurs, fix or replace the failing DR11-K. The diagnostic must be allowed to make at least four (4) non-erroring passes.

3.8 Load MAINDEC-11-DRLPG (LPA11/KW11-K Diagnostic). Follow operating instructions contained in the writeup for this diagnostic. Interrupt logic is not checked by this diagnostic. If an error occurs, fix or replace the failing KW11-K. The diagnostic must be allowed to make at least four (4) non-erroring passes.

3.9 Load MAINDEC-11DRLPK (LPA11/AD11-K Diagnostic). Follow operating instructions contained in the writeup for this diagnostic. Check and calibrate the AD11-K (s) according to A-SP-AD11-K-5 which is included in the AD11-K Field Maintenance Print Set. Use of this diagnostic appears to the user the same as if the DZADL diagnostic was being run on an AD11-K on the Unibus. Interrupt logic on the AD11-K is not checked by MD-11-DRLPK.

NOTE: Allow a 15 minute warmup f[illegible] the AD11-K(s) before calibration. Allow the diagnostic to make at least two (2) non-erroring passes of "Auto Test" after calibration is completed. Make sure the G5036 wraparound module is in place and that the switch is in the "0" position.

If an AM11-K (Multiple Gain Multiplexer) is to be installed on the system, do so at this time. Refer to A-SP-AM11-K-5 (AM11-K Manufacturing and Field Acceptance Procedure) for installation and checkout. Use MAINDEC-11-DRLPB instead of MAINDEC-11-DZADL. Omit reference to MD-11-DXKBA (DEC/X11 Module).

3.10 Load MAINDEC-11-DRLPB (LPA11/AA11-K diagnostic). Follow operating instructions contained in the writeup for this diagnostic. Checkout and calibrate the AA11-K according to A-SP-AA11-K-5 (AA11-K Manufacturing and Field Acceptance Procedure). MD-11-DRLPB will appear to the user the same as if MD-11-DZAAC were being run on an AA11-K on the Unibus. However, the interrupt logic on the AA11-K will not be checked and the settling test square wave will not be generated. Omit references to running MD-11-DXAAB (DEC/X11 Module).

3.11 Load MAINDEC-11-DRLPA. Follow operating instructions contained in the writeup for this diagnostic. The address of locations "SR1:" and "SR2:" may be found in the symbol table at the back of the listing. Load location "SR1:" with the appropriate bits to inform the diagnostic as to which options are on the LPA11-K's I/O Bus. Load location "SR2:" with the appropriate bits to inform the diagnostic as to how the options are set up for test. The FA&T area will have G5036 wraparound modules on all AD11-K's present. Set the switches on the G5036's to the "0" position. G5036 wraparound modules are optional in the field. All DR11-K's will have the one foot BC08R wraparound cable installed; if an AA11-K is present, it will have one of the display scopes connected (as described in A-SP-AA11-K-5).

Allow MAINDEC-11-DRLPA to make a minimum of six (6) non-erroring passes. If an error does occur, refer to the troubleshooting charts in Appendix B.

4.0 CHECKOUT OF AN LPA11-K WITH AN AR11

4.1 Configure the LPA11-K with an AR11 analog realtime subsystem that has previously been checked out and accepted according to the AR11 System Installation and Checkout Procedure (A-SP-AR11-O-4). Follow configuration guidelines given in the LPA11-K Installation and Maintenance Manual (EK-LPA11-SM-001).

4.2 Set the Device Address of the AR11 to 770400. Set the Vector Address to 340.

4.3 Set the Device Address, Vector Address and Priority Level of the Basic LPA11-K according to Appendix A of this document.

4.4 Make sure that Switch 7 of E76 on the M8200-YC is set to the "OFF" position.

4.5 Make sure that Jumper W1 is installed on the M8254.

4.6 Make sure a G5036 wraparound module is connected to the AR11 in the FA&T area. Set the switch to the "0" position. The G5036 wraparound module is optional in the field.

4.7 Load MAINDEC-11-DRLPA (LPA11-K System Test). Follow operating instructions contained in the writeup for this diagnostic. Patch location "SR1:" to 002000. Patch location "SR2:" to 002000 if the G5036 is present. Allow the diagnostic to make at least six (6) non-erroring passes. If an error does occur, refer to the troubleshooting flowcharts in Appendix B.

5.0 CHECKOUT OF AN LPA11-K WITH AN LPS11

5.1 Configure the LPA11-K with an LPS11 Laboratory Peripheral System that has previously been checked out and accepted according to the LPS11 Acceptance Procedure (A-SP-LPS11-S-14). Follow configuration guidelines given in the LPA11-K Installation and Maintenance Manual (EK-LPA11-SM-001).

5.2 Set the Base Device Address of the LPS11 to 770400. Set the Vector Address to 340.

5.3 Set the Device Address, Vector Address, and Priority Level of the Basic LPA11-K according to Appendix A of this document.

5.4 Make sure that Switch 7 of E76 on the M8200-YC is set to the "OFF" position.

5.5 Make sure that Jumper W1 is installed on the M8254.

5.6 Make sure that all A/D Channel inputs are shorted to ground.

5.7 If the LPS11 has the LPSDRA Option, it must have the Digital I/O Test Cable (7009192) connected. This is optional in the field, but mandatory in the FA&T area.

5.8 If the LPS11 has the LPSVC Option, a scope must be connected to the scope control output on the rear of the LPS11 chassis. Refer to paragraph 14.0 of A-SP-LPS11-S-14 (LPS11 Acceptance Procedure) for selection of the proper scope and its installation. This is optional in the field, but mandatory in the FA&T area.

5.9 Load MAINDEC-11-DRLPA (LPA11-K System Test). Follow operating instructions contained in the writeup for this diagnostic. The address of locations "SR1:" and "SR2:" may be found in the Symbol Table at the back of the listing. Load location "SR1:" with the appropriate bits to inform the diagnostic that there is a LPS11 on the LPA11-K's I/O Bus, and to inform it as to which options are in the LPS11. Load location "SR2:" with the appropriate bits to inform the diagnostic as to how the LPS11 options are set up for test.

Allow MAINDEC-11-DRLPA to make at least six (6) non-erroring passes. If an error does occur, refer to the troubleshooting charts in Appendix B.

6.0 LPA11-K OPTION ACCEPTANCE

6.1 Perform the option test given in Section 3.0 of this document if the LPA11-K has "K" options on the I/O Bus.

6.2 Perform the option test given in Section 4.0 of this document if the LPA11-K has an AR11 on the I/O Bus.

6.3 Perform the option test given in Section 5.0 of this document if the LPA11-K has an LPS11 on the I/O Bus.

6.4 Configure DEC/X11 for the system that the LPA11-K is on. DEC/X11 for the LPA11-K must include MAINDEC-11-DXLPF, MAINDEC-11-DXLPG and MAINDEC-11-DXLPH. When running DECX/11 in the FA&T area, run MD-11-DXLPG and MD-11-DXLPH. They must be selected in that order. Do not select MD-11-DXLPF and MD-11-DXLPH if a problem seemed to exist with the system when the customer was using multiuser mode. MD-11-DXLPF and MD-11-DXLPG are both loaders that are used to load the microcode that is run by the MD-11-DXLPH exerciser. MD-11-DXLPF is the microcode loader for the multiuser mode. MD-11-DXLPG is the microcode loader for the dedicated mode. If all three LPA11-K DEC/X11 modules were selected, whichever of the two loaders was the last one selected, would be the one whose microcode would be exercised by MD-11-DXLPH.

6.4 cont

Patch locations "SR1:" and "SR2:" of MAINDEC-11-DRLPH according to the instructions contained in the writeup for this DEC/X11 module. Run DEC/X11 for a minimum of four (4) hours.

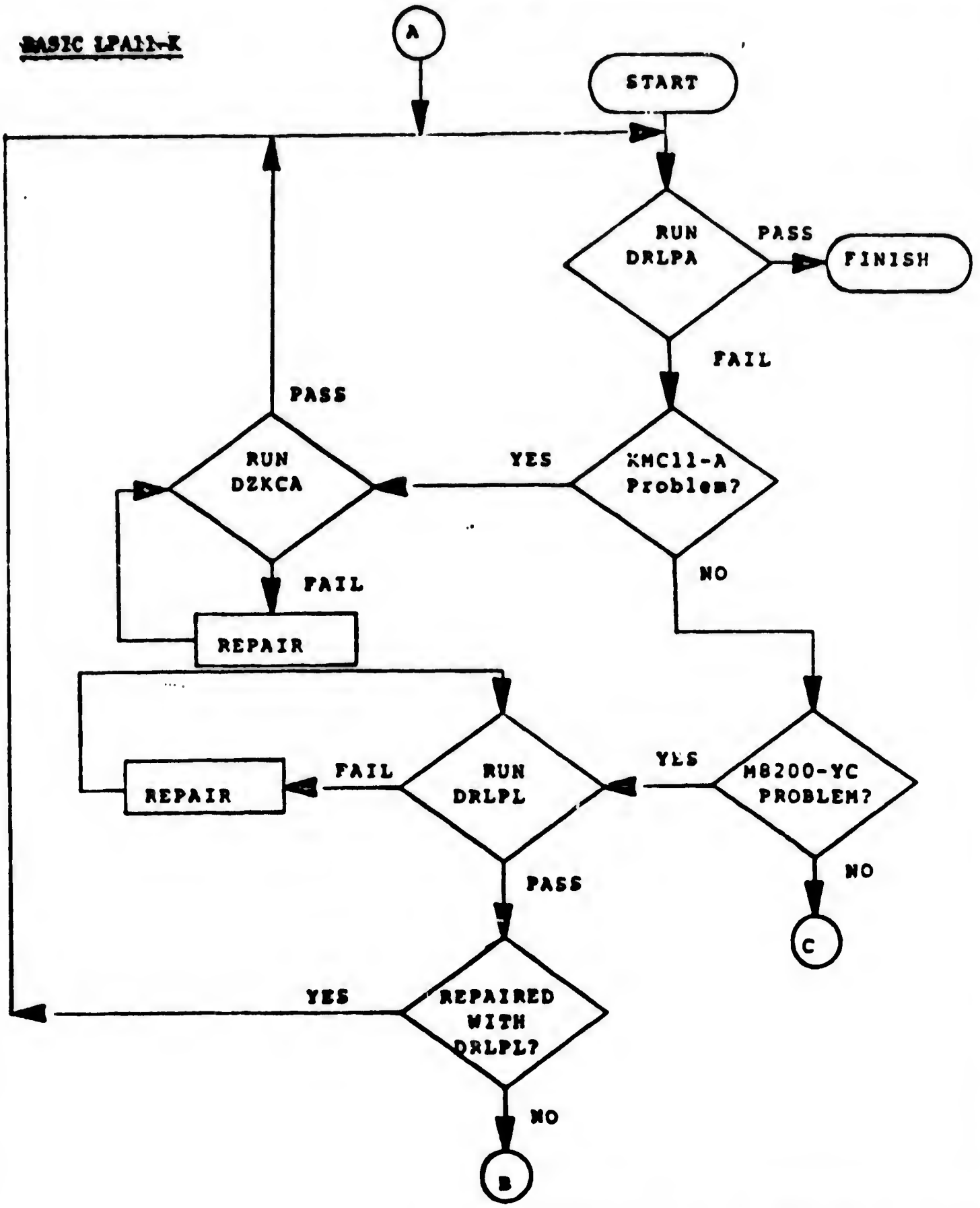
APPENDIX A

DEVICE	DEVICE ADDRESS	VECTOR ADDRESS	PRIORITY LEVEL
KMC11-A	770460	*300	5
M8200-YC	770470	420	5
AA11-K	770416	360	4
AD11-K #1	770400	340	6
AD11-K #2	770440	400	6
AR11	770400	340	Fixed
DR11-K #1	767770	310	4
DR11-K #2	767760	320	4
DR11-K #3	767750	330	4
DR11-K #4	767740	350	4
DR11-K #5	767730	370	4
KW11-K	770404	344	6
LPS11	770400	340	Fixed

* Preferred Floating Vector Address

APPENDIX B

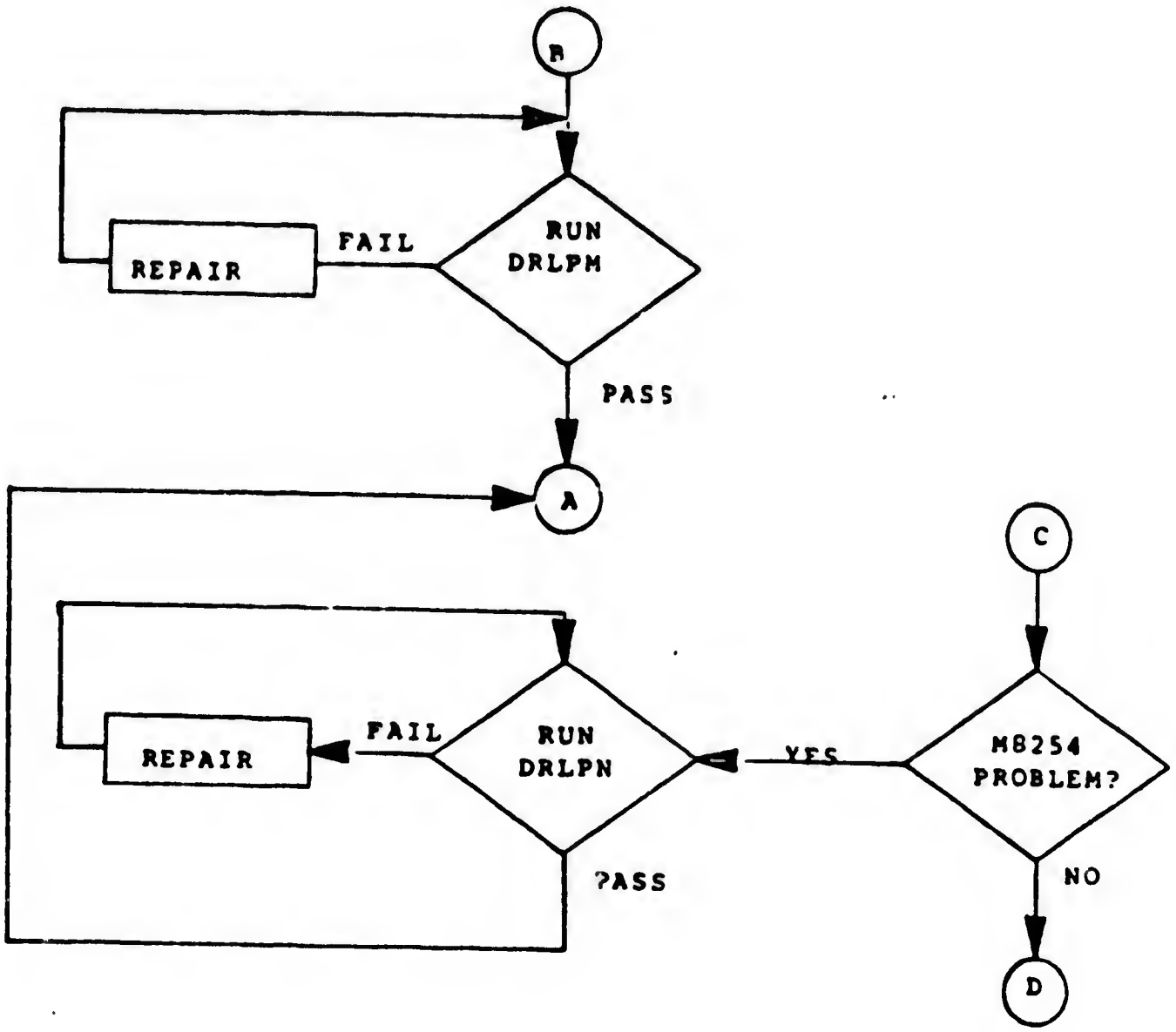
BASIC LPA11-K

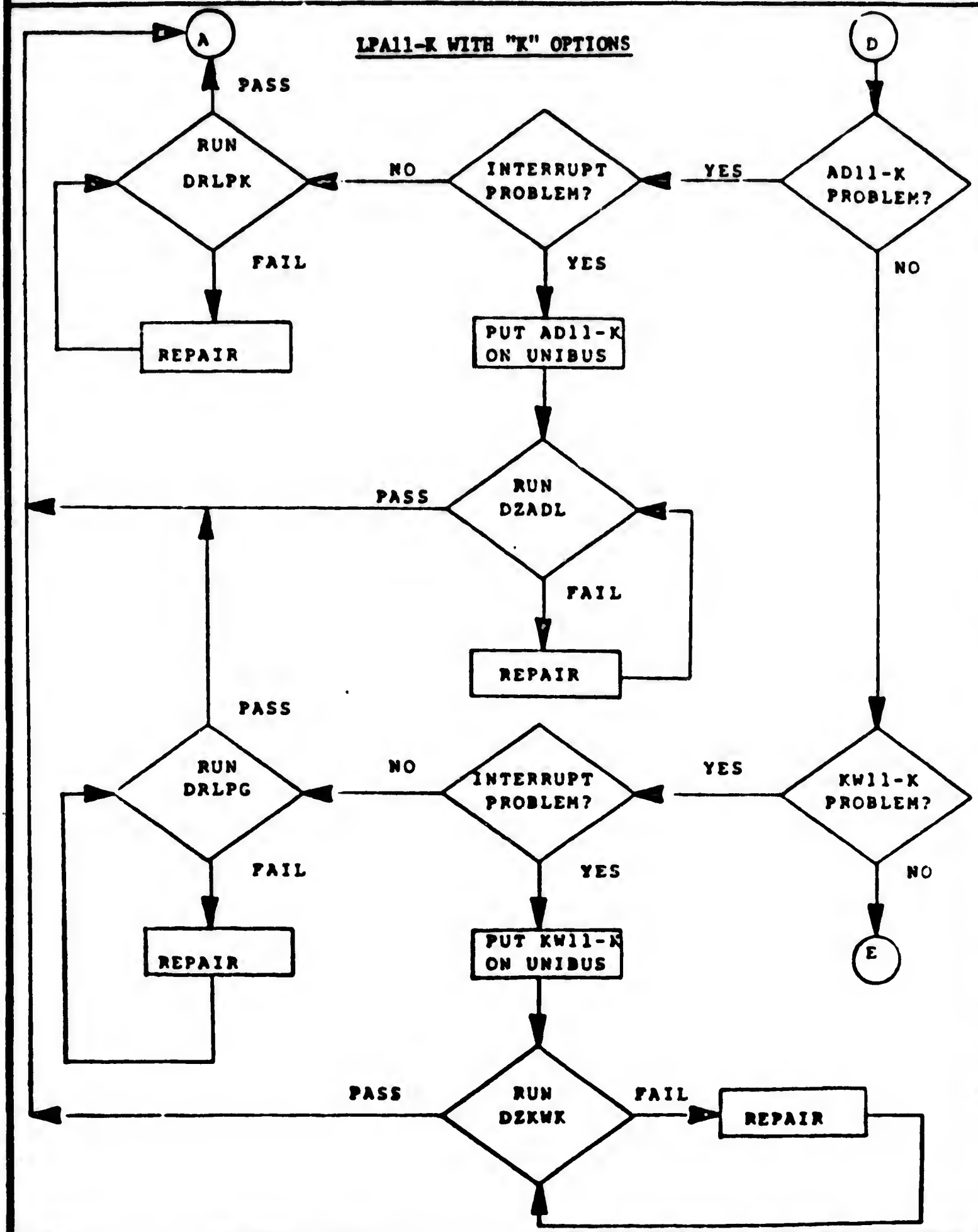


	SIZE	CODE	NUMBER	REV
	A	SP	MAA6124-0-0	A

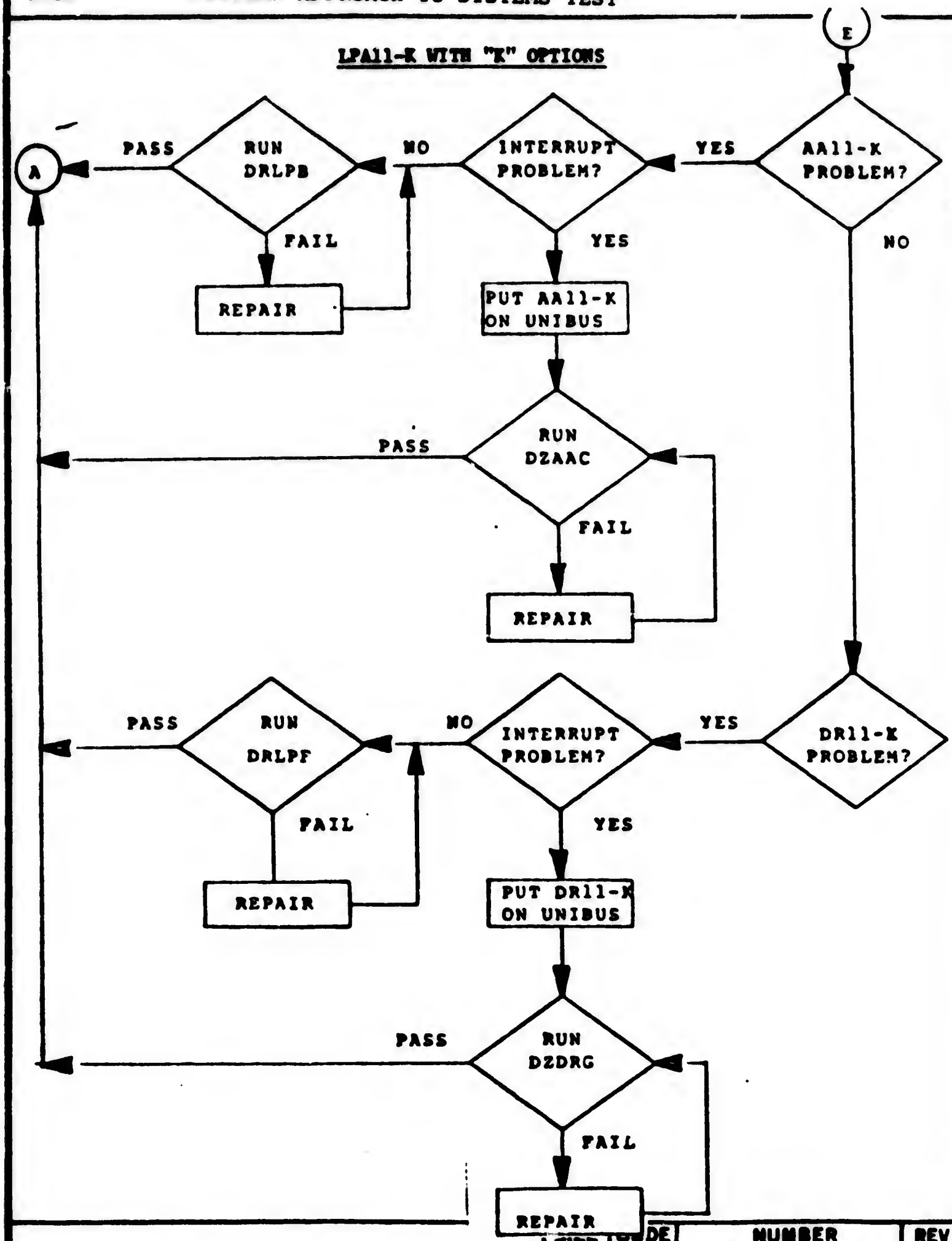
DEC 16-[illegible]-[illegible]

BASIC LPA11-K

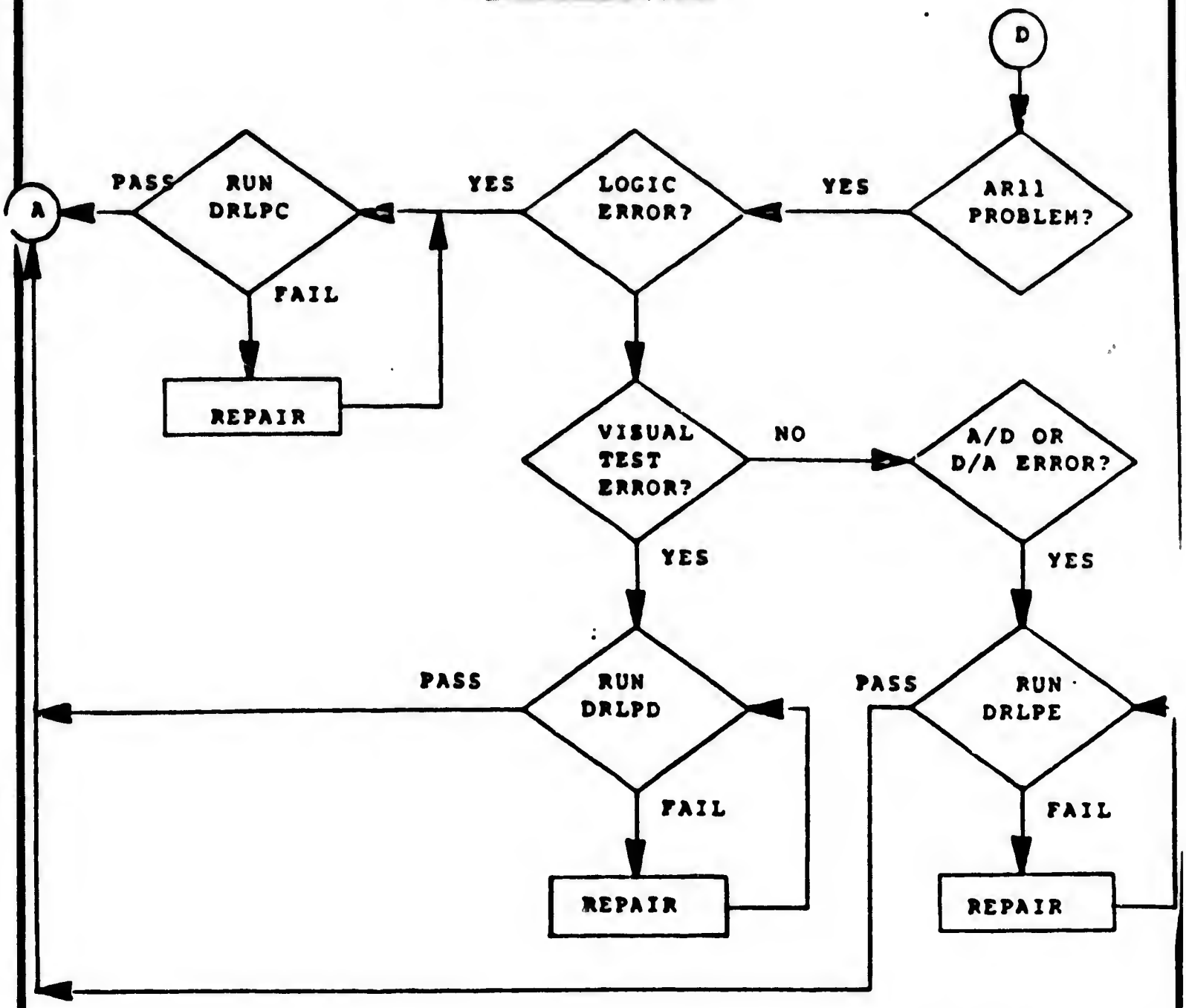



A
LPA11-K WITH "K" OPTIONS
D
PASS
RUN DRLPK
NO
INTERRUPT PROBLEM?
YES
AD11-K PROBLEM?
FAIL
YES
NO
REPAIR
PUT AD11-K ON UNIBUS
PASS
RUN DZADL
FAIL
REPAIR
PASS
RUN DRLPG
NO
INTERRUPT PROBLEM?
YES
KW11-K PROBLEM?
FAIL
YES
NO
REPAIR
PUT KW11-K ON UNIBUS
E
PASS
RUN DZKWK
FAIL
REPAIR

LPA11-K WITH "K" OPTIONS

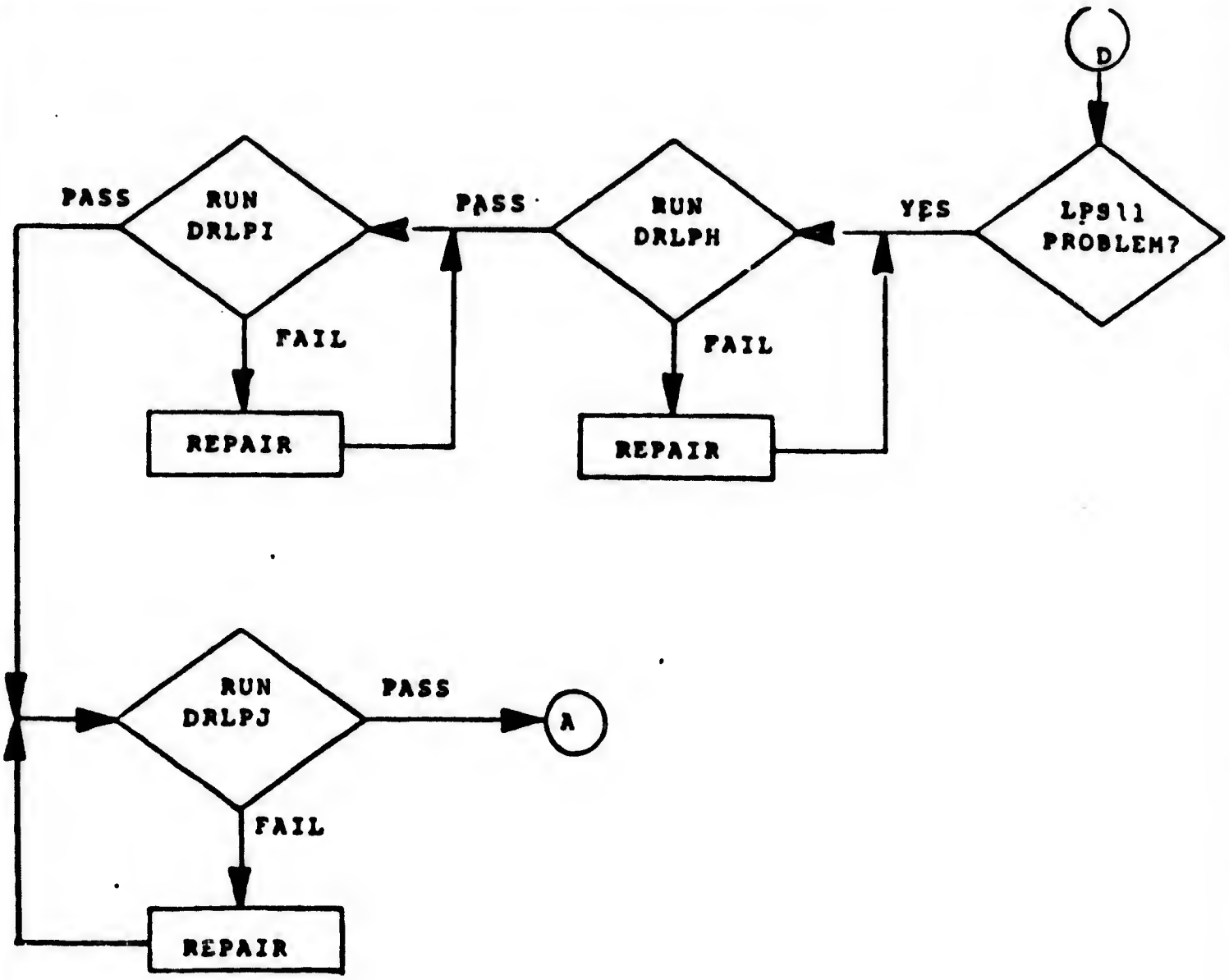


LPA11-K WITH AR11



- NOTE: If DRLPA reports an error and it cannot be found by running DRLPC, DRLPD or DRLPE; then you must connect the Unibus to the LPA11's I/O Bus. Remove the M8254 module and replace it with a G727 grant card. Run MD-11-DZARA, MD-11-DZARB and MD-11-DZARC to solve the problem. Make sure you do not exceed the Unibus Load Spec's.

TITLE MODULAR APPROACH TO SYSTEMS TEST



NOTE: If DRLPA reports an error, and it cannot be found by running MD-11-DRLPH, MD-11-DRLPI or MD-11-DRLPJ; then you must connect the Unibus to the LPA11-K's I/O Bus. Remove the M8254 module and replace it with a G727 grant card. Run MD-11-DZLPC, MD-11-DZLPD or MD-11-DZLPI to solve the problem. Make sure you do not exceed the Unibus Load Specs.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AD11-K BACKUP REFERENCE DOCUMENTATION - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6125					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM SOBKIEWSKI		A	SP	MAA6125-0-0	A

EN-01083-16-N672-(392)

AD11-K BACKUP REFERENCE DOCUMENTATION

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic write-up for the purpose of expediency. All instructions contained in this procedure are brief and direct for reasons of simplification, so not to confuse the operator when performing diagnostic testing. For more in-depth information, it will be necessary to refer to the diagnostic write-up.

2.0 REFERENCE DOCUMENTS

The documents listed below are for reference only.

2.1 Workmanship Manual

2.2 AD11-K User's Manual EK-AD11-K-OP-001

2.3 AD11-K Print Set B-TC-AD11-K-1

2.4 AD11-K Manufacturing and Field System Acceptance Procedure A-SP-AD11-K-5.

3.0 REQUIRED TEST EQUIPMENT

3.1 BG5036 Maintenance Kit (consists of a G5036 wrap-around module and a BC08R-1 cable).

3.2 Calibrated DC voltage source (EDC model MV116 or equivalent). Two are needed if a wrap-around module is not available.

3.3 PDP-11 CPU.

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC-11-DZADL AD11-K Diagnostic and Write-Up.

4.2 MAINDEC-11-DXADB DEC-X11 AD11-K Exerciser and Write-Up.

5.0 SPECIAL INSPECTION AND CHECKS

5.1 Assure the A/D converter package is securely fastened to the AD00 module.

6.0 TEST SET-UP

6.1 Set up address and vector switches per AD11-K Mfg. and Field System Acceptance Procedure A-SP-AD11-K-5 section 2.2 - 2.3.

6.2 Install G5036 wrap-around test card per AD11-K Mfg. and Field System Acceptance Procedure A-SP-AD11-K-5 section 6.1 if wrap-around module is available. If the wrap-around module is not available, refer to AD11-K Mfg. and Field System Acceptance Procedure A-SP-AD11-K-5 section 6.2.

7.0 SYSTEM INTEGRATION TEST PROCEDURE

7.1 Load diagnostic into system under test using low or high speed tape reader, XXDP, or ACT-11.

7.2 Program Start-Up

7.2.1 Load Address 200

7.2.2 Start SR = 000000 (Standard Default Condition)

7.3 Switch Register Settings

7.3.1 SW15 = 1 or Up Halt on Error

7.3.2 SW14 = 1 or Up Loop on Test

7.3.3 SW13 = 1 or Up Inhibit Error Typeouts

7.3.4 SW12 = 1 or Up for VT55 Display

7.3.5 SW11 = 1 or Up Inhibit Iterations

7.3.6 SW10 = 1 or Up Bell on Error

7.3.7 SW9 = 1 or Up Loop on Error

7.3.8 SW8 = 1 or Up Loop on Test in SR <0:7>

7.4 Operator Action

After the diagnostic has been started, this statement is printed out: "Type the letter and carriage return of the desired test." The Auto Test (A) should be selected since it operates all diagnostic portions of the AD11-K test.

The operator should observe 2 non-erroring passes. Running the Auto test on the first pass should take 18 minutes, successive passes should take 36 minutes each.

7.5 Acceptable Errors

There are no acceptable errors.

7.6 Procedure # Restart After Repair

7.6.1 Repeat steps 7.2 thru 7.5.

7.7 DEC-X11 With KW11-K Installed

7.7.1 Refer to AD11-K Mfg. and Field System Acceptance Procedure A-SP-AD11-K-5 Section 7 for interactive testing.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AA11-K DIGITAL TO ANALOG CONVERTER - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6126					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tony Jekanowski		A	SP	MAA6126-0-0	A

AA11-K DIGITAL TO ANALOG CONVERTER

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeup for the purpose of expediency. All instructions in this procedure are brief and direct for reasons of simplification, so not to confuse the operator when performing diagnostic testing. For more in-depth information, it will be necessary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

The documents listed below are for reference only.

2.1 Workmanship Manual

2.2 AA11-K user's Manual EK-AA11K-TM-001

2.3 AA11-K Print Set

2.4 AA11-K Manufacturing and Field System Acceptance Procedure A-SP-AA11-K-5

3.0 REQUIRED TEST EQUIPMENT

3.1 Calibrated DC Volt Meter

3.2 VR14 or VT01 Scope or Equivalent

3.3 Oscilloscope Tektronix 453 or Equivalent

3.4 PDP-11 CPU with 1 Quad SPC Slot

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC-11-DZAAC-A DIAGNOSTIC AND WRITEUP FOR AA11-K

4.2 MAINDEC-11-DXAAB-A AA11-K DEC-X-11 Exerciser and Writeup

5.0 SPECIAL INSPECTIONS AND CHECKS

NONE

6.0 TEST SETUP

6.1 Set up address and vector switches per AA11-K Mfg. and Field System Acceptance Procedure A-SP-AA11-K-5 Sections 3.4 - 3.6.

6.2 Connect scope cable to AA11-K berg connector J1 per AA11-K Mfg. and Field System Acceptance Procedure A-SP-AA11-K-5 Section 4.2.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 Load program through the appropriate load media.

7.2 Program starting address

7.2.1 Load address 200

7.2.2 Start 000000 (SR) standard switch settings

7.3 Alternate switch settings

7.3.1 SW15=1 Halt on Error

7.3.2 SW14=1 Loop on current test

7.3.3 SW13=1 Inhibit error typeout

7.3.4 SW12=1 Storage Scope connected

7.3.5 SW11=1 Inhibit test iterations

7.3.6 SW10=1 External delay connected

7.3.7 SW09=1 Two's compliment mode

7.3.8 SW08=1 Loop on test in SR 7:0

7.4 Operator Action

A message will be typed designating a 2 letter code for sub test selection. The auto logic test "AL" should be selected first to verify proper logic operation. Then "AD" should be typed to run the visual display portion.

NOTE: If scope display is not available, refer to the AA11-K Mfg. and Field Acceptance Procedure, A-SP-AA11-K-5 for alternative testing.

7.5 Evidence of End of Pass, or Estimated Run Time

7.5.1 Subtest "AL" takes approx. 30 sec.

7.5.2 Subtest "AD" takes approx. 60 sec.

7.5.3 Subtest "AL" is operator dependent.

7.5.4 Subtest "ML" is a non-ending loop.

7.5.5 Subtest "MD" is a non-ending loop.

7.6 Acceptable Errors

NONE

7.7 Procedure f Restart After Repair

7.7.1 Repeat steps 7.2 through 7.6.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE AM11-K MULTIPLEXER EXPANDER - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6127					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tony Jekanowski	Tom	A	SP	MAA6127-0-0	A

EN-01003-16-N678-(398)

AM11-K MULTIPLEXER EXPANDER

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic write-up for the purpose of expediency. All instructions contained in this procedure are direct and brief for reasons of simplification, so as not to confuse the operator when performing the diagnostic testing. For more in-depth information, it will be necessary to refer to the diagnostic write-up.

2.0 REFERENCE DOCUMENTATION

The documents listed below are for reference only.

2.1 Workmanship Manual

2.2 AM11-K User's Manual EK-Am11K-TM-001

2.3 AM11-K Print Set

2.4 AM11-K Manufacturing and Field System Acceptance Procedure A-SP-AM11-K-5.

3.0 REQUIRED TEST EQUIPMENT

3.1 Oscilloscope Tektronix 453 or equivalent.

3.2 BG5036 Maintenance Kit (G5036 Wraparound Module and a BC08R-01 Cable)

3.3 Calibrated DC voltage source (EDC Model MV100 or equivalent).

3.4 BC08R-08 cable

3.5 AD11-K Analog Module

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC-11-DZADB-B AD11-K diagnostic used for checkout and debug of the AM11-K.

4.2 MAINDEC-11-DXADB-A AD11-K DEC-X-11 exerciser.

5.0 SPECIAL INSPECTIONS AND CHECKS

NONE

6.0 TEST SETUP

6.1 Connect a BC11-T cable from AD11-K J2 to AM11-K J1.

6.2 Connect the BC08R-08 cable from AD11-K J1 to AM11-K J3.

6.3 Connect G5036 test module to J2, J4 or J5 depending on which bank of channels on the AM11-K are to be tested; i.e., J2 - CH20 - 37, J4 - CH40-57, J5 - CH60-77.

NOTE: G5036 module connects to the AM11-K via a BC08R-01. This cable should be installed upside down, i.e., A-VV instead of A-A.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 Load program through the appropriate load media.

7.2 Program start address

7.2.1 Load address 200

7.2.2 Start 000000 (SR) standard switch settings

7.3 Alternate Switch Settings

7.3.1 SW15 = 1 Halt on error

7.3.2 SW14 = 1 Loop on test

7.3.3 SW13 = 1 Inhibit error typeouts

7.3.4 SW12 = 1 Halt for VT55 display

7.3.5 SW11 = 1 Inhibit iterations

7.3.6 SW10 = 1 Bell on error

7.3.7 SW09 = 1 Loop on error

7.3.8 SW08 = 1 Loop on test in SWR 7:0

7.4 Operator Action

A message is printed with a list of subtests that the user may select. For acceptance verification, the only test to be selected is test "A", the auto test. Before running the test, a 1 location patch is necessary to select one of three base addresses of the channels to be tested Refer to Section 6.3 for channel selection. The location "base CH" should be patched for 20 (channels 20-37 to be tested), 40 (channels 40-57 to be tested) or 60 (channels 60-77 to be tested).

NOTE: If BC5036 wraparound test board is not available, refer to the AM11-K Mfg. & Field Acceptance Procedure A-SP-AM11-K-5 Section 7.2 for alternative testing.

7.5 Evidence of End Pass or Estimated Run Time

When running the auto test "END PASS" will be typed. Each pass of the auto test takes approximately 10 minutes.

7.6 Acceptable Errors

NONE

7.7 Procedure #Restart After Repair

Repeat steps 7.2 through 7.6.

NOTE: If analog section of the option is repaired, recalibration may be necessary. Refer to AM11-K calibration procedure for further instructions.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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE LSP-11 SYSTEM CHECKOUT & ACCEPTANCE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6130					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekerawski	Tom Sekerawski	A	SP	MAA6130-0-0	A

LPS-11 SYSTEM CHECKOUT & ACCEPTANCE

1.0 LPS-11 Setup and Calibration

Refer to Document DEC-11-HLPMA-B-D

1.1 LPS-11 Acceptance Procedure

Refer to Document A-SP-LPS11-S-14

1.2 Diagnostic Package

A) LPS-11 Test I MAINDEC-11-DZLPC
B) LPS-11 Test II MAINDEC-11-DZLPD
C) M7023 Digital I/O Test MAINDEC-11-DZLPI-A

Other Related Documents

LPS-11 System Users Guide DEC-11-HLPMA-B-D

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE 16 CHANNEL 12 BIT A/D FOR PDP-11/03 - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6135					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelenjawski	Tom	A	SP	MAA6135-0-0	A

MANUFACTURING SPECIFICATION

TITLE

MODULAR APPROACH TO SYSTEMS TEST

16 CHANNEL 12 BIT A/D FOR PDP-11/03

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeup. For the purpose of expediency, the procedure has been kept brief, and to the point, to keep from confusing the user. For additional information, it will be necessary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD 116)

2.2 Engineering Specifications SP-ADV11-A-3

2.3 ADV11-A Print Set

2.4 EK-ADV11-OP-001 ADV11-A, KWV11-A, AAV11-A, DRV11 Users Manual

2.5 11L03 Manufacturing Specifications

3.0 REQUIRED TEST EQUIPMENT

3.1 LSI11 Standard Computer with 8K of memory

3.2 Test connecter 70-12894

3.3 Precision voltage source: Electronic Development Corp. (EDC) VS-11N or equivalent.

3.4 ADV11-A module

3.5 Output terminal/DLV11

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC 11 - DVADA ADV11-A Performance Test Diagnostic and writeup.

4.2 MAINDEC 11 - DXADC DEC/X11 Exerciser and writeup.

5.0 SPECIAL INSTRUCTIONS AND CHECKS

5.1 If an H322 distribution panel is present, then connect ADV11-A by means of a BC08R-06 cable from J1 of module to J10 of the H322 (all C and D variations of 11L03)

5.2 When an ADV11-A and a KWV11-A are both present in the system module, jumpers (DEC 7010771) are installed from the KW output tab (CLK) to the A/D clock overflow tab (C) and from the KW tab (ST1) to the A/D tab(s).

5.3 Two RF shields are provided with each ADV11-A. They are installed on each side of the module.

5.4 If the ADV11-A is hooked up to an H322, then SEL signal must be grounded on the H322 so that the A/D is shipped to the customer in single ended mode. To accomplish this, connect a wire between J8 top screw terminal (SE signal) to J7 top screw terminal (logic GRD) on the H322.

6.0 TEST SET UP

6.1 Insure switch packs S2 and S1 are set up for a device address of 170400, and a vector of 400 respectively.

6.2 Install module in slots A thru D03 of CPU box C and D variations of 11L03.

6.3 Install test connecter 70-12894 in Berg Connecter J1 of module.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 ADV11-A Performance Test (DVAFA)

7.1.1 Load program through appropriate load media.

7.1.2 Summary of available tests and character typed to execute.

Character Typed	Test
W	Wrap around test
C	Calibration test
P	Print values test
L	Logic tests
A	Wraparound and logic tests

* NOTE 1: Wraparound test requires Berg Test Connecter to run.

NOTE 2: Program will give instructions on calibrating upon typing C.

7.1.3 Program starting addresses

7.1.3.1 200 - For normal test
7.1.3.2 204 - Restart
7.1.3.3 210 - Option area burn-in

7.1.4 Alternate Software SR settings (176)

7.1.4.1 SWR15 = 1 Halt on error
7.1.4.2 SWR14 = 1 Loop on test
7.1.4.3 SWR13 = 1 Inhibit error typeouts
7.1.4.4 SWR12 = 1 Halt for VT55 Display
7.1.4.5 SWR11 = 1 Inhibit iterations
7.1.4.6 SWR10 = 1 Bell on error
7.1.4.7 SWR 9 = 1 Loop on error
7.1.4.8 SWR 8 = 1 Loop on test in SWR <7:0>

7.1.5 Operator Action

7.1.5.1 Set SWR bits as desired.
7.1.5.2 Type 200G
7.1.5.3 Type character to run desired test.

7.1.6 Evidence of End of Pass

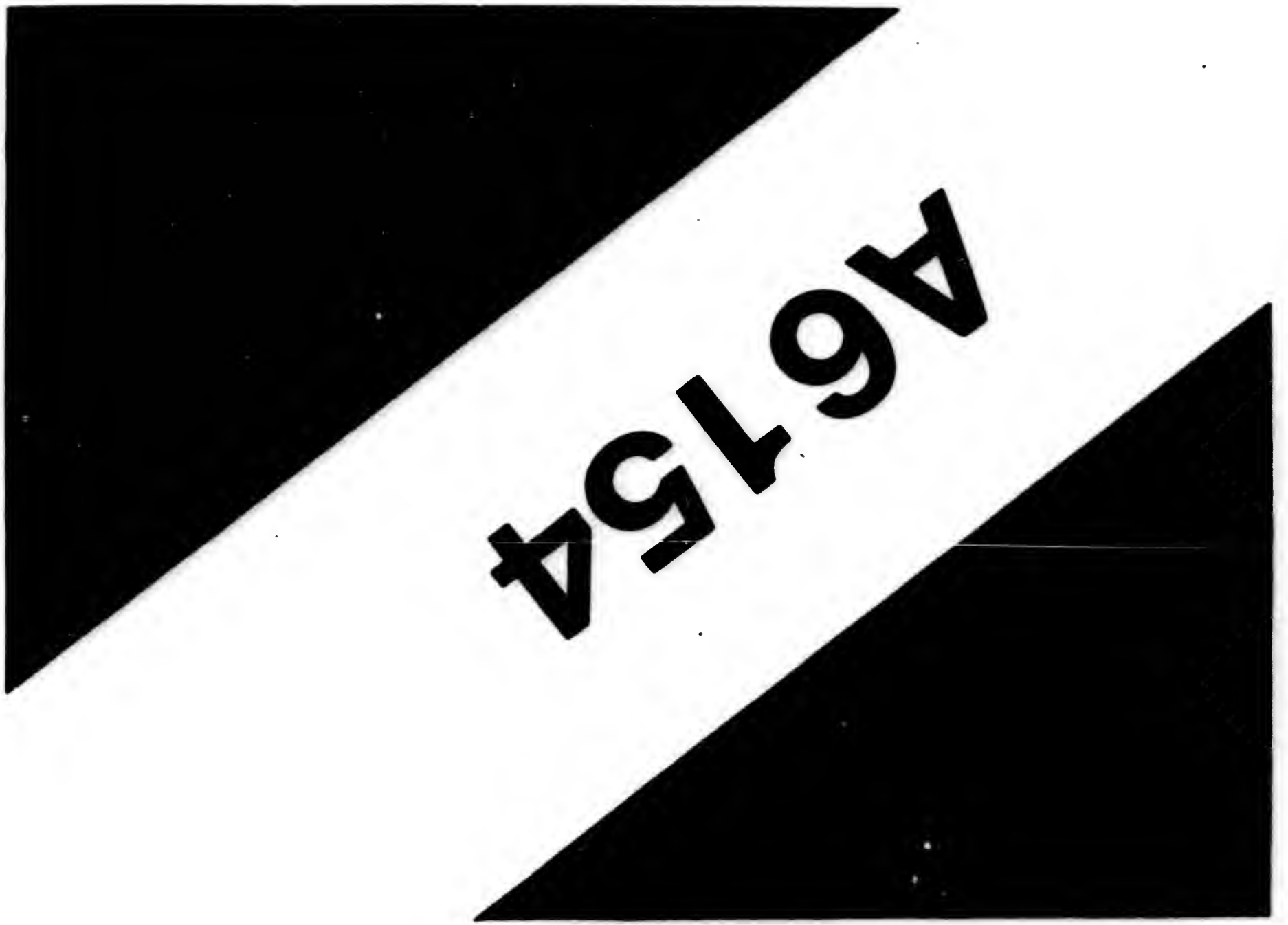
At end of pass, the following typeout will occur:

"END PASS GOOD UNITS 000000000000011"
This indicates that units 1 and 2 have run without failure.

7.1.7 Execution time for each test is:

Calibration:	5 conversions/min. @110 baud
Print Valves:	8 conversions/8 seconds @ 110 baud
Wraparound:	7 minutes first pass;32 minutes for successive passes
Logic:	1 minute
Auto:	8 minutes first pass; 33 minutes for successive passes

7.1.8 Acceptable Errors: None


A6154

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 5/7/81

TITLE M.A.S.T. IB11

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	New Release	ML013				6/2/81

ENG Art Richard	APPD Bob Beck	SIZE A	CODE SP	NUMBER MA-A6154-0-0	REV A

IB11

1.0 INTRODUCTION:

1.1 The IB11 option is a hardware/software package that allows test and measurement instruments that are IEEE bus compatible to be interfaced with the PDP-11 Unibus. The IB11 consist of a DW11 Unibus to Q-bus Interface, DDV11 Backplane, and IBV11 IEEE Instrument Bus Interface.

2.0 REFERENCE DOCUMENTATION:

2.1 Manuals & Engineering Specification:

2.1.1	IB11 Unibus to IEEE Instrument Bus Interface Installation Manual	EK-IB11A-IN
2.1.2	DW11 Unibus to LSI-11 Bus Installation Manual	EP-DW11A-IN
2.1.3	IBV11-A LSI-11 Bus to Instrument Bus Interface User's Manual	EP-IBV11-UG

2.2 Prints and Schematics:

2.2.1	IB11 Field Maint. Print Set	MP00620
2.2.2	DW11 Unibus to Q-bus Print Set	MP00459
2.2.3	IBV11-A LSI/IB Interface Print Set	MP00274

3.0 REQUIRED TEST EQUIPMENT:

3.1 PDP-11 with 16K words of memory.

3.2 Console terminal such as an LA36, LA120 or equivalent.

3.3 Appropriate load media.

3.4 Digital Volt Meter (DVM), accurate to .1V @ 15 volts.

4.0 REQUIRED DIAGNOSTIC PROGRAMS:

4.1 CVIBB?? IBV11-A Diagnostic

5.0 SPECIAL INSTRUCTIONS:

5.1 When installing the M8217 module into an available Unibus backplane SPC slot, the NPG in/NPG out jumper CA1 to CB1 must be removed.

6.0 INSTALLATION & TEST SET-UP INSTRUCTIONS:

6.1 Visual Inspection:

6.1.1 Check for any structural damage to modules such as broken components, cut etches, etc.

6.2 Module Switch Configuration:

6.2.1 The first M7954 module switches are configured as follows:

Reference Figures 1, 2, and 3.

For Bus address 160150:

S2 - switches 7, 8, & 10 on.
switches 1, 2, 3, 4, 5, 6, & 9 off.

For vector address 420:

S1 - switches 1, 5, & 8 on.
switches 2, 3, 4, 6, & 7 off.

6.2.2 Other M7954 modules to be added to the system will use floating address and vector assignments.

6.3 Module Cabling:

6.3.1 Two BC05L-06 cables connect from the M8217 to the M9401 module. See Figure 4. The red stripe on the cables must be adjacent to connectors pins VV/UU on both modules.

6.4 Module Placement:

Refer to Figures 5 and 6.

6.4.1 The M8217 is placed in a available Unibus backplane SPC slot.

6.4.2 The M9401 module is placed in slot A/B01 of the DDV11-C LSI-11 Bus backplane.

6.4.3 The M7954 Instrument Bus module is normaly placed into slot C/D01 of the DDV11-C LSI-11 Bus backplane. If more M7954 modules are to be added, install into slots noting device priority. See Figure 6.

6.4.4 The M9400-YB Terminator module is placed into the slot just after the last M7954. Normaly C/D02 of the DDV11-C.

7.0 POWER CHECKS:

The following voltage should be present on the respective backplane pins:

VOLTAGE	TOLERANCE	BACKPLANE LOC.
+5 V.D.C.	4.75V to 5.25V	AA2, BA2, or CA2

8.0 DIAGNOSTIC TEST PROCEDURE:

Note: For the specific sequence of diagnostics to be run in any particular situation, and for current MAST minimum test criteria (e.g. pass-counts, etc.), refer to the appropriate MAST CHECKLIST. The following is a list of step-by-step instructions for executing each individual diagnostic contained in the CHECKLIST.

8.1 CVIBB?? IBV11-A Diagnostic

8.1.1 Starting instructions:

Starting address is 200.

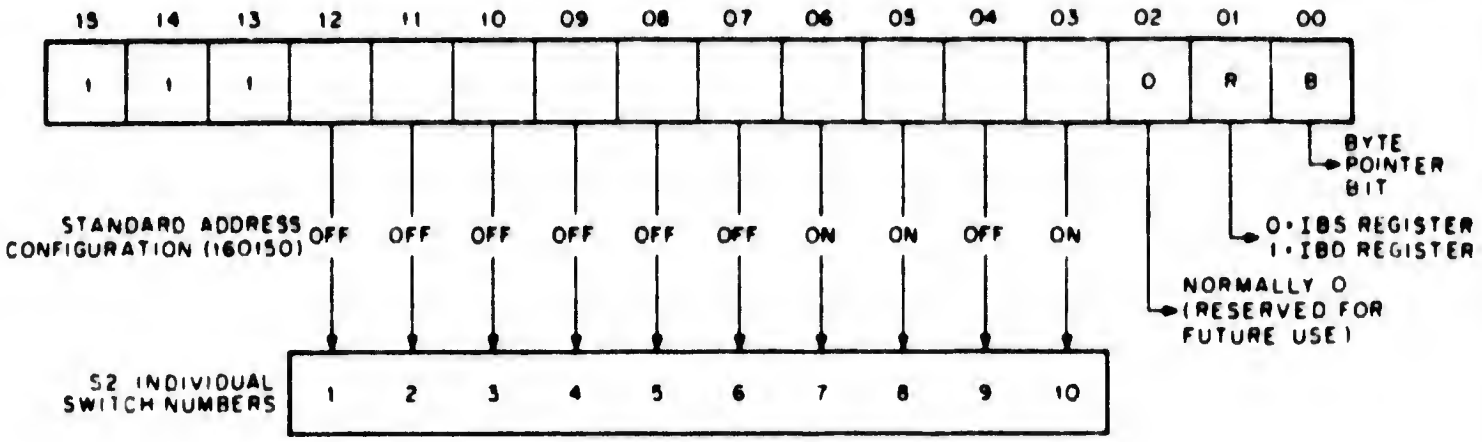
CVIBBA IBV11A DIAGNOSTIC

SWR = 000000 NEW = <CR>

END PASS# 1

END PASS# 2

8.1.2 No errors are allowed.

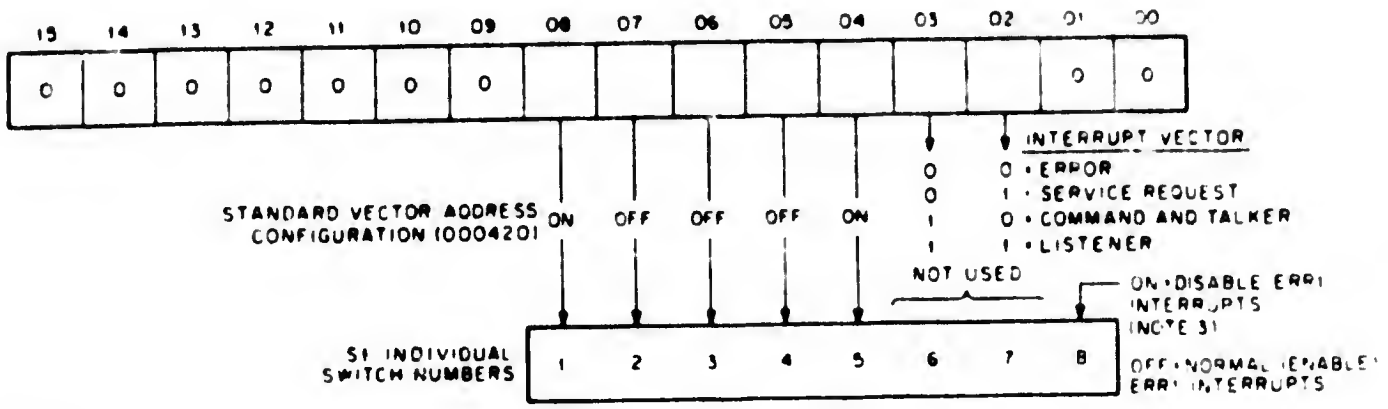


NOTES.

1 OFF • Logical 0; ON • Logical 1

2 Only the IBS REGISTER ADDRESS is configured via S2 The IBD REGISTER ADDRESS always equals the IBS REGISTER ADDRESS +2.

Figure 1 M7954 Device Address Selection



NOTES

1 OFF • Logical 0, ON • Logical 1

2 Only the VECTOR ADDRESS bits (8 4) are configured via S1 Bits 3 and 2 are IBV11-A hardware-selected for the functions shown

3 S1-8 OFF • IBV11 is the only system controller connected to the instrument bus
S1-8 ON • Another system controller is connected to the instrument bus

Figure 2 M7954 Interrupt Vector Address Selection

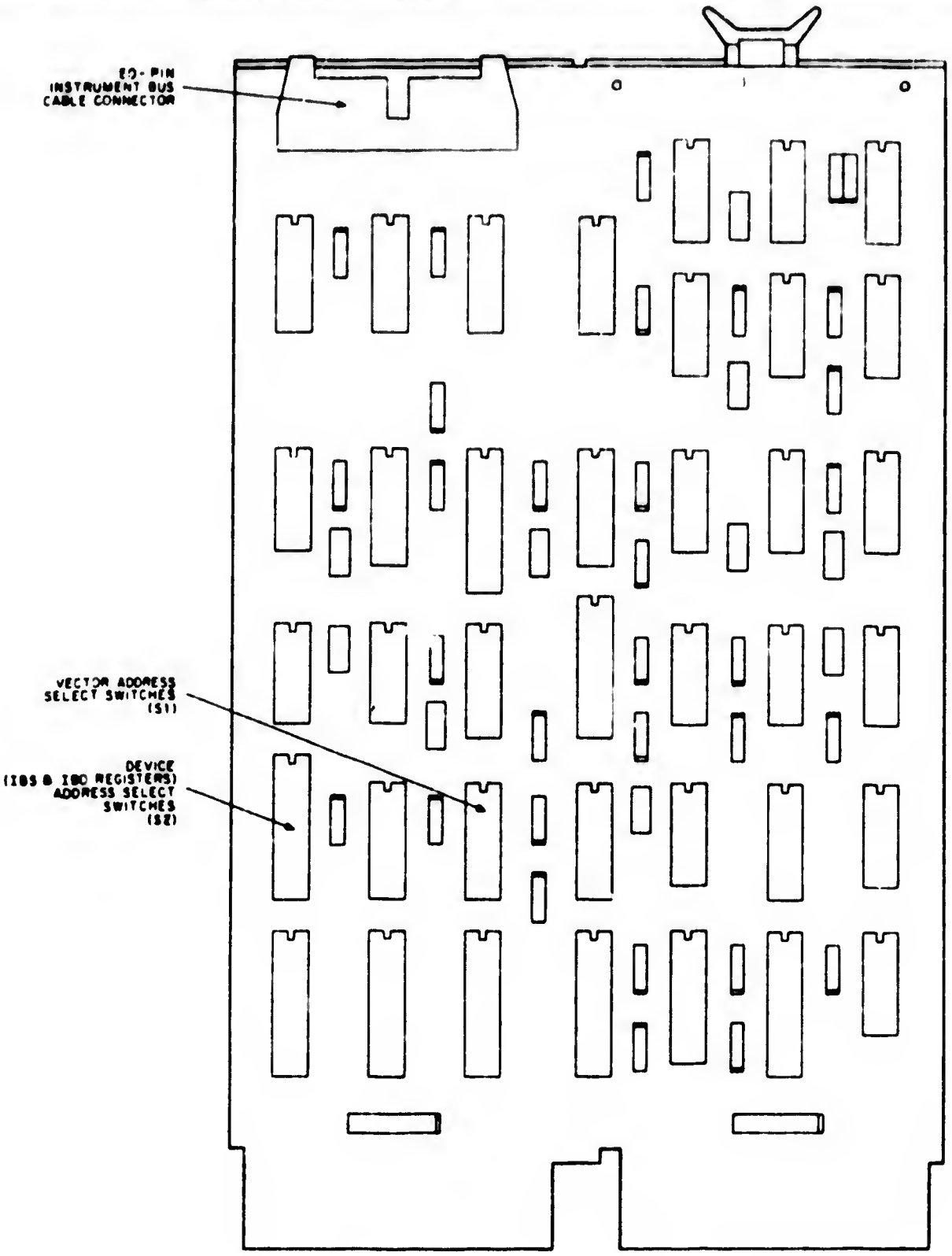
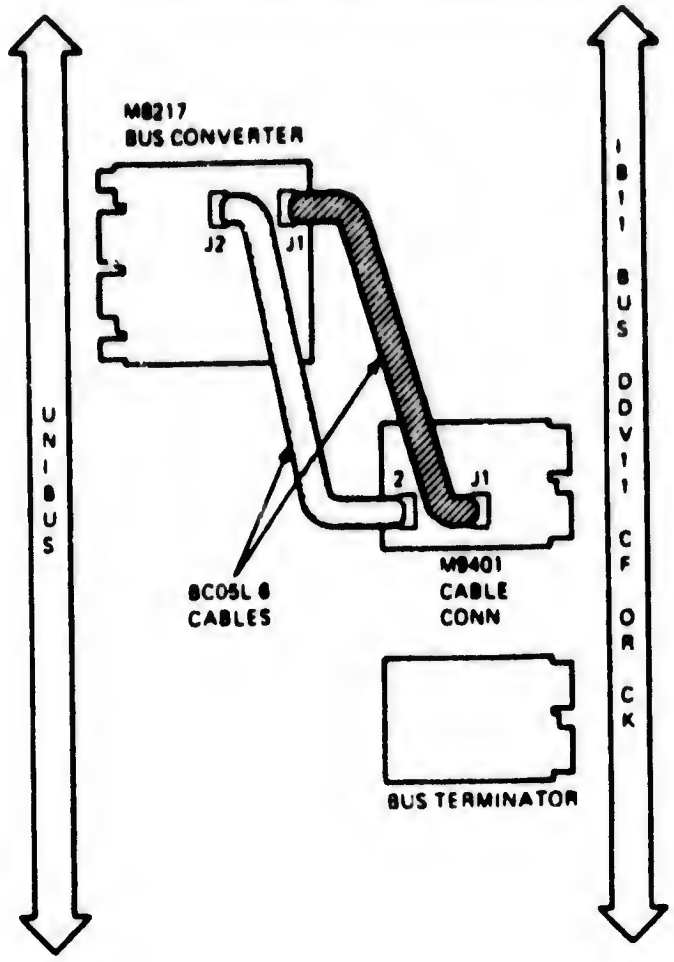


Figure 3 M7954 Module Switch Locations



IBI1 Interconnecting Diagram

Figure 4

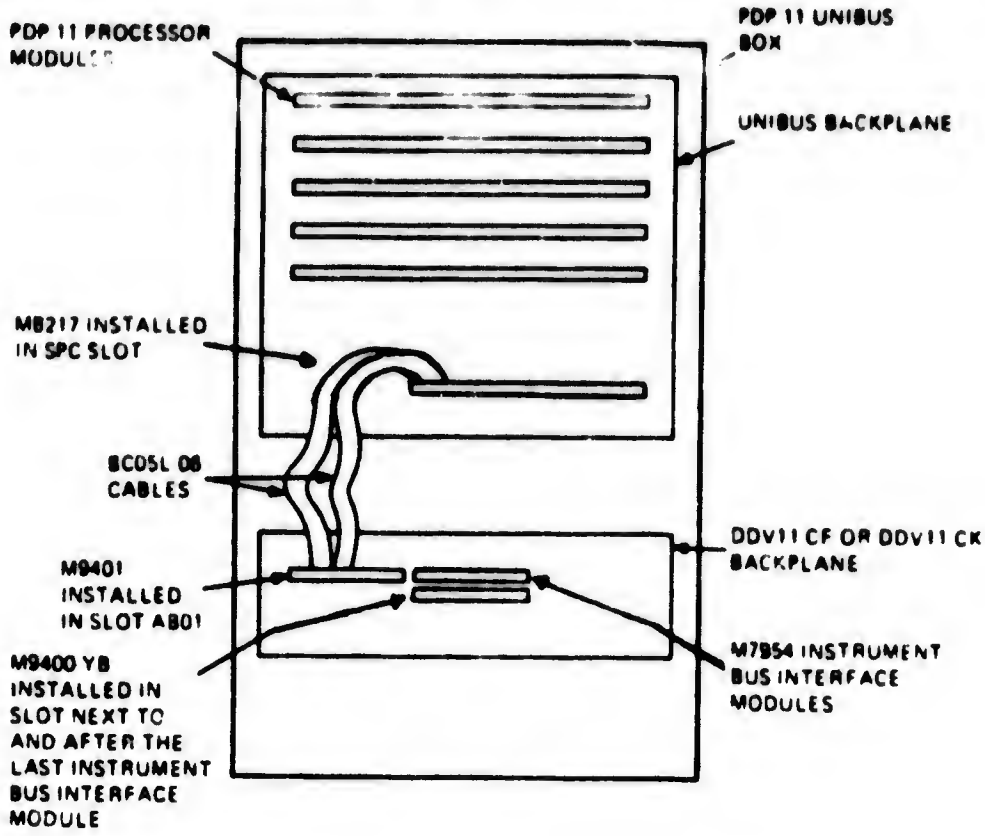


Figure 5 IB11 Option in a PDP-11 Processor Box

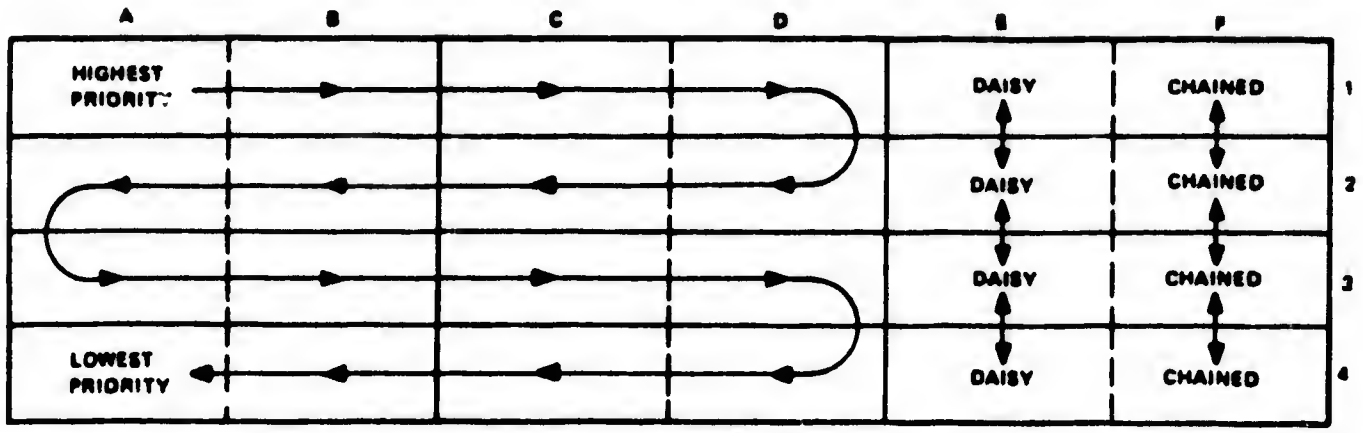


Figure 6 DDV11-C Backplane Priority Assignments


A6160

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE ICS-11 INDUSTRIAL SUB-SYSTEM PROCEDURE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	Prev. 7668001-0-6160					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekenkewski		A	SP	MAA6160-0-0	C

ICS-11 INDUSTRIAL SUB-SYSTEM PROCEDURE

1.0 SPECIAL INSTRUCTIONS

1.1 No slots may be empty between A005 and A007 modules.

1.2 W7440 modules must never be installed in ICS file slot #9.

1.3 A907 must be installed between A005/A007 and the M8030/ M8050 module (s), when the latter is located within four (4) slots of the A005/A007 module (s).

1.4 ICS-J continuity Jumper Card must be installed in the "F" connector block of all open slots between the first and last interrupting module of a file.

1.5 Mercury wetted relay modules (A005, A007, M8030, M8050) must reside in a vertical plane for a period of at least one (1) minute, to prevent module damage resulting from a shorted relay.

1.6 Interrupting modules closest t the control module has highest priority within the file, and that file closest to the processor has highest priority within the ICS11.

1.7 Options IAC-IA, IAC-IB, IAC-OA, and IAC-OB shall be system tested as IDC-ID, IDC-IE, IDC-OA, and IDC-OB respectively.

Modules used in these configurations must have jumper W1 installed, only after completion of all system testing.

1.8 The A005-YA is a computer Special System's variant, that shall require program modifications to the in-house AUTOCAT diagnostic.

1.8.1 Reference Table 5 for diagnostic changes.

1.8.2 Reference A-SP-A005-0-8, Section 7, for A005-YA explanation.

1.8.3 Field Service shall reference Table 6 for calibration test parameters when using the ICS Field Test Program.

1.8.4 FA&T shall reference the ICS Field Test Program when performing re-calibration of the A005-YA.

2.0 REFERENCE DOCUMENTS

Manuals	EK-ICS11-MM
Checkout Procedures	A-SP-A6330-0-5 A-SP-7010596
Acceptance Procedures	A-SP-A6330-0-5 A-SP-7010596
F.S. Acceptance	A-SP-ICS11-M-5
Module Test Procedures	A-SP-7010327-0-1 A-SP-7011020-0-1 A-SP-14/30-0-5 A-SP-ICS11-M-6
Engineering Specifications	A-SP-M6850-0 A-SP-M6870-0-8 A-SP-M8030-0-8 A-SP-M8050-0-8 A-SP-W7410-0-8 A-SP-W7411-0-8 A-SP-W7430-0-8 A-SP-W7431-0-8 A-SP-W7440-0-8 A-SP-ICS11-M-4 A-SP-A005-0-8 A-SP-A007-0-8 A-SP-A907-0-8 A-SP-6330-0-8 A-SP-H1501-0-1 A-SP-ICS11-M-6
Prints	B-DD-ICS11-M B-DD-H912-0 B-DD-IDA-0 B-DD-ICJ-I B-DD-ISH-I B-DD-IDC-0 B-DD-IDC-I B-DD-IAD-I B-DD-IMX-I B-DD-IRL-0 B-DD-7010596-0 B-DD-7010327-0

MainDec Listings

AUTOCAT-11-QZICA (FA&T only)
AUTOCAT-11-QZICB (Module Test only)
AUTOCAT-11-QZICC (Module Test only)
MD-11-DZICA (Field Serv. only)

3.0 REFERENCE TEST EQUIPMENT

3.1 7010596 System Tester (in-house).

3.2 Oscilloscope, tektronic 465 or equivalent.

3.3 A6330, DAC Tester.

3.4 "11" family processor, with 8K memory.

4.0 SPECIAL INSPECTION/CHECK

4.1 Ensure system components agree with ICS line items on the Customer Requisition form.

4.2 Ensure an electromagnetic shield is present between the M8090 and the first I/O module for each ICS File Box.

4.3 Verify each ICS File Box module (s) are installed according to the approved priority sequence table. See Table 1.

4.4 Verify File Box (s) are securely grounded to the mounting cabinet and that the latter is secured system power ground. (use ohm meter)

5.0 CONFIGURATION GUIDELINES

5.1 All ICS option modules are to be installed using the slot-priority sequence table. See Table 1.

5.2 H912 mounting terminals must not be installed in cabinets containing sensitive equipment, such as disks or tapes.

6.0 TEST SET-UP

Refer to test procedures A-SP-7010596-0-0 and A-SP-A6330-0-5.

Module Configuration; see Table 1 through 4.

7.0 SYSTEM INTEGRATION TEST PROCEDURE

7.1 Power up both the system tester and the system under test. Also, if the IDA-OA option tester is to be used at this time, it should also be turned on. Allow 30 minutes for this system and test gear to stabilize.

7.2 ICS11 Systems Test Program

NOTE: This diagnostic requires the use of a ICS system tester.

7.2.1 Load the ICS systems test program diagnostic AUTO-CAT-11-QZIRA using standard Digital Loading Procedures.

7.2.2 Set switch register to 200, load and start.

7.2.3 Enter the octal number of the file to be tested.

7.2.4 Enter the vector address of the same file. Addre range 234-777.

7.2.5 Enter (self (cr)). This will automatically run a self test of the system tester to verify that all internal workings of the tester are operative. Should errors be encountered during this run, repairs should be instituted before proceding.

NOTE: System tester cables should be disconnected from the following option modules before attempting to run "self test". If not, false interrupts may be generated by the customer's file. IDC-IB, IDC-IC, IDC-IE and IAD-IA.

7.2.6 Enter (Z (cr)) to clear any previous job buffer entry.

7.2.7 Enter the I/O options mounted within the ICS file to be tested. This file may be 1 or 12 possible files on the system.

7.2.7.1 Should the file configuration include IDA-OA options, (A6330) do not enter them at this time.

NOTE: It is not necessary to remove this option while testing all other options, but do disconnect the DC input from the IDA-OA option tester. (ref. A-SP-A6330-0-0 option test procedure).

SAMPLE ENTRY

#EA005 (CR) - Enter one A005 in slot address 00 to real address 171000. Module connected to system testers analog cable.

#EA007,4 (CR) - Enter four A007's in slot addresses 02,04, 06 and 10 real addresses 171002 to 171010 modules connected to system testers analog cables.

#EW7411,5 (CR) Enter five W7411's in real addresses 171012 to 171022,modules connected to system tester DC cables 0-4

#S=30 (CR) Set slot address equal to 30. NOTE: We are not running A6330's at this time, so slot addresses 24 and 26 have been bypassed.

#EM6850,4 (CR) Enter four M6850's in slot address 30 thru 36. Real addresses 171030 thru 171036.

This completes the loading of the program job buffer to run all modules with the exception of both A6330's.

7.2.8 Type in (L (CR)) to obtain the module entry loaded into the program. This should be checked against your entry to verify that all entries were made correctly.

7.2.9 After entering the modules into the job buffer, type in (K (CR)). The program will respond with K ON. This will enable the program to run non stop.

7.2.10 Type in (R (CR)). This will initiate the test on the file box. NOTE: Should the program be halted during pass 2, it should not be restarted for 30 minutes, if IAD-IA options are within the filebox configuration. This is to allow for stabilization of flying caps mounted on this module.

7.2.11 Run the diagnostic for a minimum of (1) time specified, or (1) complete pass. Whichever is longer.

7.2.11.1 The current pass count can be obtained by typing "p" on the teletype. NOTE: If the ICS file has a maximum load of (16) analog modules (worst case diagnostic run time) a complete pass will take approximately 1½ hours.

7.2.11.2 Connect all I/O cables from the ICS to the H009 MTG panel (after tests have been run successfully in Acceptance), and have QC inspect the installation.

7.3 ICS11 Field Test Program

NOTE: This diagnostic requires the use of a field UDC/ICS tester.

7.3.1 Ref. Specification A-SP-ICS11-M-5 for indepth explanation.

7.4 ICS-11 Systems Test Program In Conjunction with A6330 DAC Tester.

7.4.1 Disconnect all I/O system tester cables from the files that were previously tested.

7.4.2 Five A6330's can be connected to the option tester at this time, but they will have to be scoped independantly of one another.

7.4.3 Enter (Z CR) on the teletype to clear all previously entered jobs.

7.4.4 Enter (K CR) on the teletype to check what state the "K" command is in. The K command for this test should be in the off mode.

7.4.5 Enter the slot address location for all the IDA-0A options within the file.
NOTE: only (5) five IDA-0A options can be connected to the tester. If others are present, they can be tested upon the completion of this test.

Example of loading technique to be used for IDA-0A options:

S = 24 cr Set slot address equal to 24
E A6330, 2 <cr> Enter A6330's in slot addresses 24 and 26 real addresses 171024 and 171026, Jobs 0 and 1 respectively.

7.4.6 Adjust all settings for the scope, and switch the option tester to the first option (card/cable output) Job 0. (reference A6330 option test procedure A-SP-A6330-0-5.)

7.4.7 Type in RJ0<cr>. This will initiate pass 1 testing on the first IDA-0A option or Job 0 at slot address 171024. (see step 7.4.5) ramps will be outputed to the option for scope measurements.

7.0 SYSTEM INTEGRATION TEST PROCEDURE CONT.

7.4.8 Compare the scope waveform against the tolerences indicated within the option test procedure A-SP-A6330-0-5. If the option is found to be within tolerence, proceed to the next step. If not,repair, adjust, or replace the option, and retest until acceptable.

7.4.8.1 To adjust the A6330, or IDA-0A Option, proceed as follows: (Ref. Figure 1)

A. First measure the cards reference voltage between "TP2" and "IPG". It should be +2 volts ± 2mv. If out of spec, use the "+2 v adj." pot to adjust it within tolerence.

B. Set the thumbwheel switch to the card under test.

C. Set the thumbwheel switch to channel 0 or the first voltage output.

D. Adjust the pot "D/A 0" gain adjust for channel 0. The output on the scope should be adjusted within the ± 20mv tolerence.

E. Set the thumbwheel switch to channel 2 or the second voltage output.

F. Repeat step D, but use pot marked "D/A 1" gain adjust.

G. Repeat steps C thru F for remaining two voltage channels 2 and 3 (thumbwheel settings 4 and 6 respectively).

H. Reset thumbwheel switch to channel 1. This is the first current output channel.

I. Adjust the current offset of channel 1 as close as possible to ground by using pot. "off 0".

7.0 SYSTEM INTEGRATION TEST PROCEDURE CONT.

J. Adjust the current gain of channel 1 to fall within the required ± 20 mv tolerence.

K. Reset the thumbwheel switch to channel 3 or the second current output.

L. Repeat steps I thru J and repeat these steps for the remaining current outputs channels 5 and 7.

7.4.9 Type "Control C" to terminate the test.

7.4.10 If other IDA-0A options have been entered, type in the next job to be run. Repeat steps 7.4.7 thru 7.4.9 until all jobs have been tested.

7.4.11 Turn "K" command on by typing "K" on the terminal.

7.4.12 Enter R <cr> and run all IDA-CA options entered in step 6.4.5 for (1) hour. With the "K" command on, pass 2 will only be run during this test. It is not necessary to scope the outputs for this test.

7.4.13 Type "Control C" to terminate the test.

7.4.14 Repeat steps 7.4.6 thru 7.4.10. Should any of the options fail, repair and repeat all tests.

7.4.15 If there are more than (5) five IDA-0A options within this file, it will be necessary to repeat steps 7.4.5 thru 7.4.14 to test the remaining.

7.5 Repeat all tests 7.0 thru 7.4.15 for all other files on the systems configuration.

TABLE 1

FILE BOX - MODULE PRIORITY TABLE

PRIORITY SEQUENCE	MODULE	OPTION	COMMENTS
1	A005	IAD-IA	
2	A007	IMX-IA	7 MAX
3	A005	IAD-IA	
4	A007	IMX-IA	7 MAX
5	A907	ISH-IA	
6	W7410	IDC-IA	
7	W7411	IAC-IA	H912, + BC40J
8	W7411	IDC-ID	
9	W7440	IDC-IC	
10	W7430	IDC-IB	
11	W7431	IAC-IB	H912, + BC40J
12	W7431	IDC-IE	
13	A6330	IDA-0A	12 MAX
14	M6870	IDC-0B	
15	M6870	IAC-0B	H912, + BC40J
16	M6850	IDC-0A	
17	M6850	IAC-0A	H912, +BC40J
18	M8030	IRL-0A	
19	M8050	IRL-0B	

TABLE 2

A005 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W108 W111	OUT IN	INTERRUPT MODE ICS-11

A007 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W21	OUT	SELECT MUX # 1
W22	OUT	SELECT MUX # 2
W23	OUT	SELECT MUX # 3
W24	OUT	SELECT MUX # 4
W25	OUT	SELECT MUX # 5
W26	OUT	SELECT MUX # 6
W27	OUT	SELECT MUX # 7

W7430 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W58 W59	IN OUT	INTERRUPT MODE ICS-11

W7431 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W 9 W10	OUT IN	INTERRUPT MODE ICS-11

TABLE 3

W7440 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W 2	IN	ICS-11
W16	OUT	INTERRUPT MODE

M8090 STANDARD JUMPER CONFIGURATION

File No.	ICSR/ICAR JUMPERS									
	A12 W22	A11 W21	A10 W20	A9 W19	A8 W18	A7 W17	A6 W16	A5 W15	A4 W14	A3 W13
00	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT
01	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	IN
02	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	IN	OUT
03	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	IN	IN
04	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	OUT	OUT
05	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	OUT	IN
06	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	IN	OUT
07	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	IN	IN
08	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	OUT	OUT
09	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	OUT	IN
10	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	IN	OUT
11	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	IN	IN

Jumper OUT = Logic "1"
Jumper IN = Logic "0"

TABLE 4

M8090 STANDARD JUMPER CONFIGURATION

FILE JUMPERS

AD7 W12	AD6 W11	AD5 W10	AD4 W 9
IN	IN	IN	IN
IN	IN	IN	OUT
IN	IN	OUT	IN
IN	IN	OUT	OUT
IN	OUT	IN	IN
IN	OUT	IN	OUT
IN	OUT	OUT	IN
IN	OUT	OUT	OUT
OUT	IN	IN	IN
OUT	IN	IN	OUT
OUT	IN	OUT	IN
OUT	IN	OUT	OUT

Jumper OUT = Logical "1"
Jumper IN = Logical "0"

M8090 STANDARD JUMPER CONFIGURATION

File No.	Vector Address	VECTOR ADDRESS JUMPERS						
		D8 W7	D7 W6	D6 W5	D5 W4	D4 W3	D3 W2	D2 W1
00*	234	IN	OUT	IN	IN	OUT	OUT	OUT
01**	300	IN	OUT	OUT	IN	IN	IN	IN
02	304	IN	OUT	OUT	IN	IN	IN	OUT
03	310	IN	OUT	OUT	IN	IN	OUT	IN
04	314	IN	OUT	OUT	IN	IN	OUT	OUT
05	320	IN	OUT	OUT	IN	OUT	IN	IN
06	324	IN	OUT	OUT	IN	OUT	IN,	OUT
07	330	IN	OUT	OUT	IN	OUT	OUT	IN
08	334	IN	OUT	OUT	IN	OUT	OUT	OUT
09	340	IN	OUT	OUT	OUT	IN	IN	IN
10	344	IN	OUT	OUT	OUT	IN;	IN	OUT
11	350	IN	OUT	OUT	OUT	IN	OUT	IN

Jumper OUT = Logic "1" Jumper IN = Logic "0"

TABLE 5

AUTOCAT DIAGNOSTIC "PATCHES"

ADDRESS TO BE CHANGED		
ICS11 AUTOCAT-11-QZICA	ICR11 AUTOCAT-11-QZICA	NEW CONTENTS
033210	033272	100020
033230	033312	100420
033250	033332	100066
033270	033352	100100
033310	033372	100500
033330	033412	100466
033346	033430	100000
033350	033432	101001
033370	033452	101004
033410	033472	101066
033530	033612	101466
033550	033632	101404
033566	033650	100000
033570	033652	101401

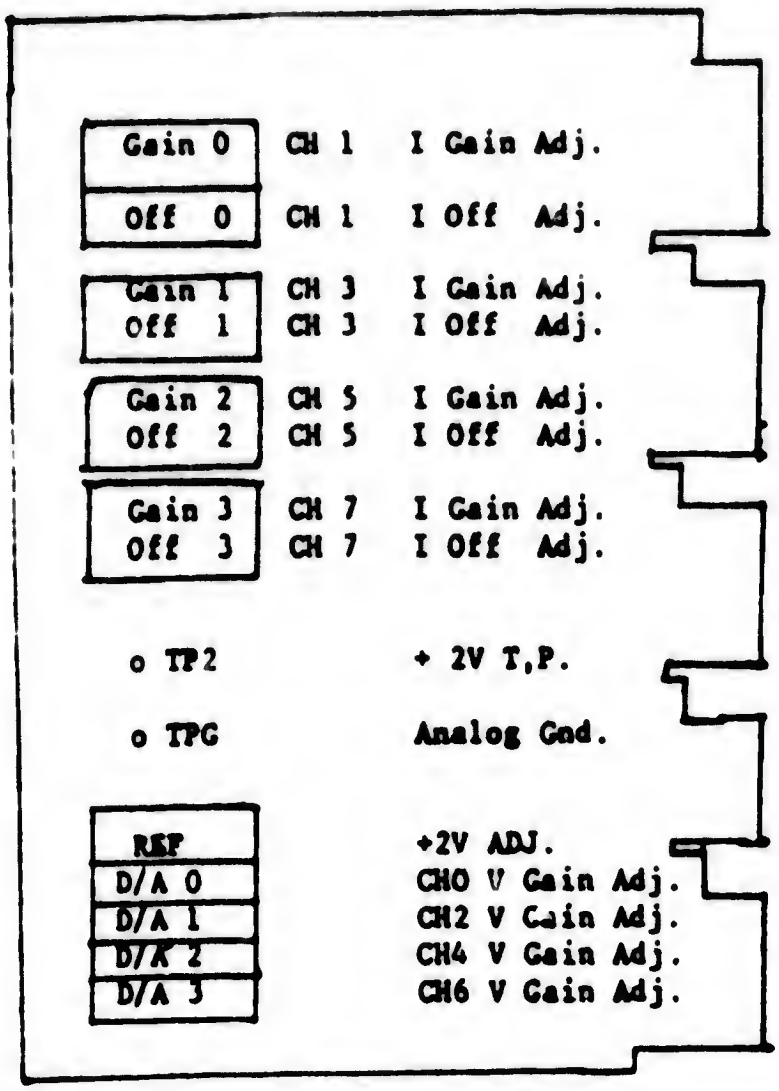
TABLE 6

CALIBRATION TABLE FOR A005-YA

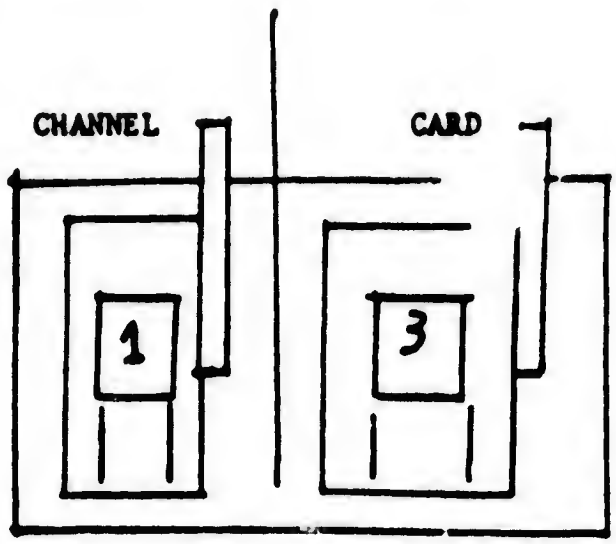
EDC Output			Channel		Average		Tolerance (LSB)	
Bipolar	Unipolar	Gain	A005-YA	A007	Bipolar	Unipolar	Bipolar	Unipolar
+0V	+0V	1000	10	*	0000	0000	+4	+6
+0V	+0V	500	10		0000	0000	∓2	∓3
+0V	+0V	250	10		0000	0000	∓2	∓3
+0V	+0V	125	10		0000	0000	∓2	∓3
+5MV	+5MV	1000	10	*	2000	4000	+5	+8
-5MV	----	1000	10		6000	----	∓5	--
+9MV	+9MV	1000	10		3463	7146	+5	+10
-9MV	----	1000	10		4315	----	∓5	--
+10MV	+10MV	500	10		2000	4000	∓3	+5
+36MV	+36MV	250	10		3463	7146	∓3	∓6
+40MV	+40MV	125	10		2000	4000	∓3	∓5
+0V	+0V	50	10		0000	0000	+2	+3
+0V	+0V	12.5	10		0000	0000	∓2	∓3
+0V	+0V	2.5	10		0000	0000	∓2	∓3
+0V	+0V	1	10		0000	0000	∓2	∓3
+180MV	+180MV	50	10		3463	7146	+2	+4
+400MV	+400MV	12.5	10		2000	4000	∓2	∓4
+3.6V	+3.6V	2.5	10		3463	7146	∓3	∓5
+5V	+5V	1	10		2000	4000	∓2	∓4
+9.9609V	+9.9609V	1	10	*	3770	7760	+3	+5
-9.9804V		1	10	*	4007	----	∓3	--
-5.0V		1	10		6000	----	∓2	--

* Channel to be used for each A007

A007 #	1	2	3	4	5	6	7
CHANNEL	21	42	63	84	105	126	147



A6330 DAC Module
Top View



VO -	0		0
IO -	1		1
V1 -	2		2
I1 -	3		3
V2 -	4		4
I2 -	5		5
V3 -	6		
I3 -	7		

THUMBWHEEL SWITCH
FRONT VIEW

FIGURE 1

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE ICR-11 INDUSTRIAL SUB-SYSTEM PROCEDURE - APPENDIX A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	Prev. 7668001-0-6165					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Jelenkiewski		A	SP	MAA6165-0-0	B

ICR-11 INDUSTRIAL SUB-SYSTEM PROCEDURE

1.0 SPECIAL INSTRUCTIONS

1.1 No slots may be empty between A005 and A007 modules.

1.2 W7440 modules must never be installed in ICS file slot #9.

1.3 A907 must be installed between A005/A007 and the M8030/M8050 modules (s), when the latter is located within four (4) slots of the A005/A007 modules (s).

1.4 ICS-J continuity Jumper Card must be installed in the "F" connector block of all open slots between the first and last interruping module of a file.

1.5 Mercury wetted relay modules (A005, A007, M8030, M8050) must reside in a vertical plane for a period of at least one (1) minute, to prevent module damage resulting from a shorted relay.

1.6 Interrupting modules closest to the control module has highest priority within the file, and that file closest to the processor has highest priority within the ICR-11.

1.7 Options LAC-1A, LAC-1B, LAC-0A, and LAC-0B shall be system tested as IDC-ID, IDC-IE, IDC-0A and IDC-0B respectively.

Modules used in these configurations must have jumper W1 installed, only after completion of all system testing.

1.8 The A005-YA is a computer special system's variant, that shall require program modification to the in-house AUTOCAT diagnostic.

1.8.1 Ref. table 7 for diagnostic changes.

1.8.2 Ref. A-SP-A005-0-8, Section 7, for A005-YA explanation.

1.8.3 Field Service shall reference table 8 for calibration test parameters when using the ICR-11 Field Test Program.

1.8.4 Reference the ICR -11 Field Test Program when performing recalibration of the A005-YA.

2.0 REFERENCE DOCUMENTS

Manuals:	EK-ICR11-MM
Checkout Procedures:	A-SP-A6330-0-5 A-SP-7010596
Acceptance Procedures:	A-SP-A6330-0-5 A-SP-7010596
F.S. Acceptance:	A-SP-ICR11-A-5
Module Test Procedures:	A-SP-7010327-0-1 A-SP-7011020-0-1 A-SP-14/30-0-5 A-SP-ICR11-A-7
Engineering Specifications:	A-SP-H1601-0-1 A-SP-M6850-0-8 A-SP-M6870-0-8 A-SP-M8030-0-8 A-SP-M8050-0-8 A-SP-W7410-0-8 A-SP-W7411-0-8 A-SP-W7430-0-8 A-SP-W7431-0-8 A-SP-W7440-0-8 A-SP-H772-0-3 A-SP-A005-0-8 A-SP-A007-0-8 A-SP-A907-0-8 A-SP-6330-0-8 A-SP-H1501-0-1 A-SP-ICR11-A-1
Prints:	B-DD-ICR11-A & C B-DD-H912-0 B-DD-IDA-0 B-DD-ICJ-I B-DD-ISH-I B-DD-IDC-0 B-DD-IDC-I B-DD-LAD-I B-DD-IMX-I B-DD-IRL-0 B-DD-7010596-0 B-DD-7010327-0

MainDec Listings:

AUTOCAT-11-QZIRA (FA&T only)
AUTOCAT-11-QZIRB (HVM only)
MD-11-DZIRA
MD-11-DZIRB (Field Service only)

3.0 REFERENCE TEST EQUIPMENT

3.1 7010596 System Tester (in-house) w/ I/O Entender cables.

3.2 Oscilloscope, tektronic 465 or equivalent.

3.3 A6330, DAC Tester.

3.4 "11" family processor, with 8K memory.

4.0 SPECIAL INSPECTION/CHECK

4.1 Ensure System Components agree with ICR line items on the Customer Requisition Form.

4.2 Ensure an Electromagnetic Shield is present between the M8096 and the first I/O Module for each ICS File Box.

4.3 Verify each ICS File Box Module (s) are installed according to the approved priority sequence table. See Table 1.

4.4 Verify File Box (s) are securely grounded to the mounting cabinet and that the latter is secured System Power Ground. (use ohm meter)

5.0 CONFIGURATION GUIDELINES

5.1 All ICS option modules are to be installed using the slot-priority sequence table. See Table 1.

5.2 H912 mounting terminals must not be installed in cabinets containing sensitive equipment, such as disks or tapes.

5.3 ICR modules are to be installed per approved placement. See Figure 1.

6.0 TEST SET-UP

Refer to test procedure A-SP-7010596-0-0 and A-SP-A6330-0-5. Module configuration: see Table 1 thru 6.

6.1 Mechanical Checkout

6.1.1 There are two distinct mechanical variations to the ICR11: the ICR11-A, which is a cabinet mountable version; and the ICR11-C (NEMA), which is enclosed for use in harsh industrial environments. Both units are electronically identical with the exception of a heat circuit present only in the ICR11-C.

6.1.2 The ICR11-C version will be shipped to the FA&T line on an enclosed skid. Before proceeding, it will be necessary to remove the shipping container cover. This is accomplished by removing (8) bolts at the base of the cover.

6.1.3 Remove top rear module card guides to allow for insertion of system test cables.

6.1.4 ICR11-A - Connect the I/O test cables to all options mounted within the file, except IAD-0A (A0005), IMX-IA (A0007), or IDA-0A (A6330). Options IAD-IA and IMX-IA require special test gear hardware, IDA-0A option tester. (reference procedures ICS/ICR systems tester procedure A-SP-7010596-0-0 and IDA-0A (A6330) Checkout Procedure A-SP-A6330-0-5 for detailed information on configuring and connecting those testers).

NOTE: Do not attempt to run IDA-0A options with IAD-IA and IMX-IA options connected to the system tester.

6.1.5 ICR11-C - All conditions in step 6.1.4 hold true for the ICR11-C, but it will be necessary to add extender cables to the I/O System Test Cables in order to make the necessary connections within the NEMA casting.

This can be best accomplished by opening the front door to the NEMA casting, and removing the four (4) file retaining screws. Slide the file forward about six (6) inches. Now open both side access doors to the NEMA. Connect the mating end of the extender cable to the I/O system test cable. Snake the remaining end up into the NEMA conduit hole located on the bottom of the casting. Work the cable up into the back of the casting until the connection can be made with the option mounted within the file.

6.1.6 It is best to connect options in the center of the file and work out to both ends. Each conduit hole is capable of excepting eight (8) cables, so if sixteen (16) options accompany the file, both conduit holes must be used. After all option cables are connected, slide the file back in, and close all three NEMA doors. All testing should be accomplished on the file in this manner.

6.1.7 Insert the Master Control and Interface Modules (M8094, and M8098) into the provided DD11B block or available SPC slots on the system. Be sure that all jumper locations are correct. (Ref.table 2-6)

6.1.8 Check the following hardware for proper installation against the ICR11 Engineering Print Set #B-DD-ICR11-A and C.

BC08 Cables (Master and Slave connections)-Teletype Jumper Connector #7011532 25 foot serial interface cable between master and slave M8098 modules #7011259.

NOTE: ICR11-C version only - disconnect the slave M8098 Digital cable from the inside bulkhead connection. This is necessary to facilitate mating of the serial interface test cable #7011259. Route the test cable up thru the bottom conduit hole before connecting to the pigtail.

6.1.9 Reference the ICS systems tester procedure #A-SP-7010596-0-0 for proper internal conversion and panel switch settings to be used on the system configuration to be tested.

NOTE: System Tester's BC11-A bus cable plugs into last unibus slot of the customer's system. DO NOT PLUG THIS CABLE INTO THE ICR FILEBOX UNDER TEST.

7.0 SYSTEMS TEST

7.1 Power up both the system tester and the system under test. Also, if the IDA-0A option tester is to be used at this time, it should also be turned on. Allow 30 minutes for this system and test gear to stabilize.

7.2 ICR-11 Controller Tests

NOTE: it is not necessary to have the ICS system tester connected to the system under test to perform this testing.

7.2.1 Load the "ICR Controller Diagnostic MAINDEC-11-DZIRA" using standard Digital Loading Procedures.

7.2.2 Set switch register to 224 and load address.
NOTE: This starting address includes power fail testing.

7.2.3 Reset the switch register to 1000 and press start.
NOTE: Reference diagnostic write up MAINDEC-11-DZIRA-D for additional information and switch settings if desired.

7.2.4 Check the system map against the system configuration to insure that all files reported on exist, and that all that exist, are reported.

7.2.5 Power fail test each remote filebox on the system, as instructed to do so by the program.

7.2.6 Upon completion of the Power Fail Test, run the diagnostic for time specified for every file on the system. Therefore, a two file system will have a diagnostic run time of doubled. When the prescribed run time has been reached, lower switch 09 to terminate the test and obtain the run summary typeout.

7.2.7 Acceptable error count for the run summary should be 0. Should errors or line errors be encountered, the system shall be considered unacceptable. Repairs shall be initiated and the program rerun for the specified time, until an error free pass is achieved.

7.3 ICR11 Systems Test Program

NOTE: This diagnostic requires the use of a ICS system tester.

7.3.1 Load the ICR systems test program diagnostic AUTOCAT-11-QZIRA using standard Digital Loading Procedures.

7.3.2 Set switch register to 200 load and start.

7.3.3 Enter the octal number of the file to be tested.

7.3.4 Enter the vector address of the same file. Address range 234-777.

7.3.5 Enter (self <cr>). This will automatically run a self test of the system tester to verify that all internal workings of the tester are operative. Should errors be encountered during this run, repairs should be instituted before proceding.

NOTE: System tester cables should be disconnected from the following option modules before attempting to run "self test". If not, false interupts will be generated by the customer's file. IDC-IB, IDC-IC, IDC-IE, and IAD-IA.

7.3.6 Enter (Z <cr>) to clear any previous job buffer entry.

7.3.7 Enter the I/O options mounted within the ICR file to be tested. This file maybe 1 of 12 possible files on the system. (See Figure 2)

7.3.7.1 Should the file configuration include IDA-OA options, (A6330) do not enter them at this time.

NOTE: It is not necessary to remove this option while testing all other options, but do disconnect the EDC input from the IDA-OA option tester. (ref. A-SP-A6330 option test procedure). Sample entry:

#EA005<CR> Enter one A005 in slot address 00 real address 171000. Module connected to system testers analog cable.

#EA007,4<CR> Enter four A007's in slot addresses 02,04, 06, and 10 real addresses 171002 to 171010 modules connected to system testers analog cables.

#EW7411,5<CR> Enter five W7411's in slot addresses 171012 to 171022 modules connected to system testers DC cables 0 thru 4.

#S=30<CR> Set slot address equal to 30.
NOTE: We are not running A6330's at this time, so slot addresses 24 and 26 have been bypassed.

EM6850,4(CR) Enter four M6850's in slot address 30 thru 36. Real addresses 171030 thru 171036.

This completes the loading of the program job buffer to run all modules with the exception of both A6330's.

7.3.8 Type in (L(CR)) to obtain the module entry loaded into the program. This should be checked against your entry to verify that all entries were made correctly.

7.3.9 After entering the modules into the job buffer, type in (K(CR)) The program will respond with K ON. This will enable the program to run non stop.

7.3.10 Type in (R(CR)). This will initiate the test on the file box.

NOTE: Should the program be halted during pass 2, it should not be restarted for 30 minutes, if IAD-IA options are within the filebox configuration. This is to allow for stabilization of flying caps mounted on this module.

7.3.11 Run the diagnostic for a minimum of (1) time specified, or (1) one complete pass. Whichever is longer.

7.3.11.1 The current pass count can be obtained by typing "p" on the teletype.

NOTE: If the ICS file has a maximum load of (16) sixteen analog modules (worst case diagnostic run time), a complete pass will take approximately 1 hour and 40 minutes.

7.3.11.2 Connect all I/O cables from the ICR to the H009 MTC panel (after tests have been run successfully in Acceptance), and have QC inspect the installation.

7.4 ICR 11 Systems Test Program In Conjunction With IDA-OA Option Tester.

7.4.1 Discount all I/O system tester cables from the files that were previously tested.

7.4.2 Reference steps 6.1.3 and 6.1.4 on connecting the IDA-OA option tester if not previously done. Five A6330's can be connected to the option tester at this time, but they will have to be scoped independantly of one another.

NOTE: Don't forget to reconnect the EDC output cable for the IDA-OA option tester.

7.4.3 Enter (Z⟨CR⟩) on the teletype to clear all previously entered jobs.

7.4.4 Enter (K ⟨CR⟩) on the teletype to check what state the "K" command is in. The K command for this test should be in the off mode.

7.4.5 Enter the slot address location for all the IDA-OA options within the file.
NOTE: Only (5) five IDA-OA options can be connected to the tester. If others are present, they can be tested upon the completion of this test.

Example of loading technique to be used for IDA-OA options shown in figure 2.

@ S = 24 ⟨cr⟩ Set slot address equal to 24
@ E A6330, 2 ⟨cr⟩ E. A6330's in slot addresses 24 and 26 rec. addresses 171024 and 171026, Jobs 0 and 1 respectively.

This completes the loading of both A6330's shown in figure 2.

7.4.6 Adjust all settings for the scope, and switch the option tester to the first option (card/cable output) Job 0. (reference A6330 option test procedure A-SP-A6330-0-5).

7.4.7 Type in RJO⟨cr⟩. This will initiate pass 1 testing on the first IDA-OA option or job 0 at slot address 171024. (see step 7.4.5) ramps will be outputed to the option for scope measurements.

7.4.8 Compare the scope waveform against the tolerances indicated within the option test procedure A-SP-A6330-0-5. If the option is found to be within tolerence, proceed to the next step. If not, repair, adjust, or replace the option, and retest until acceptable.

7.4.8.1 To adjust the A6330, or IDA-OA Option, proceed as follows: (Ref. figure 3)

A. First measure the cards Reference Voltage between "TP2" and "TPG". It should be +2 volts ± 2mv. If out of spec, use the "+2 v adj." pot to adjust it within tolerence.

B. Set the thumbwheel switch to the card under test.

C. Set the thumbwheel switch to channel 0 or the first voltage output.

D. Adjust pot "D/A 0" gain adjust for channel 0. The output on the scope should be adjusted within the ±20mv tolerence.

E. Set the thumbwheel switch to channel 2 or the second voltage output.

F. Repeat step D, but use pot marked "D/A 1" gain adjust.

G. Repeat steps C thru F for remaining two voltage channels 2 and 3 (thumbwheel settings 4 and 6 respectively).

H. Reset thumbwheel switch to channel 1. This is the first current output channel.

I. Adjust the current offset of channel 1 as close as possible ground by using pot. "off 0"

J. Adjust the current gain of channel 1 to fall within the required ± 20 mv tolerence.

K. Reset the thumbwheel switch to channel 3 or the second current output.

L. Repeat steps I thru J and repeat these steps for the remaining current outputs, channels 5 and 7.

7.4.9 Type "Control C" to terminate the test.

7.4.10 If other IDA-0A options have been entered, type in the next job to be run. For example, Job 1 would be entered next for the Figure 2 Configuration. Repeat steps 7.4.7 thru 7.4.9 until all jobs have been tested.

7.4.11 Turn "K" command on by typing "K" on the terminal.

7.4.12 Enter R <cr> and run all IDA-0A options entered in step 7.4.5 for time specified. With the "K" command on, pass 2 will only be run during this test. It is not necessary to scope the outputs for this test.

7.4.13 Type "Control C" to terminate the test.

7.4.14 Repeat steps 7.4.6 thru 7.4.10. Should any of the options fail, repair, and repeat all tests.

7.4.15 If there are more than (5) five IDA-0A options within this file, it will be necessary to repeat steps 7.4.5 thru 7.4.14 to test the remaining.

7.5 Repeat all tests 7.3. thru 7.4.15 for all other files on the systems configuration.

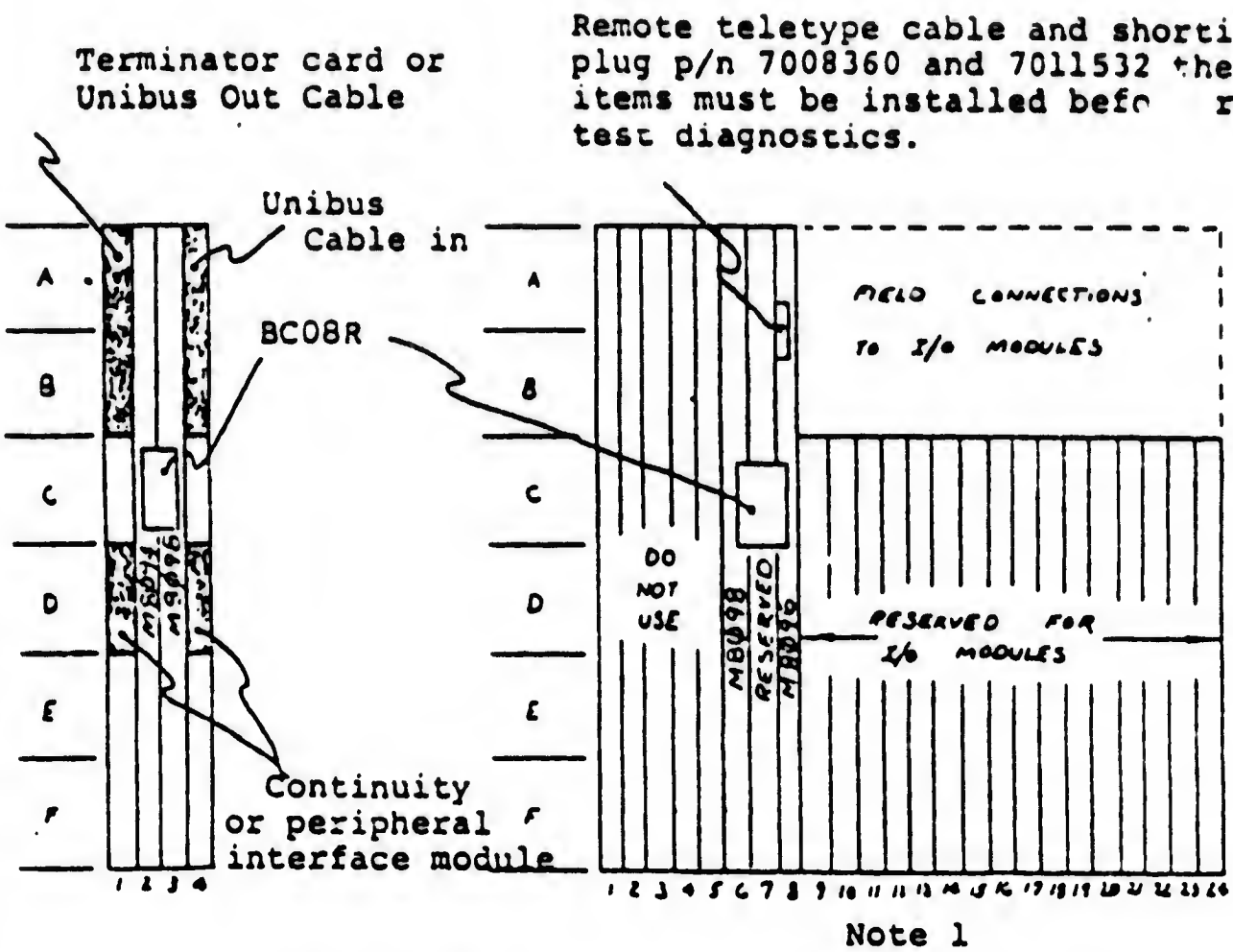
7.6 ICR11 Field Test Program

NOTE: This diagnostic requires the use of a Field UDC/ ICS Tester.

7.6.1 Reference specification A-SP-ICR11-M-5 for indepth explanation.

FIGURE 1

CONTROL AND INTERFACE MODULE ASSIGNMENTS AND CABLE LOCATIONS:



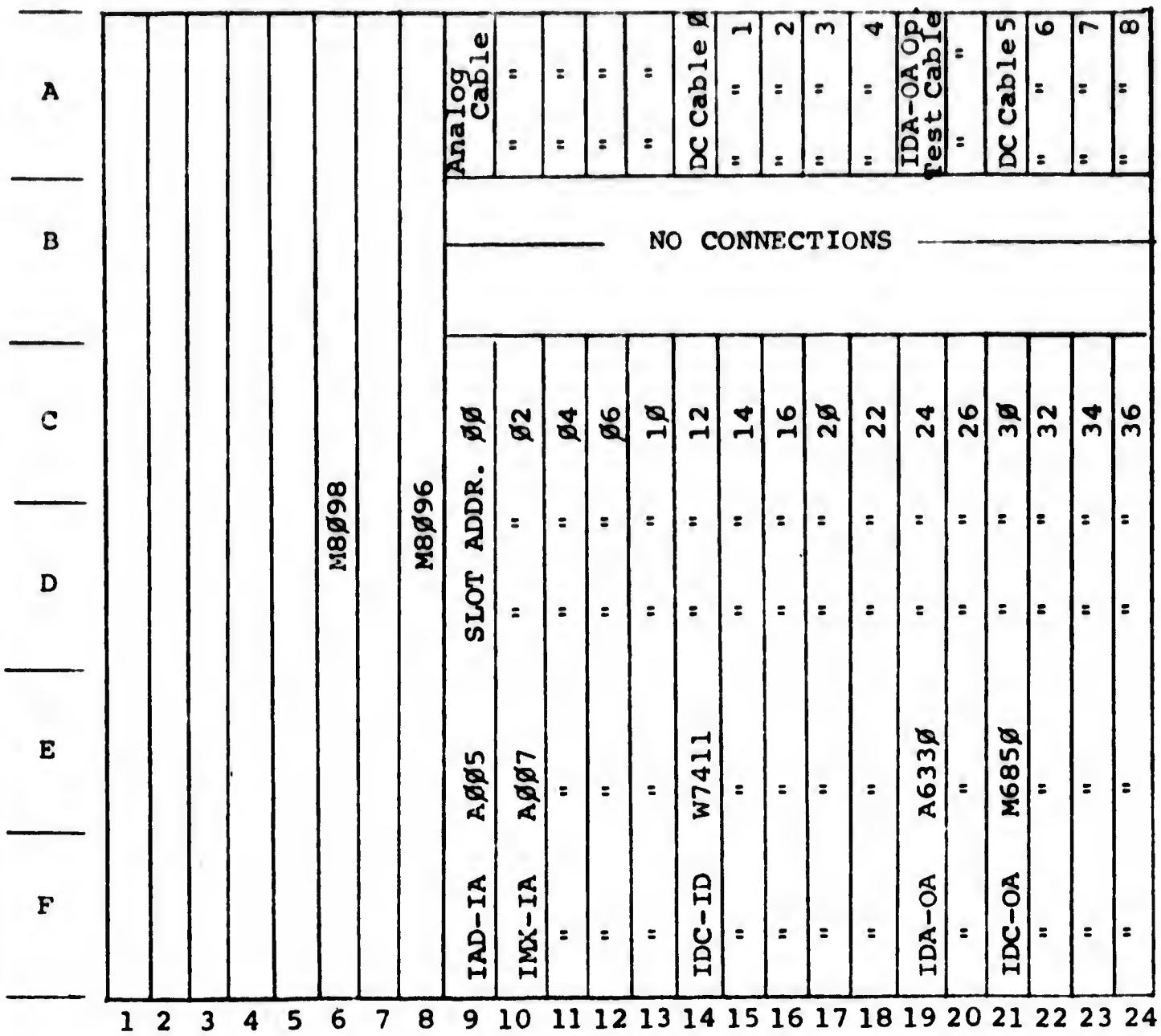
Note 1

DD 11B or availible SPC slots (Front View)

ICR File Backplane (Front View)

EXAMPLE OF TYPICAL FILEBOX CONFIGURATION

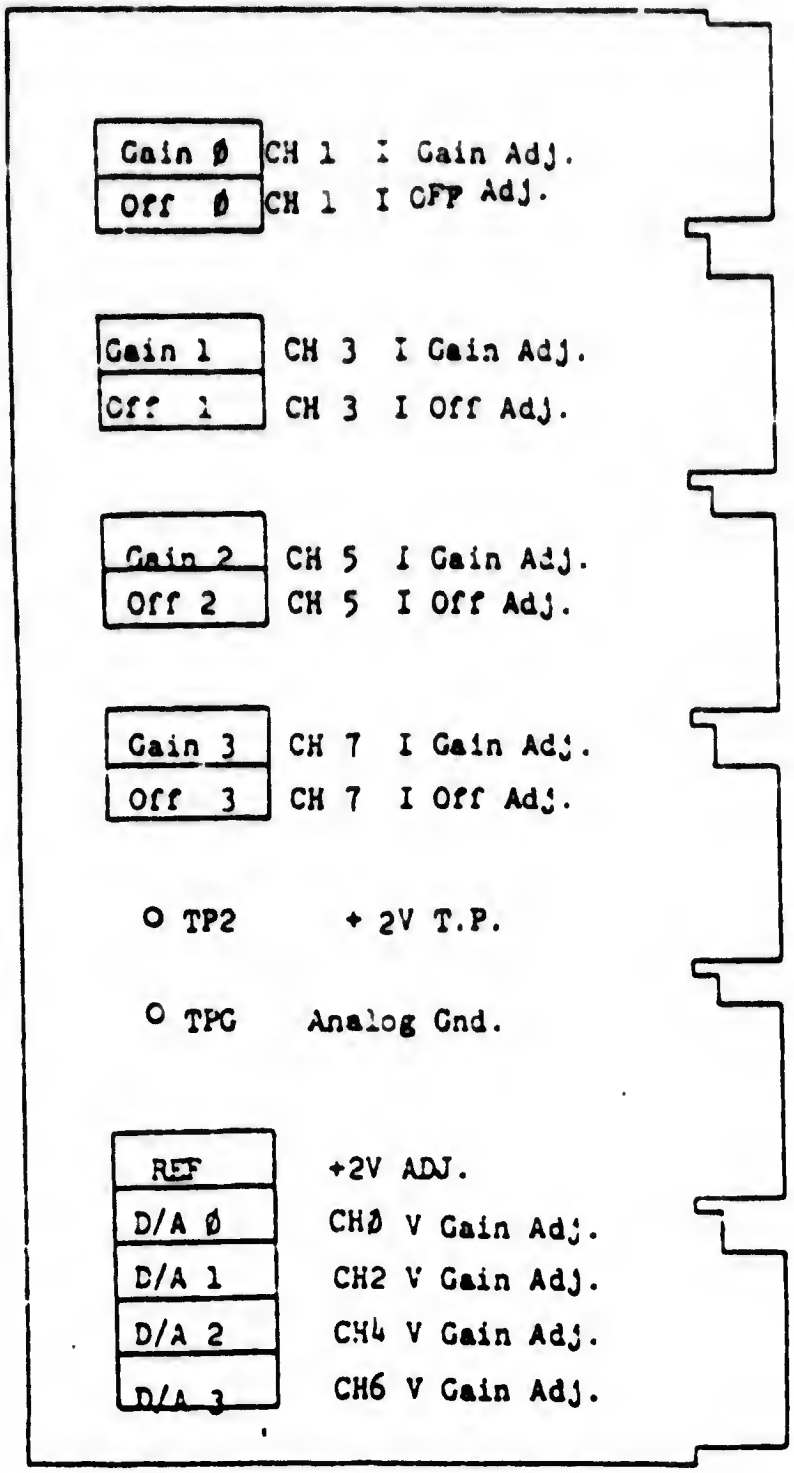
NOTE: A6330 will be tested upon completion of this test.



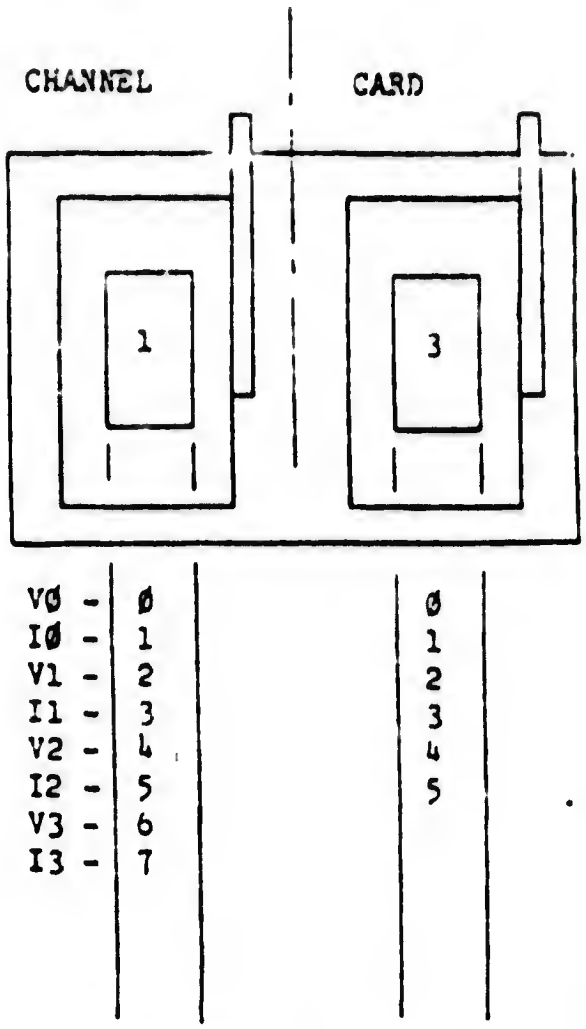
Physical Slot Location
FIGURE 2

NOTE: For module address locations other than filebox Ø reference 9.1 of the diagnostic write-up autocat-11-QZIRB.

Operator entry on teletype for configuration shown in fig. 2.



A6330 DAC Module
Top View



THUMBWHEEL SWITCH
FRONT VIEW

FIGURE 3

TABLE 1

FILE BOX - MODULE PRIORITY TABLE

PRIORITY SEQUENCE	MODULE	OPTION	COMMENTS
1	A005	IAD-IA	
2	A007	IMX-IA	7 MAX
3	A005	IAD-IA	
4	A007	IMX-IA	7 MAX
5	A907	ISH-IA	
6	W7410	IDC-IA	
7	W7411	IAC-IA	H912, + BC40J
8	W7411	IDC-ID	
9	W7440	IDC-IC	
10	W7430	IDC-IB	
11	W7431	IAC-IB	H912, + BC40J
12	W7431	IDC-IE	
13	A6330	IDA-OA	11 MAX
14	M6870	IDC-OB	
15	M6870	IAC-OB	H912, + BC40J
16	M6850	IDC-OA	
17	M6850	IAC-OA	H912, +BC40J
18	M8030	IRL-OA	
19	M8050	IRL-OB	

TABLE 2

A005 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W108	OUT	INTERRUPT MODE
W111	IN	ICS-11

A007 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W21	OUT	SELECT MUX # 1
W22	OUT	SELECT MUX # 2
W23	OUT	SELECT MUX # 3
W24	OUT	SELECT MUX # 4
W25	OUT	SELECT MUX # 5
W26	OUT	SELECT MUX # 6
W27	OUT	SELECT MUX # 7

W7430 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W58	IN	INTERRUPT MODE
W59	OUT	ICS-11

W7431 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W 9	OUT	INTERRUPT MODE
W10	IN	JCS-11

TABLE 3

W7440 STANDARD JUMPER CONFIGURATION

JUMPER	IN/OUT	FUNCTION
W 2	IN	ICS-11
W16	OUT	INTERRUPT MODE

M8094 STANDARD JUMPER CONFIGURATION

File No.	ICSR/ICAR JUMPERS									
	A12 W22	A11 W21	A10 W20	A9 W19	A8 W18	A7 W17	A6 W16	A5 W15	A4 W14	A3 W13
00	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT
01	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	IN
02	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	IN	OUT
03	OUT	IN	IN	OUT	OUT	OUT	OUT	OUT	IN	IN
04	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	OUT	OUT
05	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	OUT	IN
06	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	IN	OUT
07	OUT	IN	IN	OUT	OUT	OUT	OUT	IN	IN	IN
08	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	OUT	OUT
09	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	OUT	IN
10	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	IN	OUT
11	OUT	IN	IN	OUT	OUT	OUT	IN	OUT	IN	IN

Jumper OUT = Logic "1"
Jumper IN = Logic "0"

TABLE 4

M8094 FILE JUMPERS

File No.	F3 W12	F2 W11	F1 W10	F0 W9
0	IN	IN	IN	IN
1	IN	IN	IN	OUT
2	IN	IN	OUT	IN
3	IN	IN	OUT	OUT
4	IN	OUT	IN	IN
5	IN	OUT	IN	OUT
6	IN	OUT	OUT	IN
7	IN	OUT	OUT	OUT
8	OUT	IN	IN	IN
9	OUT	IN	IN	OUT
10	OUT	IN	OUT	IN
11	OUT	IN	OUT	OUT

Jumper OUT = Logical "1"
Jumper IN = Logical "0"

M8094 VECTOR JUMPERS

File No.	Vector Address	VECTOR ADDRESS JUMPERS V8 W7	V7 W6	V6 W5	V5 W4	V4 W3	V3 W2	V2 W1
00*	234	IN	OUT	IN	IN	OUT	OUT	OUT
01*	300	IN	OUT	OUT	IN	IN	IN	IN
02	304	IN	OUT	OUT	IN	IN	IN	OUT
03	310	IN	OUT	OUT	IN	IN	OUT	IN
04	314	IN	OUT	OUT	IN	IN	OUT	OUT
05	320	IN	OUT	OUT	IN	OUT	IN	IN
06	324	IN	OUT	OUT	IN	OUT	IN	OUT
07	330	IN	OUT	OUT	IN	OUT	OUT	IN
08	334	IN	OUT	OUT	IN	OUT	OUT	OUT
09	340	IN	OUT	OUT	OUT	IN	IN	IN
10	344	IN	OUT	OUT	OUT	IN	IN	OUT
11	350	IN	OUT	OUT	OUT	IN	OUT	IN

Jumper OUT = Logic "1" Jumper IN = Logic "0"

TABLE 5

M8096 STANDARD JUMPER CONFIGURATION

#of Input Modules	W7	W6	W5	W4	W3
1	out	in	in	in	out
2	out	in	in	out	in
3	out	in	in	out	out
4	out	in	out	in	in
5	out	in	out	in	out
6	o'	in	out	out	in
8	o'	out	in	in	in
9	out	out	in	in	out
10	out	out	in	out	in
11	out	out	in	out	out
12	out	out	out	in	in
13	out	out	out	in	out
14	out	out	out	out	in
15	out	out	out	out	out
16	in	x	x	x	x

x = Do not care

Jumpers minimize polling time for input modules. The selected jumpers short cycle the poll counter after the last module address has been selected.

Installation of jumper W8 causes an I/O signal to be sent to all I/O modules if serial link is lost for more than 20 minutes. (must not be used by FA&T)

TABLE 6

M8098 STANDARD JUMPER CONFIGURATION

Mode Selection	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1
Master	in	in	in	out	out	out	out	in	out	out
Slave	out	out	out	in	in	in	in	out	in	in

Valid for etch Rev. "A" only.

Mode Selection	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1
Master	out	out	out	in	in	in	in	out	out	out
Slave	in	in	in	out	out	out	out	in	in	in

Valid for etch Rev. "B or higher.

M8098 SWITCH SETTING (E80)

Switch	Mode Master	Slave	Function
S1-1	on	on	ADR 0
S1-2	on	on	ADR 1
S1-3	on	on	ADR 2
S1-4	on	on	ADR 3
S1-5	on	on	ADR 4
S1-6	on	on	ADR 5
S1-7	off	on	Master/Slave Select
S1-8	off	off	Broadcast

TABLE 7

AUTOCAT DIAGNOSTIC "PATCHES"

ADDRESS TO BE CHANGED		
ICS11 AUTOCAT-11-QZICA	ICR11 AUTOCAT-11-QZICA	NEW CONTENTS
033210	033722	100020
033230	033312	100420
033250	033332	100066
033270	033352	100100
033310	033372	100500
033330	033412	100466
033346	033430	100000
033350	033432	101001
033370	033452	101004
033410	033472	101066
033530	033612	101466
033550	033632	101404
033566	033650	100000
033570	033652	101401

TABLE 8

CALIBRATION TABLE FOR A005-YA

EDC Output			Channel		Average		Tolerance (LSB)	
Bipolar	Unipolar	Gain	A005-YA	A007	Bipolar	Unipolar	Bipolar	Unipolar
+0V	+0V	1000	10	*	0000	0000	±4	±6
+0V	+0V	500	10		0000	0000	±2	±3
+0V	+0V	250	10		0000	0000	±2	±3
+0V	+0V	125	10		0000	0000	±2	±3
+5MV	+5MV	1000	10	*	2000	4000	±5	±8
-5MV	----	1000	10		6000	----	±5	--
+9MV	+9MV	1000	10		3463	7146	±5	±10
-9MV	----	1000	10		4315	----	±5	--
+10MV	+10MV	500	10		2000	4000	±3	±5
+36MV	+36MV	250	10		3463	7146	±3	±6
+40MV	+40MV	125	10		2000	4000	±3	±5
+0V	+0V	50	10		0000	0000	±2	±3
+0V	+0V	12.5	10		0000	0000	±2	±3
+0V	+0V	2.5	10		0000	0000	±2	±3
+0V	+0V	1	10		0000	0000	±2	±3
+180MV	+180MV	50	10		3463	7146	±2	±4
+400MV	+400MV	12.5	10		2000	4000	±2	±4
+3.6V	+3.6V	2.5	10		3463	7146	±3	±5
+5V	+5V	1	10		2000	4000	±2	±4
+9.9609V	+9.9609V	1	10	*	3770	7760	±3	±5
-9.9804V		1	10	*	4007	----	±3	--
-5.0V		1	10		6000	----	±2	--

* Channel to be used for each A007

A007 #	1	2	3	4	5	6	7
CHANNEL	21	42	63	84	105	126	147


A6170

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 8/7/80

TITLE DPM23 DISTRIBUTED I/O SUBSYSTEM

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Updated and revised	MA-A0000 ML010				

ENG	APPD	SIZE	CODE	NUMBER	REV
BILL WHITBY	STU ESTES	A	SP	MAA6170-0-0	A

DPM23 DISTRIBUTED I/O SUBSYSTEM

1.0 INTRODUCTION .

The DPM23 is a user programmable subsystem which is based on the KDF11-AA (11/23 CPU) and interfaced to the DEC DATAWAY. It is supported under RSX11S, supports FORTRAN and MACRO, and uses DPM50 Phase 2 communications software. User programs and diagnostics are downloaded from a DPM HOST COMPUTER over the DATAWAY.

This procedure defines minimum test criteria for the base DPM23. For options added to the base, reference other appropriate mast procedures.

The base DPM23 consists of:

BA11-NC/ND	9 slot chassis and power supply
KDF11-AA	CPU with memory management
MSV11-DD	64kb mos memory
ISV11-B	DEC DATAWAY interface board set

2.0 REFERENCE DOCUMENTATION

2.1 MANUALS:

2.1.1 MICROCOMPUTER PROCESSOR HANDBOOK:	EB-15836-18/79
2.1.2 MICROCOMPUTER INTERFACES HANDBOOK:	EB-17723-20/80
2.1.3 MSV11-D,-E USERS MANUAL:	EK-MSV1D-OP-???
2.1.4 PROCESS I/O SUBSYSTEM USERS GUIDE:	EK-PIOS-UG-???
2.1.5 DPM23 USERS GUIDE:	EK-DPM23-UG-???
2.1.6 KDF11-AA USERS GUIDE:	EK-KDF11-UG-???
2.1.7 BA11-N TECHNICAL MANUAL:	EK-BA11N-TM-???

2.2 PRINTS AND SCHEMATICS:

2.2.1 DPM23 PRINTSET:	MP001058
2.2.2 DLV11-F PRINTSET:	MP000461

3.0 REQUIRED TEST EQUIPMENT:

3.1 HARDWARE AND MEDIA:

3.1.1 Valid DPM HOST SYSTEM configuration.
3.1.2 RSX11-M on appropriate host media.
3.1.3 Attenuation panel.
3.1.4 HEWLETT PACKARD DVM or equivalent accurate to .01V @ 15V.
3.1.5 Serial line unit IE. DLV11-F and Terminal for LSI error information output (LOCAL MODE).

4.0 REQUIRED DIAGNOSTIC PROGRAMS:

4.1 DPM REMOTE DIAGNOSTICS KIT #ZP125-RD

	NAME	DESCRIPTION	MODE
4.1.1	DZKCI	Remote terminal tester	Remote
4.1.2	DZKCH	Serial bus exerciser	Remote
4.1.3	CZKMP	Task Handler	N/A
4.1.4	DVDVC	DLV11-F test	Local
4.1.5	CZQMC	0-124k memory exerciser	Local
4.1.6	DVPCA	Pcs test	Local
4.1.7	CJKDA	F-11 MMU test	Local
4.1.8	CJKDB	F-11 CPU test	Local
4.1.9	CJKDC	KEF11-AA diag 1*	Local
4.1.10	CJKDD	KEF11-AA diag 2*	Local

*=OPTIONAL

5.0 SPECIAL INSTRUCTIONS

5.1.1 RSX11-M must be running in the host system with DPM REMOTE DIAGNOSTICS KIT #ZP125-RD.

5.1.2 A serial line interface (IE. DLV11-F,DLV11-J) and terminal will be required to run diagnostics in LOCAL MODE at the DPM23 subsystem. NOTE: These items are used for test only and are not shipped unless specifically ordered with system.

5.1.3 The M8080 is always the last item on the bus with the exceptions that the M8084 always occupies slot 9, and that the optional BDV11-AA(M8012) always plugs into slot 8.

5.1.4 At this writing only the following options are supported on the DPM23.

A.	MSV11-DD	32K WORDS MOS MEMORY
B.	BDV11-AA	TERMINATOR/BOOT MODULE
C.	DLV11-E	ASYNCHRONOUS LINE UNIT
D.	DLV11-J	FOUR ASYNCHRONOUS SERIAL INTERFACES
E.	DLV11-KA	20MA CURRENT LOOP OPTION
F.	DZV11-A	ASYNCHRONOUS MULTIPLEXER
G.	IBV11-B	INSTRUMENT BUS INTERFACE AND CABLE
H.	IPV11	Q BUS IOCM
I.	LPV11-PA/PD	LINE PRINTER OPTIONS
J.	RXV11-BA/BD	FLOPPY DISK OPTIONS
K.	RXV21-BA/BD	DOUBLE DENSITY FLOPPY DISK OPTIONS
L.	BA11-NE/NF	EXPANDER BOX

5.1.5 In order to run DCF11-AA diagnostic (CJKDB), LTC (LINE TIME CLOCK) interrupts must be disabled, to accomplish this jumper W4 must be installed on the KDF11-AA CPU module prior to testing. If a BDV11-AA (M8012) module has been added to the DPM23 system switchpack E21 #5 may be turned on instead. In either case this procedure must be reversed prior to running D BUS I/O module diagnostic VPCAEO. System must ship with LTC interrupts enabled.

6.0 INSTALLATION AND TEST SETUP INSTRUCTIONS

6.1 UNPACKING AND INSPECTION:

6.1.1 Save all packing material for equipment to be shipped that is not cab mounted.

6.2 MODULE CONFIGURATION SETUPS FOR DPM23

6.2.1 KDF11-AA (M8186) LSI 11/23 CPU MODULE

JUMPER DESIGNATION	JUMPER STATE
W1	IN
W2	AS RECEIVED
W3	AS RECEIVED
W4*	OUT
W5	OUT
W6	OUT
W7	IN
W8 THRU W15	DON'T CARE
W16	IN
W17	IN
W18	IN

*=Note: See special instruction at 5.1.5

Reference FIGURE 2 for jumper locations.

6.2.2 MSV11-DD (M8044-D?) FIRST 32K

S1 SWITCHPACK	SWITCH STATE
SW1	ON
SW2	ON
SW3	ON
SW4	ON
W2	IN
W3	IN
PIN 1 TO 3	IN
PIN 5 TO 7	IN
PIN 10 TO 14	IN
PIN 15 TO 16	IN

Reference FIGURE 4 for switch and jumper locations.

6.2.3 DLV11-F (M8028) SERIAL LINE UNIT

JUMPER DESIGNATION	JUMPER STATE
T0	OUT
T1	IN
T2	OUT
T3	IN
R0	OUT
R1	IN
R2	OUT
R3	IN

The DLV11-F is default jumpered for console use, but the above baud rate jumpers must be reconfigured from 110 baud operation to 300 baud.

The DLV11-F is not a standard part of the DPM23 system, but is a frequent option, and is needed in FA&T for diagnostic testing in LOCAL MODE. See FIGURE 5 for jumper locations.

6.2.4 ISV11-B (M8080,M8084) DEC DATAWAY INTERFACE

FACTORY CONFIGURED:

CSR ADDRESS	160140 160142 160144
VECTOR ADDRESS	300 304

JUMPERS	STATE	LOCATION
W1 THRU W6	OUT	M8080
W7 THRU W10	IN	M8080
W11 THRU W16	OUT	M8080
W17 THRU W20	IN	M8080
W21 THRU W23	OUT	M8080
W1,W3,W5,W7,W9	IN	M8084
W2,W4,W6,W8,W10	OUT	M8084

NOTE: If DLV11-J is installed in DPM23 system its default vector address of 300 must be reconfigured because of its conflict with the ISV11-B.

Reference FIGURES 7.1 and 7.2 for jumper locations.

6.3 CABL[illegible]G OF THE DPM23

6.3.1 Cabling of the DPM23 consists of a serial bus cable (70-15928-03) coming from the M8084 board of the ISV11-B, which interconnects with the DEC DATAWAY cable (70-14152), which in turn is run through an attenuation panel to simulate cable length, finally exiting the attenuation panel and connecting to the HOST CPU'S ISB11. Reference FIGURE 1.

NOTE: The attenuation panel is only used for test and is not shipped with the system.

7.0 POWER CHECKS

7.1 +5VDC ±250MV
+12VDC ±600MV

The +5VDC and +12VDC regulated voltages can be measured at J7 of the backplane or, preferably at the tip jacks on the M8012 (BDV11-AA) module (if it has been added to the system). The pins of J7 are numbered, and color coded. +12VDC and +5VDC are assigned the following pins and colors.

+12VDC----------PIN 2, PURPLE WIRE
+12VDC GROUND----------PIN 3, BLACK WIRE
+5VDC----------PIN 5, RED WIRE
+5VDC GROUND----------PIN 4, BLACK WIRE

The tip jacks on the M8012 module are color coded and labeled as follows:

+12VDC----------J3, PURPLE
+5VDC----------J2, RED
GROUND----------J1, BLACK

If adjustment becomes necessary, remove the two power supply mounting screws to tilt the power supply forward exposing the adjustment potentiometers R1 for +12VDC, and R22 for +5VDC. Reference FIGURES 3.1 and 3.2 for locations.

8.0 DIAGNOSTIC TEST PROCEDURE

The host processor whether it be an 11/70 or 11/34 along with its ISB11'S must be fully checked out according to MAST prior to connecting a DPM23 to the DATAWAY.

8.1 DPM23 HOST SYSTEM BOOTING PROCEDURE

8.1.1 Obtain a disk pack for the appropriate host media which has the RSX11-M host package #AP-F152A-MC and install it into DRIVE #0. Load DRIVE #0 and insure that "WRITE PROTECT" is off.

8.1.2 When DRIVE #0 is ready and "ON LINE" (heads loaded) BOOT the drive.

8.1.3 When the program asks for the date and time, you may either enter the information or default it by typing a carriage return. An example would be 08:30 04-JUN-80.

8.1.4 The program will continue setting up parameters and will ask: "Do you want to load IPG diagnostics from magtape [Y/N]:". Type in a carriage return which will default your answer to a NO condition.

8.1.5 The program will now output:
>@ <EOF> (This signifies end of file and parameters are now set) and waits for you to key in a command.

8.1.6 Type in:
Set /UIC=[200,270] (This may not be necessary if the UIC is already at 200,270.)

8.2 RUN THE ERROR REPORT TASK IN ORDER TO CLEAR OUT THE ERROR LOG

```
8.2.1 >RUN ISBRPT--------------------------TYPE:<RUN ISBRPT>
      ISBRPT-DEC DATAWAY ERROR REPORT TASK
      >
      PRINT SUMMARY [Y OR N]?N-------------TYPE:<N>
      PRINT ENTIRE FILE [Y OR N]?N---------TYPE:<N>
      DELETE ERROR FILE [Y OR N]?Y---------TYPE:<Y>
      ISBRPT...OPERATION COMPLETE
      TASK "ISBRPT" TERMINATED
      TASK EXIT WITH OUTSTANDING I/O
      PC=125130
      PS=170000
      R0=120720
      R1=125576
      R2=125650
      R3=000000
      R4=143470
      R5=000000
      SP=120476
```

8.2.2 Type:CTRL C to terminate ISBRPT task and receive back MCR> prompt.

8.3 RUN THE DEC DATAWAY DIAGNOSTIC EXERCISER.

```
8.3.1 >RUN DZKCH---------------------------TYPE:<RUN DZKCH>
      DCP-A>STA----------------------------TYPE:<STA>

      #UNITS (D)?1-------------------------TYPE:<1>
      ENTER CONTROLLER NUMBER:(O)0?0-------TYPE:<0>
      ENTER TERMINALS ON THAT CONTROLLER:
      (O)1?1-------------------------------TYPE:<1>
      NUMBER OF ENTERED TERMINALS=1

      UNIT**CONTROLLER**LOGICAL SB**LUN**
       001       000          001       011

      TOTAL ACTIVE PASSES = 21,ACTIVE TERMINALS=1, TIME=8:33

      TOTAL ACTIVE PASSES = 41,ACTIVE TERMINALS=1, TIME=8:34
```

8.3.2 After required run time has elapsed terminate running of diagnostic by typing CTRL C.

```
TASK "TTO" TERMINATED
TASK EXIT WITH OUTSTANDING I/O
PC=046000
PS=170000
R0=000002
R1=000000
R2=000000
R3=000000
R4=000003
R5=000001
SP=001246
```

8.4 After DZKCH has run,The error log must be checked for errors that may have occured during running.

```
8.4.1 >RUN ISBRPT-------------------------TYPE:<RUN ISBRPT>
      ISBRPT-DECDATAWAY ERROR REPORT TASK
      >
      PRINT SUMMARY[Y OR N]?Y-------------TYPE:<Y>
      PRINT ENTIRE FILE [Y OR N]?N--------TYPE:<N>
      OUTPUT TO LINE PRINTER [Y OR N]?N---TYPE:<N>
      WANT ONE CONTROLLER [Y OR N]?N------TYPE:<N>
      DELETE ERROR FILE [Y OR N]?N--------TYPE:<N>
      ISBRPT...ERROR FILE IS EMPTY
      ISBRPT...OPERATION COMPLETE
```

8.4.2 Type: CTRL C to terminate ISBRPT task and receive back MCR> prompt.

8.4.3 Error reporting can be in the form of hard errors, typed out immediately, or soft errors;(Errors that are logged by the error logger). No errors are allowed.

8.5 RUN ROM RESIDENT TESTS OF ISV11-B

8.5.1 MCR>RUN CZKCIB----------TYPE:<RUN CZKCIB>
>
DCP-A>STA----------TYPE:<STA>

UNITS (D) ? 1----------TYPE:<1>

UNIT 1
ENTER CONTROLLER NUMBER:(0)0?0------TYPE:<0>
ENTER TERMINALS ON THAT CONTROLLER:
(D)1?1----------TYPE:<1>

SELECTED SERIAL LINE PORTS

UNIT**CONTROLLER**LOGICAL SB**LUN**TYPE
1 0 001 9 DPM50-PORT 0

START OF TESTING

END OF PASS 0, TIME = 9:29

END OF PASS 1, TIME = 9:31

8.5.2 After required run time has elapsed terminate running of the diagnostic by typing CTRL C.

8.6 LOAD DIAGNOSTIC MONITOR CZKMPB

8.6.1 >RUN CZKMPB----------TYPE:<RUN CZKMPB>
>
CZKMPB VERSION 2.2
SELECT MODE: LOCAL, HOST, AUTO-MAP, COMMUNICATION OR EXIT
(L,H,A,C,E)L----------TYPE:<L>
ENTER NUMBER OF TERMINALS [D]=1-----TYPE:<1>
ENTER CONTROLLER NUMBER [0]=0-------TYPE:<0>
ENTER TERMINAL NUMBERS [0]=1--------TYPE:<1>
NUMBER OF ENTERED TERMINALS = 1
UNIT**CONTROLLER**LOGICAL SB**
1 0 1

At this point the console terminal at the DPM23 subsystem comes on line and is used to ask for and run subsystem diagnostics.

8.7 RUN 11/23 CPU AND MEMORY DIAGNOSTICS ON DPM23

See Figure 6 for explanation of monitor interaction inputs and outputs at local DPM23 terminal.

8.7.1 >JKDAC0----------TYPE:<JKDAC0>
157776
@200G----------TYPE:<200G>
CJKDAC0 KTF11-AA MMU DIAG.
SWR=000000 NEW=CR----------TYPE:<CR>

END PASS# 1 ;TOTAL ERRORS SINCE LAST START AT 200 0

8.7.2 After required run time has elapsed, terminate running of the diagnostic at the DPM23 console terminal by depressing the break key.

8.7.3 @760144/000000 2----------TYPE:<760144/>
TYPE:<2>
>JKDBC0----------TYPE:<JKDBC0>
157776
@200G----------TYPE:<200G>
CJKDBC0 DCF11-AA CPU DIAGNOSTIC
END PASS# 1
END PASS# 15

NOTE: LTC interrupts must be disabled to run diagnostic JKDBC0. See special instruction at 5.1.5.

8.7.4 After required run time has elapsed,terminate running the diagnostic at the DPM23 console terminal by depressing the break key.

```
8.7.5 @760144/000000 2----------------------TYPE:<760144/>
                                             TYPE:<2>
      >ZQMCGO--------------------------------TYPE:<ZQMCGO>
      157776
      @200G----------------------------------TYPE:<200G>
      SWR=000000 NEW= CR---------------------TYPE:<CR>

      KT11(MEMORY MANAGEMENT)AVAILABLE

      MEMORY MAP
      FROM 000000 TO 757777 (WITH 4 MSV11-D INSTALLED)
      NO PARITY REGISTERS FOUND
      PROGRAM RELOCATED TO 720000
      PROGRAM RELOCATED TO 000000
      END PASS# 1
```

Above will be received when 4 MSV11-D modules are installed, typeouts will vary with lesser amounts of memory. No relocation will occur when only 1 MSV11-D is installed.

8.7.6 *NOTE THE following two tests are to be run if the optional KEF11 chip is installed.

```
8.7.7 @760144/000000 2----------------------TYPE:<760144/>
                                             TYPE:<2>
      >JKDCB0--------------------------------TYPE:<JKDCB0>
      157776
      @200G----------------------------------TYPE:<200G>
      CJKDCB, KEF11-A FP DIAGNOSTIC PART 1

      SWR = 000000  NEW=CR-------------------TYPE:<CR>

      END PASS #    1
      END PASS #    2
```

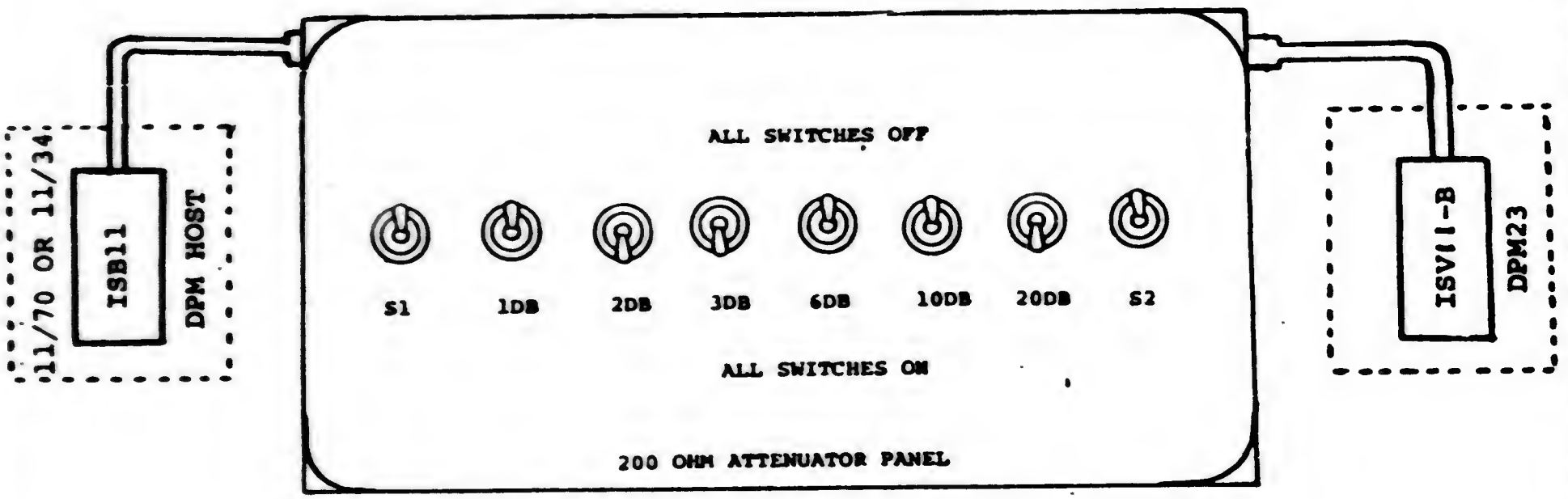
8.7.8 After required run time has elapsed, terminate running of the diagnostic at the DPM23 console terminal by depressing the break key.

```
8.7.9 @760144/000000 2--------------------TYPE:<760144/>
                                           TYPE:<2>
      >JKDDB0-----------------------------TYPE:<JKDDB0>
      157776
      @200G-------------------------------TYPE:<200G>
      CJKDDB KEF11-A DIAGNOSTIC PART 2

      SWR = 000000  NEW =CR---------------TYPE:<CR>

      END PASS #    1
      END PASS #    2
```

8.7.10 After required run time has elapsed, terminate running of the diagnostic at the DPM23 console terminal by depressing the break key.

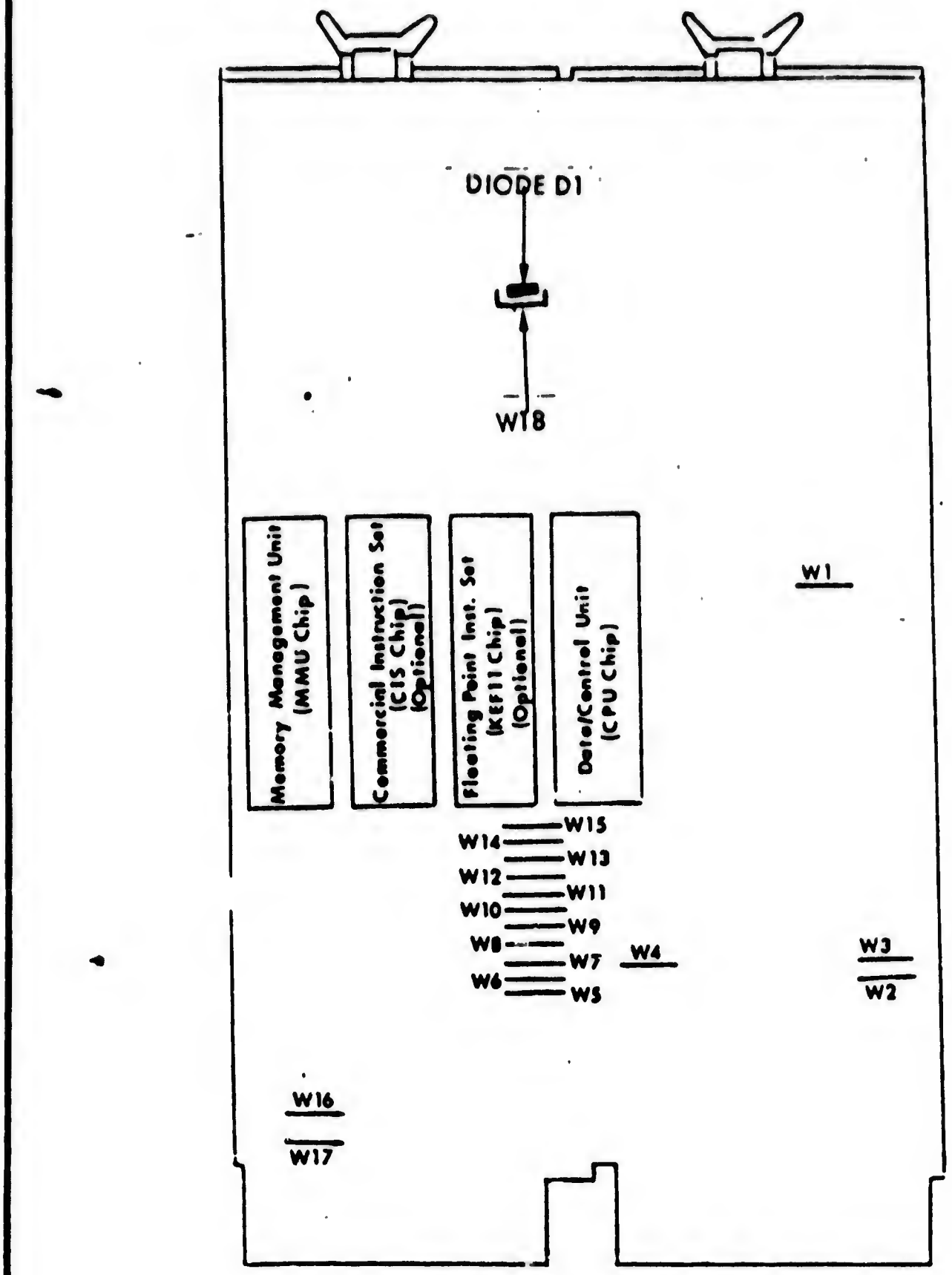
8.7.11 Load and run diagnostics for any additional LSI option modules installed, using same method used to run the CPU tests.

8.7.12 After all LSI modules have been run, if any D BUS I/O modules exist within the DPM23 subsystem, load diagnostic VPCAE0 and follow procedure POO-00COA-00-0000WM-06-8055. Reference section 4.0 DIAGNOSTIC TESTING.



# OF TERMINALS	ATTENUATOR SETTING	
1 TO 9	25DB	(SHOWN ABOVE)
10 TO 19	24DB	
20 TO 29	23DB	
30 TO 39	22DB	
40 TO 49	21DB	
50 TO 59	20DB	
60 TO 63	19DB	

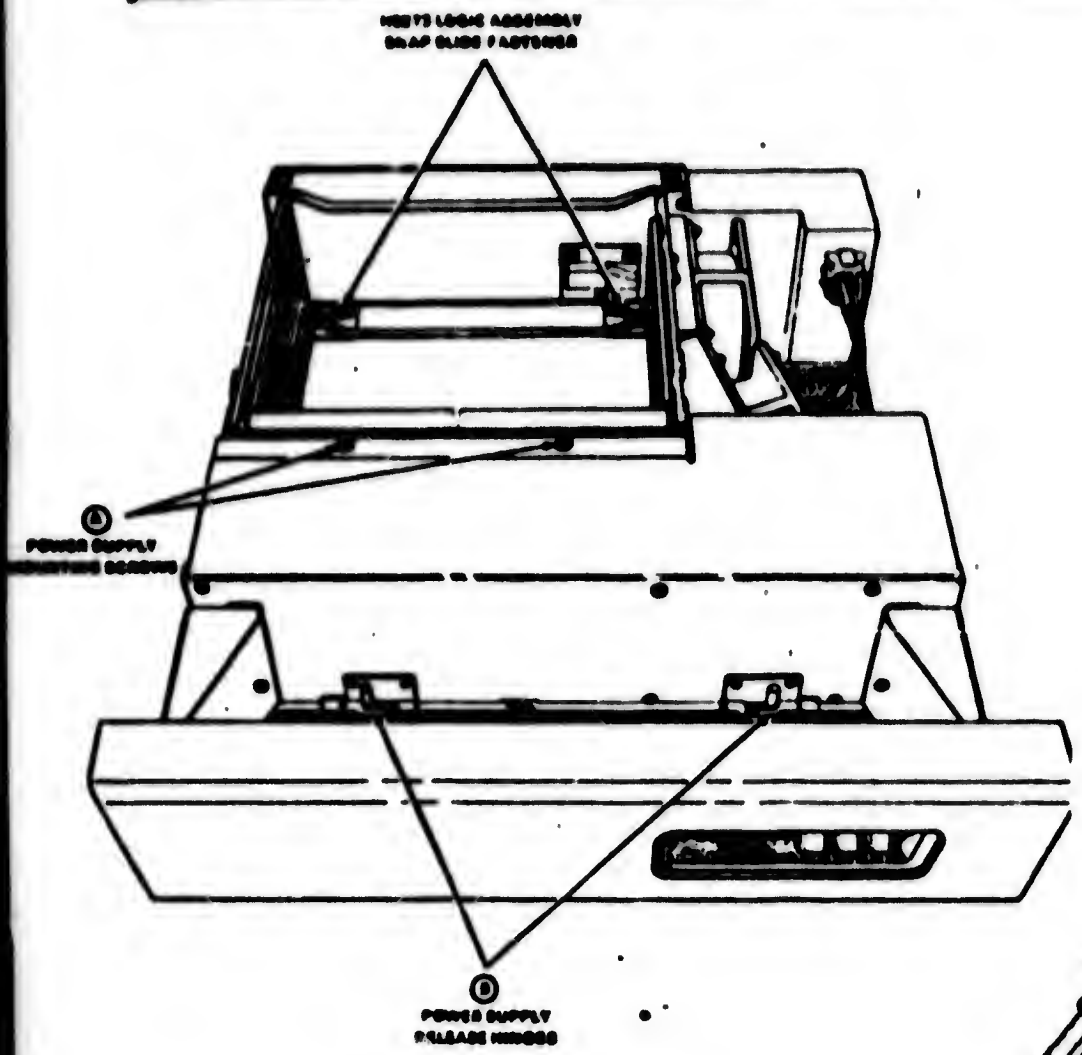
FIGURE 1



KDF11-AA

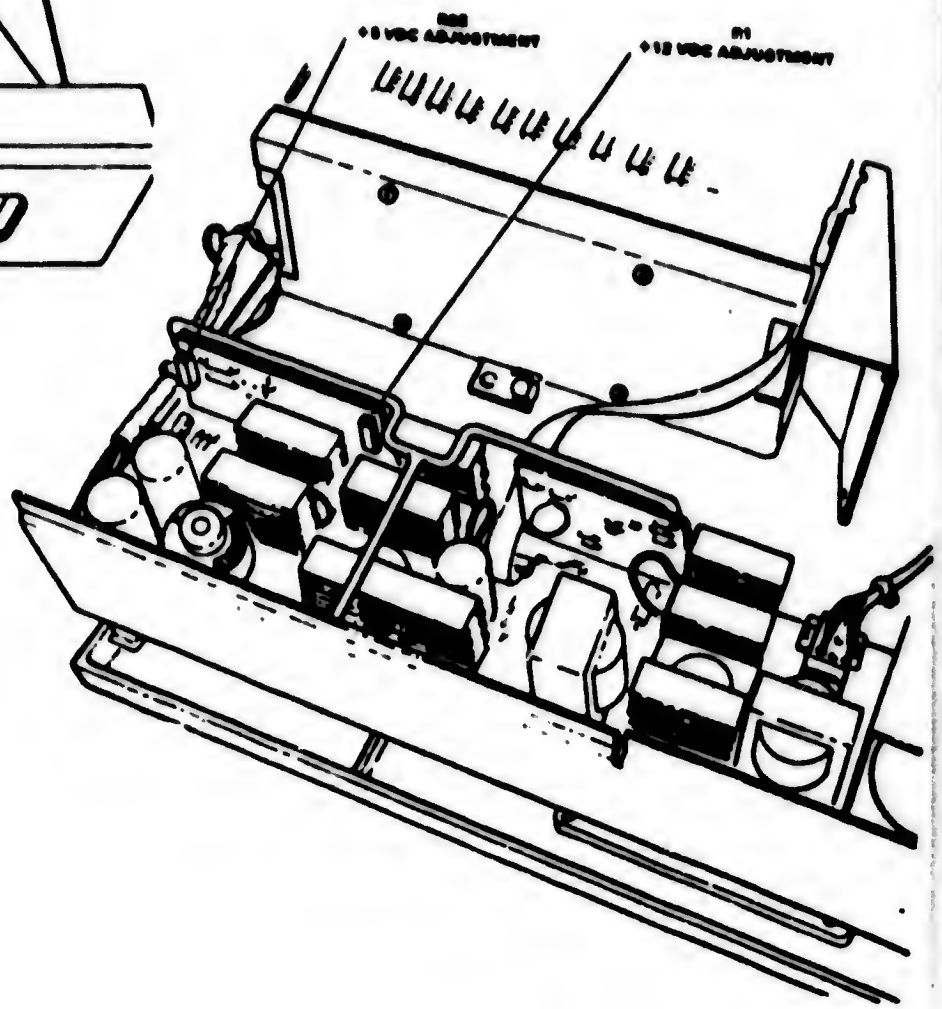
(M8186 DUAL SIZE MODULE)

FIGURE 2



Power Supply Assembly

FIGURE 3.1



Power Supply Adjustments

FIGURE 3.2

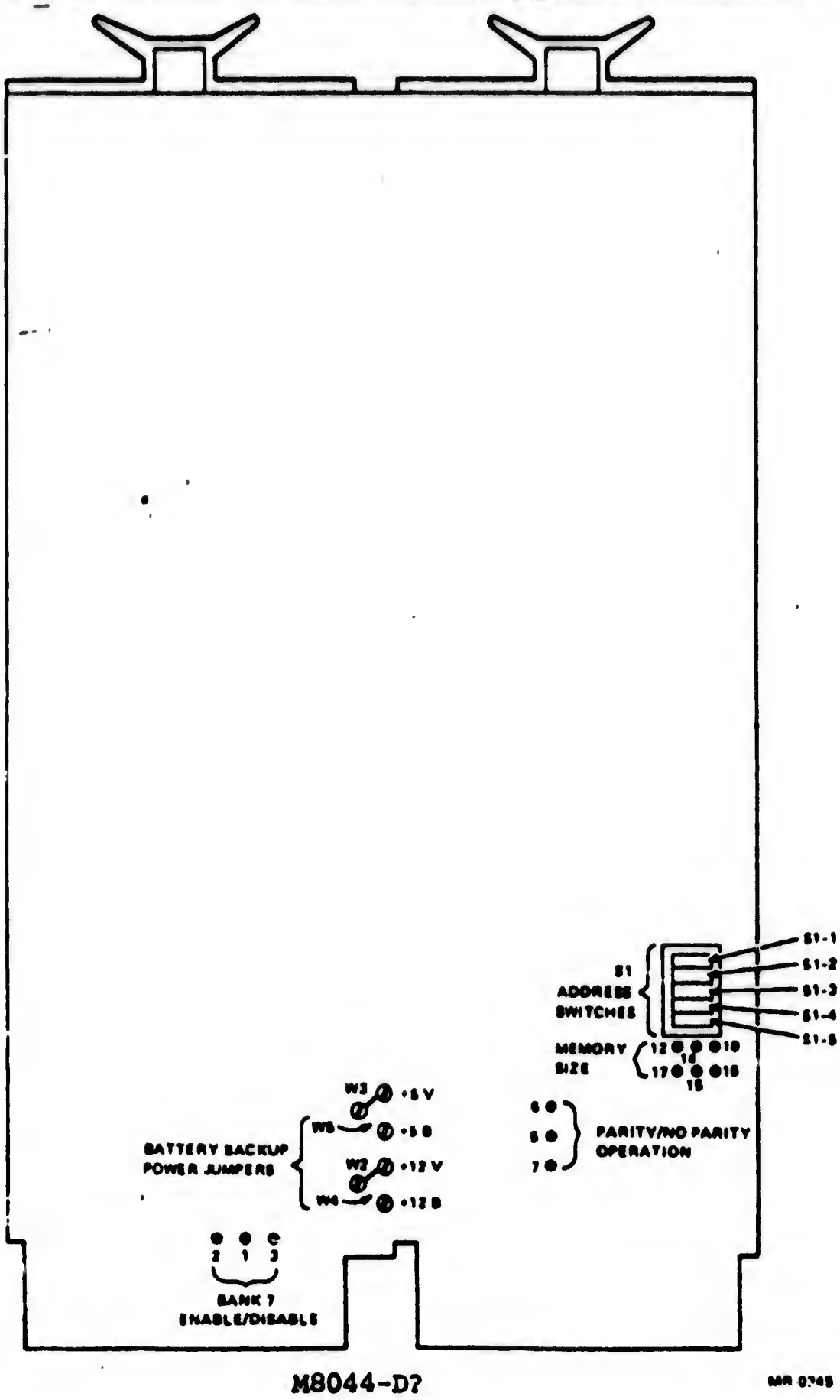


Figure 4 MSV11-D, MSV11-E Switch and Jumper Locations

	SIZE	CODE	NUMBER	REV
	A	SP	MAA 6170-0-0	A

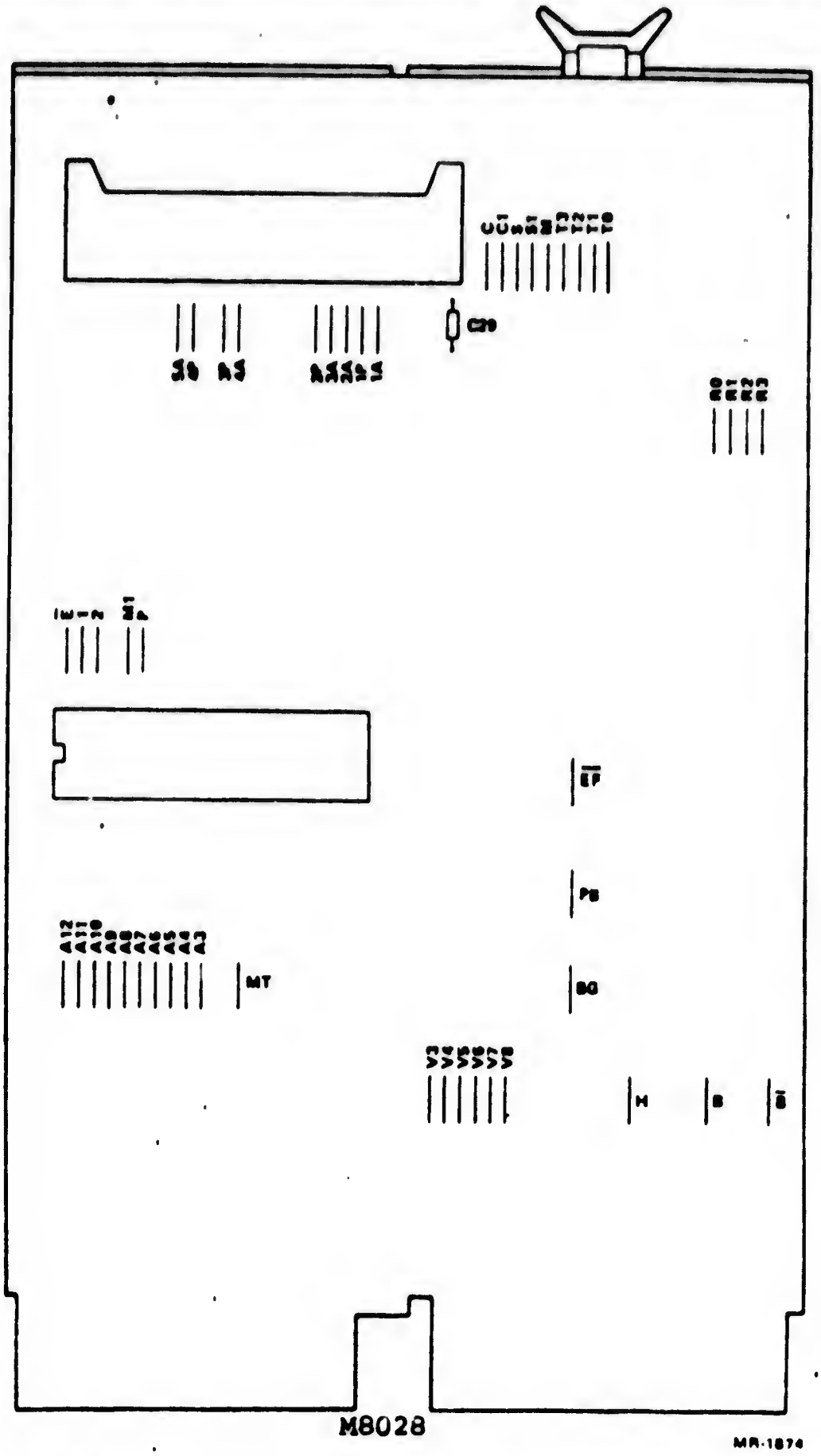


Figure 5 DLV11-F Jumper Locations

MONITOR INTERACTION AT LOCAL TERMINAL

Prompts		
	>	Operator may enter file name to call next diagnostic, or type control Z to put LSI-11 in ODT mode.
	@	If following 157776 after a file name has been entered, indicates the diagnostic is in the LSI-11 and the operator may communicate with it via ODT. If following "End pass" and the current PC, indicates the operator may give further instructions in ODT. Giving "760144" reestablishes communication with local monitor.
Inputs		
	File names	Used following ">" to call diagnostics.
	200G	Not to monitor - starts diagnostic if LSI-11 is in ODT.
	Break	Not to monitor - stops diagnostic.
	760144/	Reestablishes communication with local monitor if LSI-11 is in ODT.
Deposit	2	Following "000000" tells monitor that operator wishes to run another diagnostic
Deposit	1	Follow "000000" aborts monitor to host. This is the last input by the operator.
	Control Z	Following ">" puts LSI-11 in ODT.
Outputs		
	157776	Following file name entry indicates the diagnostic has been downloaded.
	NX	The requested file cannot be found.
	BDLD	The attempt to download the diagnostic was unsuccessful.
	END PASS	Diagnostic has completed a pass.
	Current PC	Following break indicates diagnostic has stopped at address printed.
	000000	Following "760144" indicates operator may input further instructions to local monitor (1 or 2).
	EX	Monitor has terminated at host.

FIGURE 6

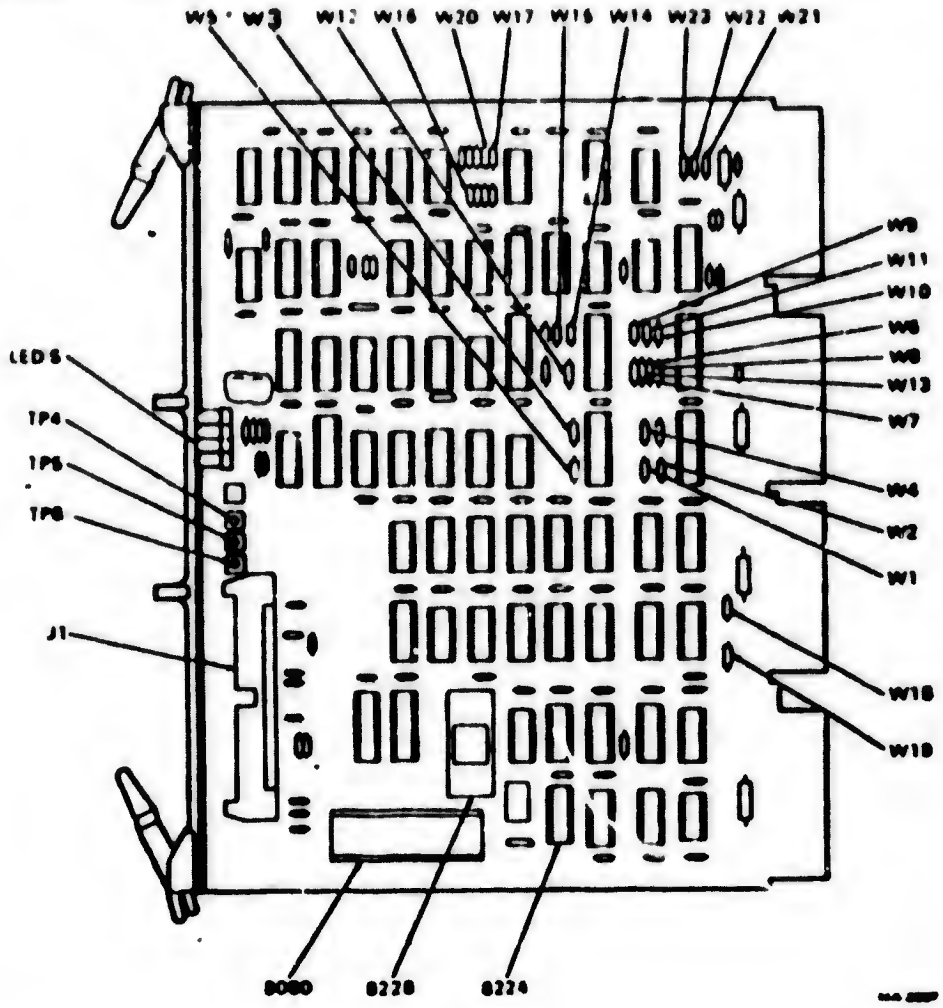


FIGURE
7.1

M8080

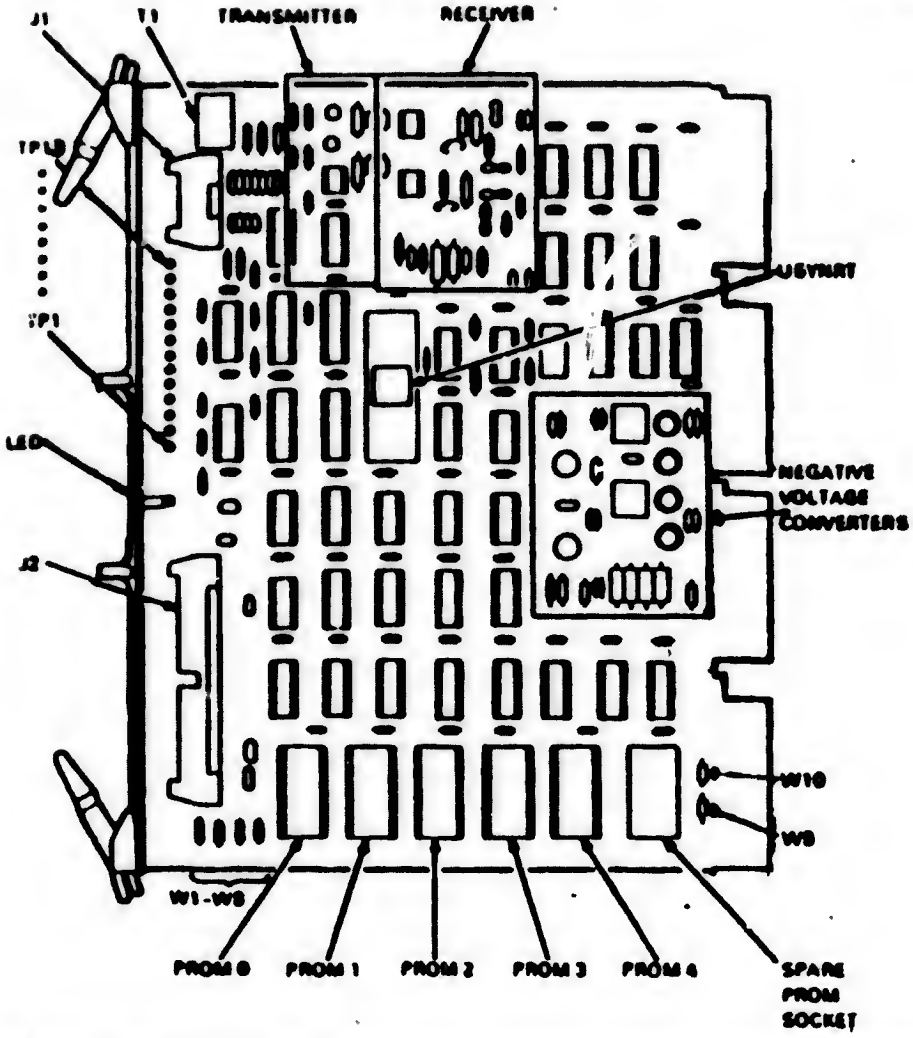


FIGURE
7.2

IS.11B

M8084

	SIZE	CODE	NUMBER	REV
	A	SP	MAA 6170-0-0	A


A6176

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. **DATE** 11 Jan 89

TITLE ISB-11 DEC DATAWAY CONTROLLER

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6175					
B	New update ECO CHANGE	MA-A0000-ML00 7	L.LECLERC	1 90	L. LeClerc (Lab)	7 Feb 90

ENG	APPD	SIZE	CODE	NUMBER	REV
Wayne Bungett		A	SP	MAA 6175-0-0	B

ISB-11 DEC DATAWAY CONTROLLER

1.0 REFERENCE DOCUMENTATION

1.1 Print sets order # MP00452

1.2 Maintenance Manual: EK-KMCMP-OP, EK-DMCLU-OP

1.3 ISB-11 Users Guide: EK-ISB-11-US

1.4 ISB-11 Field Acceptance Procedure: A-SP-ISB-11-07

1.5 Lib Kit: (KMC-11 Lib Kit) #ZJ234-RB

1.6 DZKCH Serial Bus Exerc[illegible]r (document) #MD-11-DZKCH-D

1.7 CZQRT RSX11M Test System (document) #AC-F153A-MC

2.0 REQUIRED TEST EQUIPMENT

2.1 PDP 11/34 or PDP 11/70 with minimum of 16K of memory, some type of disc load media, and one DD11-C SPC block.

2.2 SPC must be DD11-C.

2.3 SPC must provide +5, +15, and -15 volts.

2.4 Oscilliscope H475 or equivalent.

2.5 Digital volt meter

2.6 Multilayer Extender Module (W9048-Hex)

2.7 One 16 pin I.C. clip

2.8 Test Cable #7014152

2.9 Frequency counter may be required.

2.10 Some type of DPM terminal; such as a RT801, RT803, RT805, DPM01, VT110, or DPM50.

3.0 AVAILABLE DIAGNOSTIC PROGRAMS

3.1 Stand Alone Diagnostics Kit #ZJ-234-RB

Maindec	Description
CZKCC	Static Test, M8204 Data Path Test
CZKCD	Static Cram Branch Test (M8202)
CZKCA	Free Run, M8204 Data Path Test
CZKCE	Line Unit Test (M8202)
CZKCF	Bit Stuff Line Unit Test (M8202)
KMCA	DEC X-11 System Test

3.2 On-Line Diagnostics Kit #ZP-125-RD (Mag tape kit)

AP-F152A-MC	CZQRH RSX11M Test System Diagnostic

NOTE: The ZP-125-RD kit must be used to sys-gen a disc test pack before on-line diagnostics can be run.

4.0 INSTALLATION INSTRUCTIONS

4.1 M8204 Installation

4.1.1 The M8204 module should be installed in slot #2 of the DD11-C SPC block before installing. Remove the NPR Grant continuity wire that runs between pins CA1 and CB1 on the back plane for slot #2. If a system change requires removal of the M8204, this wire must be replaced.

4.1.2 The address and vectors for this module fall into the floating range, and a standard setup configuration is required.

ISB-11 #	Address	Vector
#1	160140	400
#2	160150	410
#3	160160	420
#4	160170	430

4.2 M8202 Installation

4.2.1 The M8202 module should be installed in Slot #3 of the DD11-C SPC block.

4.2.2 All switches on the module should be placed in the OFF position, for they are not used.

4.2.3 An ISB-11 Test Cable #7014152 should be fastened to the cable connector, attached to the module.

4.2.4 Some type of DPH terminal should be attached to the #7014152 test cable; such as a RT801, RT802, RT803, DPH01, VT110, or DPH50.

5.0 TEST SET UP

5.1 No special test set up is required, unless problems occur running diagnostics. If problems occur, refer to the maintenance manual for adjusting the line unit clock and read data one shot on the M8202 module.

6.0 POWER CHECKS

6.1 The ISB-11 utilizes 8 amperes of plus five volts per ISB. Care should be exercised that any test stand, or system installation considers the minimum current per regulator.

6.2 Voltage settings for the ISB-11 are very critical, and a Digital volt meter is recommended for making any adjustments. Test points, given below, for making adjustments should be taken on the module when making -15 volt adjustments on the 11/34's only. Set the -15 volts for exactly the same as the +15 volt reading, which is non-adjustable.

Voltage Test Points

Voltage	Module	Test Point
+15	M8202	+ side of C65
-15	M8202	- side of C64
+5	M8202	E 35 pin 16

6.3 Unibus Loading

The ISB-11 presents one DC and seven AC unibus loads to the system. A maximum of 20 AC loads are acceptable before separation by an M9202, or a 2 ft. bus cable is required.

The ISB-11 presents one DC and seven AC unibus loads to the system. A maximum of 20 AC loads are acceptable before separation by an M9202, or a 2ft. bus cable is required.

7.0 DIAGNOSTIC TEST PROCEDURE (STAND ALONE)

7.1 See Section 3.0 for order of diagnostics. The following procedure is used for all diagnostics.

7.1.1 Load diagnostic.

7.1.2 Load address at 200.

7.1.3 Set switch register to all zeros. Start program.

7.1.4 End of pass will be shown by type out.

7.1.5 No errors allowed.

8.0 DIAGNOSTIC TEST PROCEDURE (ON-LINE)

8.1 Host System Booting Procedure

8.1.1 Obtain a disk pack from the appropriate host media, which contains the RSX11M test system diagnostic package #ZP125-RD, and install it into Drive #0. Load Drive #0, and insure that "WRITE PROTECT" is off.

8.1.2 When Drive #0 is ready, and "ON LINE", boot the drive.

8.1.3
```
074036  000024  000652   001472
$DKO ----------------------------------TYPE: <DKO-RK05, DLO-
DEVICE DB00: NOT IN CONFIGURATION       RL01, DM0-RK06 or 07,
DEVICE DB01: NOT IN CONFIGURATION       DR0-RM02 or 03, DB0-
DEVICE DR00: NOT IN CONFIGURATION       RP04, 5, or 06>
DEVICE DR01: NOT IN CONFIGURATION
DEVICE MT00: NOT IN CONFIGURATION

RSX-11M V3.1  BL22  64K  MAPPED
>RED DK0:=SY0:
>RED DK0:=LB0:
>MOU DK0:SYSTEM
>@C1, 2]STARTUP
>* PLEASE ENTER TIME AND DATE (HR:MN DD-MMM-YY) [S]:
08:30 10-DEC-79  ---------------TYPE: <08:30 10-DEC-79>
```

```
>TIM 08:30  10-DEC-79
>INS  $ISBRPT
>INS  $ISBERR
>INS  $ISBOWL
>INS  $ISBINI
>INS  [7,7]FDCTIM
>FIX  FDCTIM
>LOA  SB:/PAR=GEN
>RUN  FDCTIM  M/RSI=20S
>INS  $PIP
>INS  $FLX
>* DO YOU WANT TO LOAD IPG DIAGNOSTICS
FROM MAGTAPE? [Y/N]:N----------------------------TYPE: (N)
>@ <EOF>
>SET /UIC=[200,270]-------------TYPE: <SET /UIC=[200,270]>
```

8.2 Run the error report task in order to clear out the error log.

8.2.1
```
>RUN ISBRPT ------------------------TYPE: <RUN ISBRPT>
ISBRPT - DEC DATAWAY ERROR REPORT TASK
>
PRINT SUMMARY [Y OR N]? N ----------TYPE: <N>
PRINT ENTIRE FILE [Y OR N]? N ---------TYPE: <N>
DELETE ERROR FILE [Y OR N]? Y ---------TYPE: <Y>
ISBRPT . . . OPERATION COMPLETE
```

8.3 Run the ISB11 DEC Dataway Diagnostic Exerciser.

8.3.1
```
RUN DZKCH ---------------------TYPE: <RUN DZKCH>
DCP-A>STA ---------------------TYPE: <STA>
# UNITS (D)  ? 1 ------------TYPE: <1>
UNIT 1 ------------------------TYPE: <1>
ENTER CONTROLLER NUMBER: (0) 0 ? 0 -----------TYPE: <0>
ENTER TERMINALS ON THAT CONTROLLER: (0) 1 ? 1 -----TYPE: <1>

NUMBER OF ENTERED TERMINALS = 1
UNIT ** CONTROLLER ** LOGICAL SB ** LUN **
001      000            001          011
```

8.4 After a complete run, the diagnostic must be terminated with a carriage return ----------TYPE: <CR>

```
TASK "TTO    " TERMINATED
TASK EXIT WITH OUTSTANDING IO
  PC = 046000
  PS = 170000
  R0 = 000002
  R1 = 000000
  R2 = 000000
  R3 = 000000
  R4 = 000003
  R5 = 000001
  SP = 001246
```

8.5 After a complete run, the error log must be checked to make sure there are no errors reported.

```
8.5.1 >RUN ISBRPT ----------TYPE: <RUN ISBRPT>
       ISBRPT - DEC DATAWAY ERROR REPORT TASK
      >
       PRINT SUMMARY [Y OR NO]? Y ----------TYPE: <Y>
       PRINT ENTIRE FILE [Y OR N]? N -------TYPE: <N>
       OUTPUT TO LINE PRINTER [Y OR N]? N ------TYPE:<N>
       WANT ONE CONTROLLER [Y OR N]? N ---------TYPE:<N>
       DELETE ERROR FILE [Y OR N]? N -----------TYPE:<N>
       ISBRPT . . . ERROR FILE IS EMPTY
       ISBRPT . . . OPERATION COMPLETE

       MCR>
```

8.6 Error reporting can be in the form of hard errors, typed out immediately, or soft errors; errors that are logged by the error logger. No errors are allowed.

DRAWING NO.	REV.NO.	PPS.	DESCRIPTION
A-SP-MAA7600	A	10	CSIG2-A RAINBOW TST-ACCP.PROC.
A-SP-MAA8010	A	2	UNIBUS TESTER
A-SP-MAA9025	A	4	PRE ACCEPTANCE HARDWARE Q.C.
A-SP-MAD2440	A	12	KT8-A
A-SP-MAD4216	A	16	RL8-A/RL01
A-SP-MAE0050	C	6	MAST PHASE III UETP
A-SP-MAE1000	A	44	PHASE III BACKUP DOC. RSX11-M
A-SP-MAF1050	A	14	WPS-8/211 PHASE III USER'S GUIDE
A-SP-MAF2050	A	16	WPS-8/212 PHASE III USER'S GUIDE
A-SP-MAV2100	B	26	11/780 CPU
A-SP-MAV2102	A	31	11/750 MAST I
A-SP-MAV2103	A	28	VAX 11/751 TEST
A-SP-MAV2200	B	16	FP780 FLOATING POINT ACC.
A-SP-MAV2605	A	25	MA780
A-SP-MAV2850	C	24	MS780 MEMORY
A-SP-MAV2910	B	18	RH780 MASS BUS ADAPTOR
A-SP-MAV2912	A	11	RH750

A76005

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE CS1G2-A RAINBOW TEST & ACCEPTANCE PROCEDURE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7600					

ENG.	APPD	SIZE	CODE	NUMBER	REV
Tom Zelenkewski		A	SP	MAA7600-0-0	A

CS1G2-A RAINBOW TEST & ACCEPTANCE PROCEDURE

1.0 INTRODUCTION

This procedure will be used in conjunction with other Maat Procedures to test the minimum and maximum rainbow equipment.

Optional rainbow equipment will also be included as part of this procedure, but will be separated prior to shipment.

1.1 The minimum configuration will be comprised of the following hardware:

1.1.1 1134A-DH - 16K Mos Memory, 10.5" box.

1.1.2 MS11-JP - 16K Mos Memory.

1.1.3 M9301-YX - Xerox Boot Terminator.

1.1.4 DL11-WB - SLU/RTC with BC05C-25.

1.1.5 DR11-K - Digital I/O Interface.

1.1.6 H775-CA - Battery Backup for 1134A.

1.1.7 X020 & X030 - CDC Disk Interface.

1.1.8 X020 & X021 - Character Dispatcher.

1.1.9 X026 - IG Output.

1.1.10 X027 - IG Input

1.1.11 X025 - Font Memory.

1.1.12 X604 - 14 Slot Backplane mounted in the 1134A.

1.1.13 BA11-LH - 5.25 Expander Box.

1.1.14 X605 - 9 Slot Backplane mounted in the BA11-LH.

1.1.15 X023 - Ampex Tape Controller.

1.1.16 X031 - 5V Regulator

1.1.17 BC11A-02 - 2 ft Unibus Cable

1.1.18 M9202 - Unibus Connector

1.1.19 M9001-YX - Connector module

1.1.20 BC08R-08 - Cable

1.2 The maximum configuration will be comprised of the following hardware:

1.2.1 The minimum configuration, minus BC11A-02.

1.2.2 XAUC - Auxillary Unibus Controller.

1.2.3 X025 - Font Memory (3 additional array modules).

1.2.4 MS11-JP - 16K Mos Memory (2 additional) total of 32K on the Aux. Bus.

1.2.5 M7850 - Parity Controller for memory on the Aux. Bus.

2.0 REFERENCE DOCUMENTATION

2.1 Standard DEC Equipment

2.1.1 Prints:

2.1.1.1 1134A Print Set - MP00190

2.1.1.2 H775 Print Set - MP00014

2.1.1.3 DR11-K Print Set

2.1.1.4 BA11-L Print Set - MP00018

2.1.2 Manuals:

2.1.2.1 EK-KD1EA-MM

2.1.2.2 11/34 System User's Guide - EK-11034-OP

2.1.2.3 M9301 - EK-M9301 - TM

2.1.2.4 MS11-E-J - EK-MS11E-MM

2.1.2.5 M7850 - EK-M7850-MM

2.1.2.6 BA11-L - EK-BA11L-MM

2.1.2.7 DR11-K - EK-DR11K-MM

2.1.2.8 DL11-W - EK-DL11W-MM

2.1.2.9 PDP 1134A Power System Desc EK-1134A-TM

2.2 Rainbow Equipment:

2.2.1 Prints:

2.2.1.1 CS1G2-A Print Set MP00548

2.2.2 Manuals:

2.2.2.1 IG-CSS-MO-F-4.3-17

2.2.2.2 CD-CSS-MO-F-4.3-16

2.2.2.3 X023 Tape - CSS-MO-F-5.9-01

2.2.2.4 X022 - CSS-MO-F-10.3-11

2.2.2.5 X030 -

3.0 REQUIRED TEST EQUIPMENT

3.1 CDC Disk Drive (9762)

3.2 ACT 11 or equivalent

3.3 VOM or Oscilloscope

3.4 LA36 or equivalent

3.5 VT50 or equivalent

3.6 Ampex Tape Drive

3.7 Three (3) X025 Font Memory Arrays

3.8 Two (2) MS11-JP Mos Memories

3.9 M7850 Parity Controller

3.10 Prewritten Tape for Ampex Tape Drive

3.11 XAUC

4.0 AVAILABLE DIAGNOSTICS

4.1 11/34 Lib Kit - ZJF04-RB

4.2 DR11-K Lib Kit - ZJ187-RB

4.3 Disk Controller (X020-X030)
Maindec-11-CIBBJ
Maindec-11-CIBBL

4.4 CD/IG Maindec-11-CIBBI

4.5 Tape Maindec-11- CIBBK

4.6 Aux Window Maindec-11-CIBBH

4.7 DECX-11

4.7.1 Rainbow DECX-11 Module

4.7.1.1 Disk - RRA

4.7.1.2 Tape - TXA

4.7.1.3 CD/IG - CXA

4.8 Diagnostic to generate prewritten tape for Ampex Drive.
Use tape diagnostic Maindec-11-CIBBK, answer questions.

5.0 INSTALLATION INSTRUCTIONS

5.1 Install the H785 Regulator into the 1134A. See 1134A Power Description Manual - EK-1134A-TM.

5.2 Mount the X604 Backplane into the 1134A box.

5.3 Mount the X605 Backplane into the BA11-L Expander Box.

5.4 Remove the Battery Backup jumpers from the DD11-PK Processor Backplane. See drawing C-IA-7011523 in the 1134A Print Set.

5.5 Connect the H775-B to the H785 Regulator using cable 7011906.

5.6 Remove the NPG wire (DD11-PK Backplane) C08A1 to C08B1.

5.7 Remove the NPG wire (X604 Backplane) C02A1 to C02B1. (X020 Disk controller)

5.8 Remove the NPG wire (X604 Backplane) C12A1 to C12B1 (X020 CD controller)

6.0 TEST SET UP

6.1 Place switch 2 on the M9301 to the "OFF" position.

6.2 Set the DR11-K to the following device and vector addresses

Device = 767770
Vector = 000150
Set the priority to BR4

6.3 Set the DL11-W to the following device and vector addresses:

Device = 777560
Vector = 000060
Set the priority to BR4

6.4 Set the DL11-W RCVR/TRAN. Baud to 300.

6.5 Check the disk controller for the following device and vector addresses:

Device = 764000
Vector = 000160
Check the priority for BR5 (X020 & X030)

6.6 Check the CD (X020 & X021) for the following device and vector addresses:

Device = 764300
Vector = 000270
Check the priority for BR5

6.7 Check the tape controller (X023) for the following device and vector addresses:

Device = 764100
Vector = 000110
Check priority for BR5

6.8 Set the MS11-JP memories to the following starting addresses:

1st - 000000
2nd - 100000
3rd - 200000 } Test Memories will be placed on the Aux Bus.
4th - 300000 }

6.9 Check the parity controllers for the following device addresses:

1st - 772100
2nd - 772102 (Aux Bus)

6.10 Install modules according to UA drawings. Refer to CS1G2-A Print Set, Drawing M-UA-CS1G2-A-0.

7.0 POWER CHECKS

7.1 Check the 1134A voltages as per Mast CA2260, Section 6.5.2

7.2 Connect the H775-B to the H785 regulator.

7.3 Check the H775-C for proper "BATT" status indication. See Mast Procedure (CA2832).

7.4 Check H775-C voltages. See Mast Procedure (CA2832).

7.5 Check X604 Backplane voltages. The voltage values are labeled (etched) onto the Backplane.

7.6 Check BA11-L Expander Box voltages. See Mast CA2260, Section 6.5.1.

NOTE: The core regulator will not be present; therefore, +20V and -5V voltages, will be zero.

7.7 Check X031 for $-5V$. Use test point located on X031 module, voltage is not adjustable.

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 Test 1134A as per Mast Procedure CA2260. See checklist for CA2260.

8.1.1 Memory CA 2825.

8.2 Test DL11-W as per Mast Procedure CA 5330. See checklist for CA 5330.

8.3 Test DR11-K as per Mast Procedure CA6260. See checklist for CA6260.

8.4 Test H775-C as per Mast Procedure CA2832. See checklist for CA2832.

8.5 Test M9301 as per Mast Procedure CA3330. See checklist for CA3330. Use the following CRC = 521
LPC = 46526

8.6 Test the disk controller off-line diagnostic.

8.6.1 Load into memory the disk diagnostic MAINDEC-11-CIBBJ

8.6.2 Set the switch register to 000000.
Load and start 000200. Run in accordance to checklist.

8.6.3 Pass indicator. "END PASS 0"

8.7 Test Disk interface on-line

8.7.1 Cable the disk to the controller. Place disk on-line.

8.7.2 Load into memory MAINDEC-11- CIBBL.

8.7.3 Set the switch register to 000000.

8.7.4 Load and start 000200. Run in accordance to checklist.

8.7.5 Pass indicator. "END PASS 0"

8.8 Test the CD and IG

8.8.1 Connect the CD to the IG.

8.8.2 Load into memory the CD diagnostic, MAINDEC-11-CIBBI.

8.8.3 Set the switch register to 000000.
Load and start 000200. Run in accordance to checklist.

8.8.4 Pass indicator. "END PASS 0"

8.9 Test the tape controller

8.9.1 Maintenance Mode

8.9.1.1 Load into memory the tape diagnostic MAINDEC-11-CIBBK

8.9.1.2 Set switch register to 000000.
Load and start 000200, Run in accordance to checklist.

8.9.1.3 Pass indicator. "END PASS 0"

8.9.2 On-Line

8.9.2.1 Connect tape drive to the tape controller.

8.9.2.2 Set switch register to [redacted].

8.9.2.3 Load and start [redacted]. Run as per checklist.

8.9.2.4 Pass indicator. "END PASS #"

8.10 Test minimum configuration with DECX-11 (off-line)

8.10.1 Load into memory the configured DECX-11.

NOTE: Enable DECX-11 to run off-line. See checklist

8.10.2 Load and start. Run in accordance with Mast checklist.

NOTE: Run with disk deselected.

8.11 Test minimum configuration with DECX-11 (on-line)

8.11.1 Connect tape and disk drives to controllers. Place both on-line.

NOTE: Prewritten tape for DECX-11 must be installed on the tape drive.

8.11.2 Load and start. Run as per Mast checklist.

8.11.3 Perform Unibus margining. See Mast Checklist.

8.12 Test maximum configuration (on-line)

8.12.1 Reconfigure system for maximum configuration.

8.12.2 Test auxilliary Unibus control

8.12.2.1 Load into memory the AUC diagnostic, MAINDEC-11-CIBBH

8.12.2.2 Set the switch register to [redacted].

8.12.2.3 Load and start [redacted]. Run as per Mast checklist.

8.12.2.4 Pass indicator. "END PASS #25"

8.12.3 Load into memory DECX-11 for maximum system.

8.12.4 Load and start. Run as per Mast checklist.

8.13 Test system as per specified on construction requisition (max or min).

8.13.1 If necessary, reconfigure to minimum system configuration.

8.13.2 Load and start DECX-11, on-line. Run as per Mast Checklist.

8.14 Check serial bit stream from IG.

8.15 Test DL11-W's @ 9600 Baud.

8.15.1 Load into memory MAINDEC-11-DZDLD.

8.15.2 Run as per Mast Procedure for DL11-WB. See Mast CA5330.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE UNIBUS TESTER Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-8010					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sobieski		A	SP	MAA8010-0-0	A

EN-01083-18-N672-(892)

UNIBUS TESTER

INSTRUCTIONS

Insure that the Bus Tester is grounded to the System Under Test. (Use ground strap provided)

Always power up tester first and down last.

REFERENCE DOCUMENTATION

Maint. Manual	A-SP-7605829-12
Engr. Specs:	A-SP-7605829-11
Prints:	D-BS-7605829-0-
MAINDEC Listing:	11-D8A Unibus Test Diag.

A9025

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE PRE ACCEPTANCE QC HARDWARE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-9025					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelewski		A	SP	MAA9025-0-0	A

PRE ACCEPTANCE QC

HARDWARE

1. All hardware with option(s) or system.
2. All hardware tight (screws, subassemblies, sliding racks, etc.)
3. Check for damaged hardware (crushed dents, deep scratches, etc.)
4. Spin fans for bearing or rubbing problems.
5. Wrong hardware (screws too long or short, wrong type washers, etc.)
6. Check alignment of black latches.
7. Filler bars between cabs, kick plates where applicable.
8. Jones strip covers in place.
9. Check extractor and module guides for tightness or cracks.
10. Cabs using only one carousel fan at top must have a plate covering second hole.
11. Check all cab fans for proper direction of air flow. (see prints)
12. Door pins must be secured with "E" rings.
13. Levelers firm with skid.
14. Sliding track mounted units should not interfere with other units in system (verify by sliding in and out to each extreme).
15. Check for missing turn fastners (devices with covers).
16. Three screws must be used on all ends of sliding tracks.

MODULES AND LOGICS

17. Shippability status. (REVCOM vs. ECO Status Sheet physical inspection of current ECO's).
18. Visually inspect any exposed modules for broken components. (pull modules if necessary).
19. DL11 modules must have crystals taped. (tape part #90-08269)

20. Copper shield between M411L 8K memory increments. (e.g. between slots 3&4 on 16K memory system) (between slots 3,4,6 and 7 on 24K memory system).

21. Check logics for improper wraps or shorts (workmanship).

22. Check logics for cracks, bent pins, and pin markers (on wired logic only).

23. Shrinkies on all pin connectors on logics (capacitors, resistors, etc.)

WIRING/CABLING

24. Harnesses and wiring meet workmanship standards.

25. Check cables for stripped wires and proper labeling (workmanship).

26. Check cable stickons for tightness, etc.

27. Pin crimps secured properly in connectors.

28. All panel mounted power supply panels must be grounded to cabinet frame using screw and Tinnerman clamp not at each mounting hole.

29. No pinched wire insulation.

30. Loose tie wraps.

31. Strain reliefs or cable clamps on tubing not wires.

32. No sharp edges near wiring.

33. Check black and white power wiring on reel motor in TU10 for proper crimping.

34. All mate-n-lock wiring in expander box should not be excessively stressed. (Pin crimps should have limited stress on them)

35. Check for cat grommet when blank panels are used near logics.

IDENTIFICATION

36. Correct decals (115V or 240V).

37. Seven digit serial tag (system no.) Top left hand corner of processing bay.

38. U.L. stickers where applicable.

39. Patent decals Mechanical and caution stickers on BAll boxes.

40. All fuses for proper decals.

MISCELLANEOUS

41. Check all circuit breaker switches for tightness and action.

42. Check console keys for rubbing, etc.

43. Check for recent ECO's.

44. Check cabs and doors for proper grounding.

45. Make sure slide on connectors are crimped properly.

46. Tight shipping blocks and flush with cab.

47. Filters on all cabs.

48. Cardboard on short cabs to eliminate excessive scratching.

49. Hour meters (hooked up at final inspection only). Exception - TU10 bay uses a slave timer to be removed at final inspection.

50. Check for push pennies on logics.

2240

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE 2/19/79

TITLE KT8-A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ORIG. PER ECO	ML003	L.LECLERC	15-MAY-79	TEJ/JGM	7-18-79

ENG	APPD	SIZE	CODE	NUMBER	REV
D. AYOTTE	Tom Jelenick	A	SP	MA-D2440-0-0	A

KT8-A

1.0 Introduction

The KT8-A is a memory management option that extends the memory capabilities of a PDP8 (KK8-A or KK8-F) CPU from 32K to 128K words. It offers virtual field addressing and memory protection in multi-user, realtime applications with full access of main memory space by DMA devices. In other words; memory addresses are generated by the CPU and by direct memory access (DMA) peripherals. However; the CPU can only provide a 12-bit address and DMA devices are limited to 15-bit addresses. Therefore; to reach a full potential of 128K word memory address space, the KT8-A adds 5 bits to a CPU generated address and 2 bits to a DMA generated addresses.

The intent of this procedure is to provide the necessary information needed for installation and checkout (acceptance) of the KT8-A.

2.0 Reference Documentation

2.1 Manuals & Engineering Specifications

2.1.1 Engineering Product Spec. (A-SP-KT8-A)
2.1.2 User's Manual (EK-KT08A-UG)

2.2 Prints and Schematics (both dev. & controller)

2.2.1 Manufacturing Print Set (MP00561)
2.2.2 Field Print Set (8-TC-KT8-A)

3.0 Required Test Equipment

3.1 Hardware & Media

3.1.1 Any KK8-A or KK8-F CPU
3.1.2 At least 4K of memory
3.1.3 KM8-AC Option

3.1.4 Console Device
3.1.5 DVM accurate to .1 volts at +/-15 volts
3.1.6 Oscilloscope (453 or equivalent)
3.1.7 Assorted soldering tools

4.0 Required Diagnostic Programs

4.1 AJKTA-??

6.0 Installation & Test Set - Up Instructions

6.1 The KT8-A consists of a hex height M8416 memory management control module. Although the M8416 module may be installed in any unused slot with an "E" connector ; it is normally installed in slot 4 or 8 depending on what type of CPU you have. If you have an 8A600 (KK8-F); the KT8-A should be installed in slot 8. But if your CPU is an 8A400 (KK8-A); then the KT8-A should be installed in slot 4.

A system with the KT8-A option can only be configured using any combination of MM8AB (16K core) and MS8C (16K or 32K MOS) memories.

6 2 The KM8-AC must have its jumpers reconfigured if the system has more than 32K of memory. (see table A and refer to figure 3)

TABLE A

If System Has -	W1	W2	W3	W4
MORE THAN 32K -	OUT	IN	IN	IN
LESS THAN 32K -	IN	OUT	OUT	OUT

6.3 MM8AB (CORE MEMORY)

6.3.1 If the system is made up of MM8AB core memories (16K), then they must be modified per ECO MM8AB #7. But if the total memory is 32K or less; then no changes need be made. (see table B and refer to figure 2)

TABLE B

MM8-AB 16K CORE MEMORY CONNECTIONS

MEMORY BANK	FIELD	CONNECTIONS WIRE *	JUMPERS **
0	0-3 (0-16K)	AB1 to EB2	1-3, 3-4 in
	4-7 (16-32K)	AB1 to EB2	2-4, 3-4 in
1	0-3 (32-48K)	AB1 to ED2	1-3, 3-4 in
	4-7 (48-64K)	AB1 to ED2	2-4, 3-4 in
2	0-3 (64-80K)	AB1 to EL2	1-3, 3-4 in
	4-7 (80-96K)	AB1 to EL2	2-4, 3-4 in
3	0-3 (96-112K)	AB1 to ER2	1-3, 3-4 in
	4-7 (112-128k)	AB1 to ER2	2-4, 3-4 in

* - A wire must be tack soldered to the fingers of the module for the purpose of Bank Select.
** - See figure 2 for locations

6.4 MS8C (MOS MEMORY - M8417)

6.3.1 If the system is made up of MS8C type memories (16K or 32K MOS), then refer to table C and D for the appropriate switch configuration.

TABLE C

MS8-CA 16K MOS MEMORY SWITCH SETTINGS

MEMORY		SWITCHES SET TO "OFF"	
BANK	FIELD	ALL OTHERS "ON"	***
0	0-3 (0-16K)	S1-1	
	4-7 (16-32K)	S1-2	
1	0-3 (32-48K)	S1-3	
	4-7 (48-64K)	S1-4	
2	0-3 (64-80K)	S1-5	
	4-7 (80-96K)	S1-6	
3	0-3 (96-112K)	S1-7	
	4-7 (112-128K)	S1-8	

*** - See figure 2 for illustration

TABLE D

MS8-CB 32K MOS MEMORY SWITCH SETTING

MEMORY		SWITCHES SET TO "OFF"	
BANK	FIELD	ALL OTHERS "ON"	***
0	0-7 (0-32K)	S1-1 and S1-2	
1	0-7 (32-64K)	S1-3 and S1-4	
2	0-7 (64-96K)	S1-5 and S1-6	
3	0-7 (96-128K)	S1-7 and S1-8	

*** - See figure 2 for illustration

7.0 Power Checks

7.1	Voltage	Backplane Pin	Tolerance
	+5	ANY A2	+/-.25

8.0 Diagnostic Test Procedure

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria, e.g.: Pass Counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the "CHECKLIST".

8.1 AJKTA-?? KT8-A MEMORY MANAGEMENT DIAGNOSTIC

8.1.1 It is assumed that all basic CPU and memory diagnostics have been run successfully before attempting to run the KT8-A diagnostic.

8.1.2 Load the diagnostic using the appropriate load mediam. eg.(APT,RX,RL,ETC.)
The starting and running of the test is determined by the absence or presence of an operators console.

8.1.3 Starting and running with a console-
A. Load address 200 -
B. Select the desired control switch settings-(see table E)
C. Depress clear; then continue-
D. The program will then print:

"AJKTA-??"
KT8-A MEMORY MANAGEMENT OPTION

AMOUNT OF MEMORY(1-37)?" XX<CR>

note - XX is operator input for the number of memory fields. One field = 4K

Examples: 8K = 01
16K = 03
32K = 07

At this point you should enter the number of memory fields available for testing. This figure is required for running the basic addressing section of the diagnostic. If a "0" is typed then the addressing test is not run.

E. Upon completion the diagnostic will type :

"END PASS # N."

No errors are allowed.

TABLE E

CONTROL SWITCHES

SWITCH	STATE	DESCRIPTION
0	0	Halt on error
	1	Inhibit error halt continues on to next test.
1	0	Continue on error
	1	Loop on error
2	0	Don't loop on test
	1	Loop on test displayed in switches 6-11
3	0	Continue testing after a completed pass.
	1	Halt at the end of a pass.
4	0	Print all errors
	1	Inhibit error type-outs
5	UNUSED	

8.1.5 Starting and running without an operators console.

A. Because a hardware console is not necessary a console package has been added to the KT8-A diagnostic. In order to utilize and activate the console package there are three parameter control words that must be altered. These three words are contained in memory locations 20,21 and 22 where:

Location 20 / PSEUDO SWITCH REGISTER

Location 21 / HARDWARE IDENTIFIER 1

Location 22 / HARDWARE IDENTIFIER 2

8.1.6 To activate the console package, you must set location 22 - bit 3=1 and you must also set location 21 - bit 0=0 in order to enable the pseudo switch register.
You can access these locations by running ODT (Octal Debugging Technique) before starting the program. As the following example depicts.

note - the underscored characters are user inputs

```
TYPE:              .ODT
RESPONSE:
TYPE:              20/ ???? XXXX<LF>
TYPE:              21/ ???? 3000<LF> (SYS. HAS OPT 1&2)
TYPE:              22/ ???? 400<CR>  (SYS. HAS NO CONS.)
```

note - The ? are previous contents of.
The X are your desired contents

note - see table E for control switch settings

See tables F and G for a complete breakdown of the hardware identifier 1 and 2 functions.

8.1.7 Starting the program can be accomplished by typing in the following:

200G<CR>

8.1.8 The program will then print the following message:

"AJKTA-??"
KT8-A MEMORY MANAGEMENT OPTION

AMOUNT OF MEMORY(1-37)?" <CR>

note - <CR> is the default

8.1.9 Type in the number of extended memory fields and type a caraige return. The program should run error free and will terminate with the message:

"END PASS # N."

Run times will vary according to how much memory is selected.

8.1.10 Control characters are supplied to give the user the ability to perform various functions while the program is running. They are as follows:

CONTROL C (^C)	This forces a restart at location 7600 of field zero or return to the console monitor.
CONTROL S (^S)	This will stop any output to a console terminal. The only way to continue is to type a ^Q to resume printing or a ^C to abort the program completely. This is a non printing character.
CONTROL Q (^Q)	This is to continue a program after a ^S is typed. This is a non printing character.

CONTROL G (^G) The ^G allows the user to change the value of the psuedo-switch register. Upon typing ^G the console terminal will print "^G" and then the switch register question. At this point the user may change the value of the pseudo-switches or type a terminating character.

TABLE F

LOCATION 21 / HARDWARE IDENTIFIER 1

BIT	OCTAL VALUE	FUNCTION WHEN 0	FUNCTION WHEN 1
0	4000	use pseudo switches	use hard switches
1	2000	no option 1	has option 1
2	1000	no option 2	has option 2
3	400	no 8A simulator	has simulator
4	200	no option simulator	has simulator
5	100	not on 8A XOR	on 8A XOR
6	40	not PDP8-E type CPU	PDP8-E type CPU
7-11		8A memory size EX.	4K = 00 8K = 01 28K = 06 128K = 37

TABLE 6

LOCATION 22 / HARDWARE IDENTIFIER 2

BIT	OCTAL VALUE	FUNCTION WHEN 0	FUNCTION WHEN 1
0	4000	not on APT line	on APT 8A line
1	2000	not on ACT line	on ACT 8E line
2	1000	not yet defined	
3	400	use pseudo switches	

KMS -AC (M8317-YB)

SWITCH SETTINGS:

	1	2	3	4	5	6	7	8
S1:	OFF	ON	ON	OFF	OFF	ON	ON	ON
S2:	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON

FIGURE 1

MM8-AB CORE MEMORY

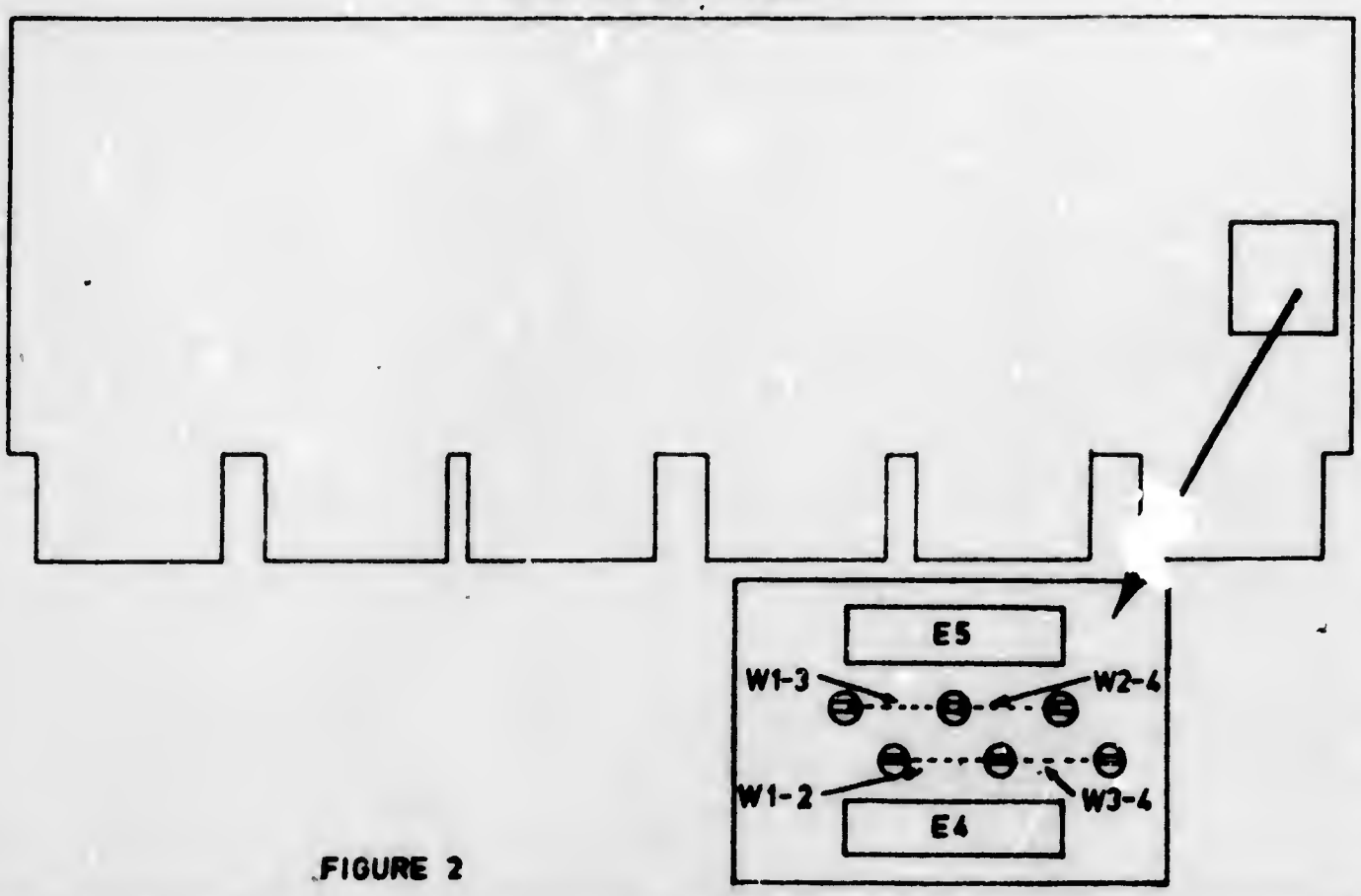


FIGURE 2

MS8-CA/CB (M8417)

JUMPER CONFIGURATIONS (REFERENCE ONLY-SET AT FACTORY):

IN: W2, W3, W4, W9

OUT: W1, W5, W6, W7, W8, W10, W12, W13, W14, W15, W16

FIGURE 3

D42160

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE 2/20/79

TITLE RL8-A/RL01

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ORIG. PER ECO	ML0003	L LECLERC	15-MAY-79	TGJ/DTM	7-18-79

ENG	APPD	SIZE	CODE	NUMBER	REV
D. AYOTTE	Tom Jelenevich	A	SP	MA-D4216-0-0	A

RL8-A/RL01

1.0 Introduction

The RL8-A/RL01 Disk Subsystem is a random access, mass storage system that stores up to 3.5 million 12-bit words (per disk) in fixed length blocks on pre-formatted disk cartriges. The RL8-A controller provides the interface and the control functions between all Omnibus PDP-8's and the RL01 disk drives.

The RL8-A (M8433) interface and control logic is contained on a single multi-layer hex height module. It is inserted into the Omnibus backplane and connected to the first drive via a BC08J-20 interface cable. Connections between the controller and the drives are made using the conventional daisy chain method with a 70-12122-08 cable.

The RL8-A controller can control up to four RL01 disk drives. It can communicate with one or more drives, but can only transfer data to or from one drive at a time.

2.0 Reference Documentation

2.1 Manuals & Engineering Specifications

2.1.1 RL8-A Omnibus controller Technical Manual	EK-RL8A-TM
2.1.2 RL01 Drive Technical Description Manual	EK-RL01-TD
2.1.3 RL01 Disk Subsystem Service Manual	EK-RL01-SV
2.1.4 RL01 Disk Drive, Parts Breakdown	EK-RL01-IPB
2.1.5 PDP8-A Miniprocessor User's Manual	EK-81002-MM
2.1.6 PDP8-A Operator's Handbook	DEC-8A-HOPHB

2.2 Prints and Schematics (Both Drive & Controller)

2.2.1 RL8A Field Maintenance Print Set MP00538

2.2.2 RL01 Field Maintenance Print Set MP00527

3.0 Required Test Equipment

3.1 Hardware & Media

3.1.1 A PDP8A,E,F or 8M CPU

3.1.2 At least 8K of memory

3.1.3 An RL8A/RL01 Controller/Drive

3.1.4 Diagnostic loader (Diskette,Paper tape,etc.)

3.1.5 A console device

3.1.6 DVM, accurate at .1V @ 15V

4.0 Required Diagnostic Programs

4.1 08-AJRLA.....DISKLESSS CONTROLLER

4.2 08-AJRLB.....DRIVE FUNCTION 1

4.3 08-AJRLC.....DRIVE FUNCTION 2

4.4 08-AJRLD.....DRIVE COMPATIBILITY

4.5 08-AJRLE.....PERFORMANCE EXERCISER

4.6 08-AJRLG.....PACK VERIFIER

5.0 Special Instructions

5.1 When converting a RL01 from 115V to 230V, it is only necessary to invert the voltage selector plug, change the [illegible] and the serial tag. The voltage range plug should be left on "NOM".

6.0 Installation And Test Set Up Instruction

6.1 Unpacking and Installation

6.1.1 Remove the drive from the shipping carton and inspect for physical signs of shipping damage. The shipping carton should contain the following items:

1 - RL01 disk drive assembly
1 - envelope w/paperwork
1 - I/O cable assembly - 10 ft.
1 - Set of chassis slides
1 - Bag of mounting hardware (quantities and P/N's specified by A-PL-RL02-A-0)
1 - RL01 Disk subsystem users guide
1 - Field Maintenance print set

6.1.2 Shipping Brackets

6.1.2.1 There is a shipping bracket; the head retainer bracket. When the drive is powered on, the top cover may be opened and the bracket can be seen in front of the positioner assembly. Loosen the one screw holding it in place, and let the bracket pivot downwards 90 degrees. Re-tighten the screw.

6.1.2.2 When shipping the drive, restore the head restraint shipping bracket to its upright position, and if the drive is slide mounted, install the 2 shipping brackets which were contained in the hardware kit. For instructions, refer to drawings E-UA-RL8A-0-0 or E-UA-RL01AK-0-0 for bracket location.

6.2 Controller Installation

6.2.1 To make the RL8-A (M8433) compatable with the RL02 disk (double density), remove W9 and install W8. Refer to figure 1.

6.2.2 Verify that the IOT Device code and Break Priority jumpers are configured properly. Refer to tables A, B and C. (See figure 1 for jumper and ROM locations.)

NOTE - standard Device Codes are 60/61 and priority 0

TABLE A

IOT DEV. CODE	JUMPERS INSTALLED	
	W1	W2
60/61	IN	OUT
62/63	IN	IN

TABLE B

BREAK PRIORITY	JUMPERS INSTALLED		
	W3	W4	W5
0	IN	OUT	IN
1	OUT	IN	OUT

TABLE C

FACTORY INST. JUMPERS		W1	1--3	2--5	W6	W7
ROM PN#	23012E2-00	IN	OUT	IN	IN	OUT
UV PROM PN#	23040B7-00	IN	IN	OUT	OUT	IN

6.2.3 Dress the BC08J-20 interface cable in the PDP-8 chassis and connect the Berg connector to the M8433 controller module.

6.2.4 Install the M8433 module in any unused slot that lies below the last memory slot in the Omnibus backplane. (Slot 17 in KK8-F "Word Processors")

6.2.5 Insert the free end of the BC08J-20 interface cable into the RL01 "CABLE IN" connector of the rear of the first disk drive.

6.2.6 If this is a multi-drive system, connect the daisy chain cable (70-12122-08) from the "CABLE OUT" connector of the previous drive to the "CABLE IN" connector on the next drive.

6.2.7 Install the drive terminator module (70-12293) in the last drive's connector marked, "CABLE OUT".

6.2.8 Install the proper unit select plug at the front of each drive.

SELECT PLUG	PART NUMBER
0	12-12691-00
1	12-12691-01
2	12-12691-02
3	12-12691-03

7.0 Power Checks:

7.1 Inspect the terminal block assembly at the rear of the drive to ensure that it is configured properly for the input power to be used. There are two voltage ranges: Low 90-132 VAC, High 180-264 VAC

The power requirements for the RL8-A (M8433) are:

+5 Vdc +/- .25 V -at test point/Finger AA2
+15 Vdc +/- .5 V -at test point/Finger DA2
-15 Vdc +/- .5 V -at test point/Finger DB2

8.0 Diagnostic Test Procedure

"For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria, e.g.: pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the CHECKLIST."

The diagnostics that are run to checkout the RL8-A/RL01 all contain the "CONSOLE PACKAGE". This package is a part of every diagnostic and supplies the user with a software switch register and a few control keys that allow operator intervention. A description of the control keys; along with a complete breakdown of the solftware parameters (switch register, etc.), can be found in the diagnostic listings.

8.1 08-AJRLA - Diskless Controller Diagnostic

8.1.1 It is assumed that the CPU, console device and all available memory have successfully run their respective diagnostics.

8.1.2 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX, APT,etc.)

note - the drive with the terminator must be powered off or turned off line because this is a "diskless" diagnostic.

8.1.3 With the switch register = 0; start the program by typing:

200G

8.1.4 Upon start-up the program will ask the following :

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLA?? RL8-A DSKLS CTRLR	
SR=0000	<CR>
ENTER AMOUNT OF CONTIGUOUS MEMORY AVAILABLE FOR USE:	XX<CR>

where XX = 1 - 8K
2 - 12K
3 - 16K
4 - 20K
5 - 24K
6 - 28K
7 - 32K

EXECUTE PHASE LOCKED LOOP ADJUSTMENT ROUTINE?	<CR>

"END PASS 000X"

8.2 06-AJRLB - Drive Function 1

8.2.1 It is assumed that the diskless controller diagnostic (AJRLA) has been run error free before continuing.

8.2.2 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX,APT,etc.)

note - power up all drives

8.2.3 With the switch register = 0; start the program by typing:
200G

8.2.4 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLB?? RL8-A/RL01 DR PT1	
SR=0000	<CR>
TEST DRIVE 0 ?	Y/N<CR>
TEST DRIVE 1 ?	Y/N<CR>
TEST DRIVE 2 ?	Y/N<CR>
TEST DRIVE 3 ?	Y/N<CR>
IS 8/A OPTION 1 AVAILABLE?	Y<CR>
DO YOU WISH TO SELECT NON-DEFAULT PARAMETERS?	N<CR>
END PASS 000X	

8.3 08-AJRLC - Drive Function 2

8.3.1 It is assumed that the drive function 1 diagnostic (AJRLB) has been run error free before continuing.

8.3.2 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX,APT,etc.)

8.3.3 With the switch register = 0; start the program by typing:

200G

8.3.4 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLC?? RL8-A/RL01 DR PT2	
SR=0000	<CR>
TEST DRIVE 0 ?	Y/N<CR>
TEST DRIVE 1 ?	Y/N<CR>
TEST DRIVE 2 ?	Y/N<CR>
TEST DRIVE 3 ?	Y/N<CR>
IS 8/A OPTION 1 AVAILABLE?	Y<CR>
DO YOU WISH TO SELECT NON-DEFAULT PARAMETERS?	<CR>
END PASS 000X	

8.4 08-AJRLC - Pack Verifier

8.4.1 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX,APT,etc.)

8.4.2 With the switch register = 0; start the program by typing:

200G

8.4.3 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLG?? RL8A/RL01 PCK VFYR	
SELECT NON-DEFAULT PARAMETERS?	<CR>
TEST DRIVE 0 ?	Y/N<CR>
TEST DRIVE 1 ?	Y/N<CR>
TEST DRIVE 2 ?	Y/N<CR>
TEST DRIVE 3 ?	Y/N<CR>
ARE YOU SURE?	YES<CR>

```
WORKING ON UNIT X

PACK SERIAL NO.: XXXXXX

NO NEW BAD SECTORS FOUND (FIELD FILES NOT REWRITTEN)


DONE
```

8.5 08-AJRLD - Drive Compatibility

8.5.1 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX,APT,etc.)

NOTE - at least 2 disk drives are needed along with one RL01 Disk Pack with not more than 16 bad sectors

8.5.3 With the switch register = 0; start the program by typing:

200G

8.5.4 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLD?? RL8A/RL01 DRIVE COMPATIBILITY TEST	
UNIT 0 = DRIVE (0-7)?	0<CR>
UNIT 0 ON THIS SYSTEM (Y/N)?	Y<CR>
DEVICE CODE (60,61) (Y/N)?	Y<CR>
UNIT 1 = DRIVE (0-7)?	1<CR>
UNIT 1 ON THIS SYSTEM (Y/N)?	Y<CR>
DEVICE CODE (60,61) (Y/N)?	Y<CR>
UNIT 2 = DRIVE (0-7)?	2<CR>
UNIT 2 ON THIS SYSTEM (Y/N)?	Y/N<CR>
DEVICE CODE (60,61) (Y/N)?	Y<CR>
UNIT 3 = DRIVE (0-7)?	3<CR>
UNIT 3 ON THIS SYSTEM (Y/N)?	Y/N<CR>
DEVICE CODE (60,61)?	Y<CR>
SR=0000	<CR>
ARE YOU SURE (Y/N)?	Y<CR>

NOTE - the following dialogue is for two drives selected

MOUNT PACK ON DRIVE 0 THIS SYSTEM

WAIT FOR DRIVE READY

TYPE <RETURN> TO CONTINUE . . . <CR>

MOUNT PACK ON DRIVE 1 THIS SYSTEM

WAIT FOR DRIVE READY

TYPE <RETURN> TO CONTINUE . . . <CR>

TEST COMPLETE - ALL DRIVES COMPATIBLE

NOTE - a <CR> will restart the program without the dialogue
- a <LF> will restart the program completly

8.6 08-AJRLE - Performance Exercisor

8.6.1 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX,APT,etc.)

8.3.3 With the switch register = 0; start the program by typing:

200G

8.3.4 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLE?? RL8A/RL01 PERFORMANCE EXERCISER	
NUM FLDS EXTD R/W MEM (1-7)?	XX<CR> where X = 1 - 8K 2 - 12K 3 - 16K 4 - 20K 5 - 24K 6 - 28K 7 - 32K
TEST DRIVE 0 (Y/N)?	Y/N<CR>
TEST DRIVE 1 (Y/N)?	Y/N<CR>
TEST DRIVE 2 (Y/N)?	Y/N<CR>
TEST DRIVE 3 (Y/N)?	Y/N<CR>
DC (60,61) (Y/N)?	Y<CR>
SR=0000	<CR>
ACPT MODE (Y/N)?	Y<CR>
ARE YOU SURE (Y/N)?	Y<CR>

NOTE - the following is for two drives (0 and 1)

DRIVE 0 PACK WRITTEN

DRIVE 0 PACK READ OK

DRIVE 1 PACK WRITTEN

DRIVE 1 PACK READ OK

END PASS DRIVE 0 SEEK

END PASS DRIVE 1 SEEK

END PASS DRIVE 0 DATA

END PASS DRIVE 1 DATA

END PASS DRIVE 0 ACPTD

END PASS DRIVE 1 ACPTD

8.7 Error Summary - no errors allowed

R L 0 1
DISK CONTROLLER BOARD
M 8 4 3 3

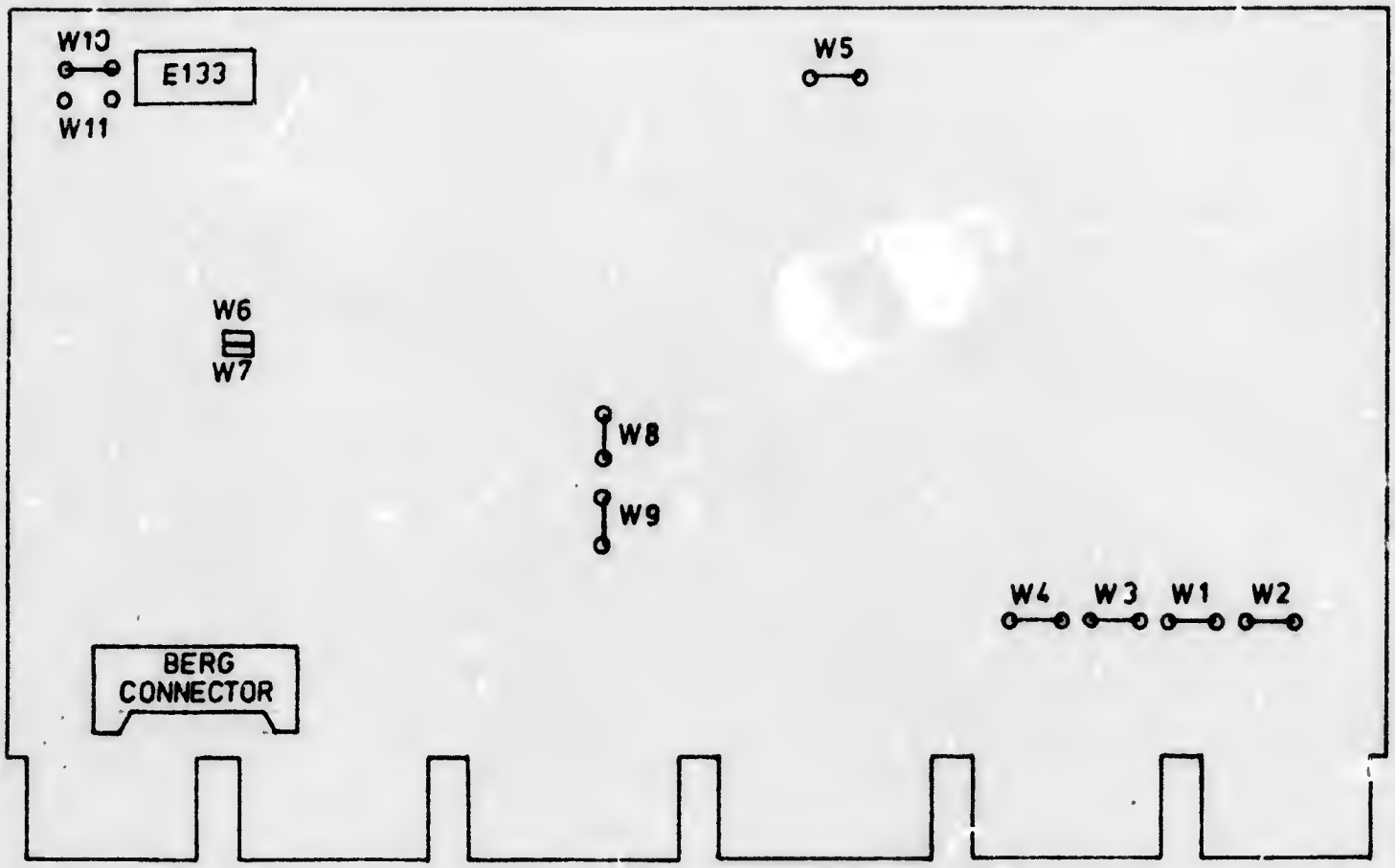


FIGURE 1


E00560

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 2/3/81

TITLE MAST PHASE III UETP

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Initial Release	-	S. Estes	8/27/79		
B	Add to spec inst. and RSX11M+ to sheet 3.	1	S. Estes	11/15/79		
C	Remove 11/74 references and LSI references. Add note about "Q-BUS" CPU's. Add RSX11M+ to UETP matrix on page five.	2 MLO12	T. Kenney D. Ayotte	6/10/80 2/3/81	David Ayotte	8/9/81

ENG	APPD	SIZE	CODE	NUMBER	REV
S. Estes	B. Beck	A	SP	MA-E0050-0-0	C

EN-01009-10-N872-0895/

MAST PHASE III - UETP

1.0 Introduction

UETP (User Environmental Test Package) is a universal name for system test software that runs under an operating system. Currently only RSX11, RSTS/E, RT11, and RSX11M+ have some form of recognized UETP package. Since every available operating system does not have a separate UETP package, a decision matrix has been developed to aid the user in the selection of UETP packages based on the Customer's configuration. This document is not intended to instruct the user on UETP or system software build. Reference appropriate system software manuals for software and UETP build and run procedures.
Note: This document is only applicable to PDP11 family processor's.

2.0 Reference Documentation

2.1 Software Product Description (SPD)
Table of Contents.

3.0 Recuired Test Equipment

3.1 Minimum Hardware & Media
The minimums presented in this section may override the 'No Software Ordered' matrix in section 5.1.2.

3.1.1 UETP minimums

3.1.1.1 For RSTS/E UETP - More than 64KW of memory, memory management (KT) and at least one supported system disk. NOTE: RSTS/E UETP DOES NOT SUPPORT"Q-BUS" CPU's.

3.1.1.2 For RSX11 UETP - 32KW of memory, memory management (KT) and at least one supported system disk (with a MAGTAPE) or two supported system disks (without a MAGTAPE).

3.1.1.3 For RT11 UETP - 16KW of memory and at least two supported system disks.

3.1.1.4 For RSX11M+ - 256KW of memory and one supported system disk (with MAGTAPE) or two supported system disks (without MAGTAPE).

3.1.2 Hardware minimums

3.1.2.1 VAX 11/780 systems run VAX VMS UETP.

3.1.2.2 RX floppy disks are currently only supported as a system disk by RT11.

3.1.2.3 All systems require an appropriate console terminal.

4.0 Required Diagnostic Programs

Not Applicable

5.0 Special Instructions

5.1 The UETP decision matrix's listed in sections 5.1.1 and 5.1.2 should be used as the guide for selecting a particular operating system UETP package.

Note: Should the Customer configuration support the operating system software ordered but does not meet the UETP minimums as outlined in section 3.1.1 , Software Support will determine which UETP will be run. Software Support will either select the next level UETP (from RSTS to RSX, from RSX to RT11) or modify the Software build as deemed necesary.

5.1.1 This Matrix is to be used when Customer has specified operating system software or license. This matrix is based on the best estimate of operating system similarities with RT, RSTS/E, RSX, and RSX11M+. If Customer software is not listed below, use "No Software" Matrix in 5.1.2.

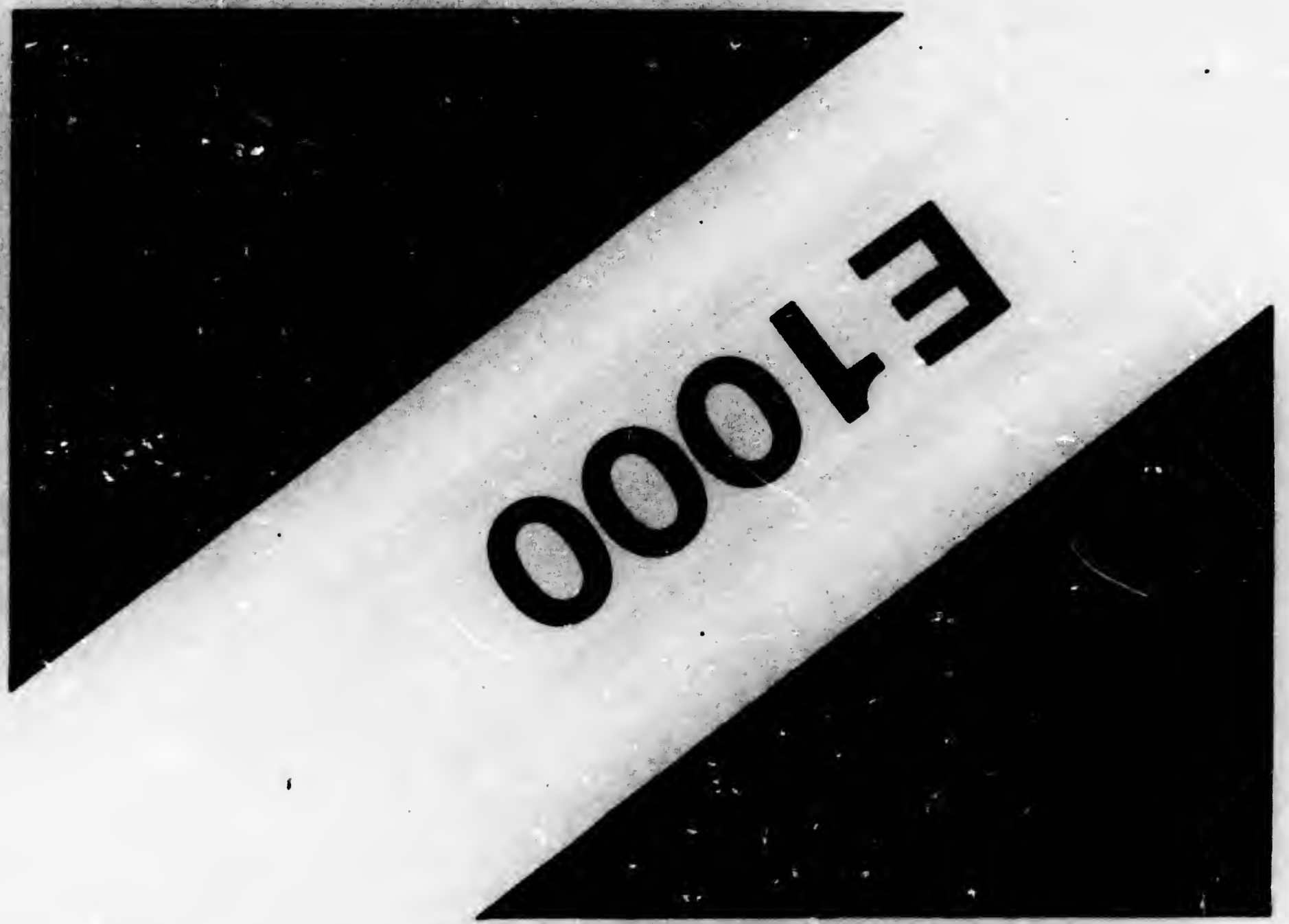
UETP MATRIX
KNOWN CUSTOMER SOFTWARE

Customer ordered this base software or license	UETP to be run				
	RSX11	RSTS	RT11	RSX11M+	
RSX11	X				
TRAX	X				
IAS	X				
TMS11	X				
RSTS/E		X			
CTS-500		X			
DSM11 (DEC STD. MUMPS)		X			
RT11			X		
CTS-300			X		
RSX11M PLUS					
RSX11M+				X	

5.1.2 Matrix to be used when Customer has not ordered an operating system software or license. This matrix is based on general RSX, RSTS/E and RT software system usage and limitations.

UETP MATRIX
NO SOFTWARE OR LICENSE ORDERED

Customer did not order any software or license	UETP to be run		
	RT11	RSX11	RSTS/E
System has ≤ 32KW of memory	X		
System has > 32KW but ≤ 64KW of memory		X	
System has > 64KW of memory			X


0001

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 10/6/80

TITLE PHASE III BACK UP DOCUMENTATION RSX11-M (DLD)

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	NEW BACKUP	MA-A0000-ML011			[illegible]	12/5/

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Kenney	[signature]	A	SP	MA-E1000 -0-0	A

1.0 INTRODUCTION

1.1 This document details the steps necessary in generating an RSX11-M operating system and running the UETP, utilizing DYNAMIC LOADABLE DRIVERS (DLD).

1.2 Document Usage:

Section 8, Sample Sysgen, provided for those users unfamiliar with RSX11 DLD UETP.
Section 7, UETP Flow Chart, brief instructions for those users familiar with RSX11 DLD UETP.
Section 5, Special Instructions, further detail of section 7 and 8 usage.

2.0 REFERENCE DOCUMENTATION

2.1 "DLDSGN USERS GUIDE" by Ken Williams (Salem Systems Software Support Group, Real-Time Team).

2.2 RSX11-M System Generation and Management Guide, number AA-H625A-TC.

2.3 RSX11-M Utilities Manual, number AA-H268A-TC.

2.4 RSX11-M/M+ MCR Operations Manual, number AA-H263A-TC.

3.0 MINIMUM HARDWARE REQUIREMENTS

3.1 32KW of memory, memory management, and at least one supported system disk.

NOTE: RSX11-M DLD DOES NOT SUPPORT DUAL PORT DISK CONFIGURATIONS.

4.0 SOFTWARE REQUIRED

4.1 System image on magtape or disk.

4.1.1 For example: If you are using an RP06 as a system disk, you must use an RP06 image tape or an RP06 disk pack with the DLD on it.

4.2 "DSCS8" utility program on disk or magtape. "DSCS16" on magtape only.

4.2.1 You MUST use "DSCS16" if you are using a TS11, or any other tape device that uses a recording density of 1600 BPI exclusively .

NOTE: REFER TO APPENDIX "B" FOR DEVICES SUPPORTED BY EACH "DSC".

4.3 "BAD" utility program on disk or "BADSYS" utility program on magtape .

4.4 "DLD" software available from SALEM SYSTEMS SOFTWARE SUPPORT GROUP. (REAL-TIME TEAM)

5.0 SPECIAL INSTRUCTIONS

5.1 Ensure that the media used, matches the DISK type being used as the SYSTEM DISK.

NOTE: Magtape system image media is NOT BOOTABLE, therefore you must use one of the "DSC" utility programs to copy the image tape to the SYSTEM DISK.

5.2 Refer to section 7.1 pages 4 thru 8 for disk to disk sysgen flowchart.

5.3 Refer to section 7.2 pages 9 thru 14 for magtape to disk sysgen flowchart.

5.4 Refer to section 8.1 pages 16 thru 33 for disk to disk sample sysgen.

5.5 Refer to section 8.2 pages 34 thru 42 for magtape to disk sample sysgen.

6.0 SOFTWARE SET-UP INSTRUCTIONS

6.1 Ensure that the Distribution Media is protected from accidental erasure.

6.2 The system should be powered up with the CPU halted.

6.3 All turn-around connectors should be removed from any and all COMM. GEAR.

7.0 SYSGEN AND UETP FLOW CHARTS

7.1 RSX11M V3.2 DLD SYSGEN FROM DISK TO DISK

INSTALL DISTRIBUTION MEDIA IN DISK DRIVE AND BOOT

7.1.1 **BADDISK**

USE INDIRECT COMMAND FILE TO LOCATE BAD BLOCKS ON SYSTEM DISK.

@[2,300]BADDISK

7.1.2 **DSCS8/DSCS16**

ASSIGN NON-STANDARD ADDRESSES AND VECTORS. COPY DISTRIBUTION MEDIA TO SYSTEM DISK. REFER TO PG.24 IN "DLD-SGN USERS GUIDE" AND APPENDIX IN THIS DOCUMENT.

BOO [1,51]DSCS8 (or DSCS16)

REMOVE DISTRIBUTION MEDIA

7.1.3 **BOOT SYSTEM DISK**

HARDWARE BOOT THE SYSTEM DISK.

7.1.4

START DLD SYSGEN

TYPE @DLDSGN TO START SYSTEM GENERATION.

7.1.5

REBUILD DEVICE DRIVERS

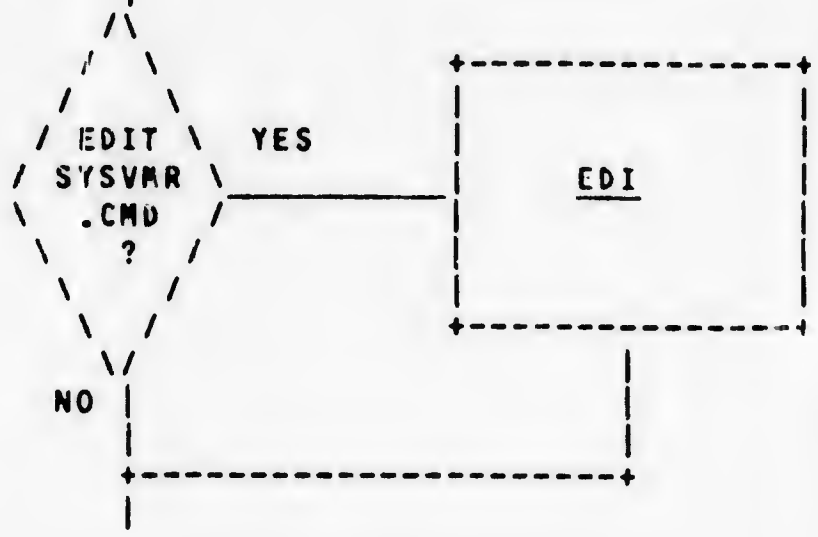
REFER TO PG. 38 IN "DLDSGN USERS GUIDE" FOR PRE-BUILT DRIVER PARAMETERS. REBUILD ANY DRIVERS THAT DIFFER FROM LIST.

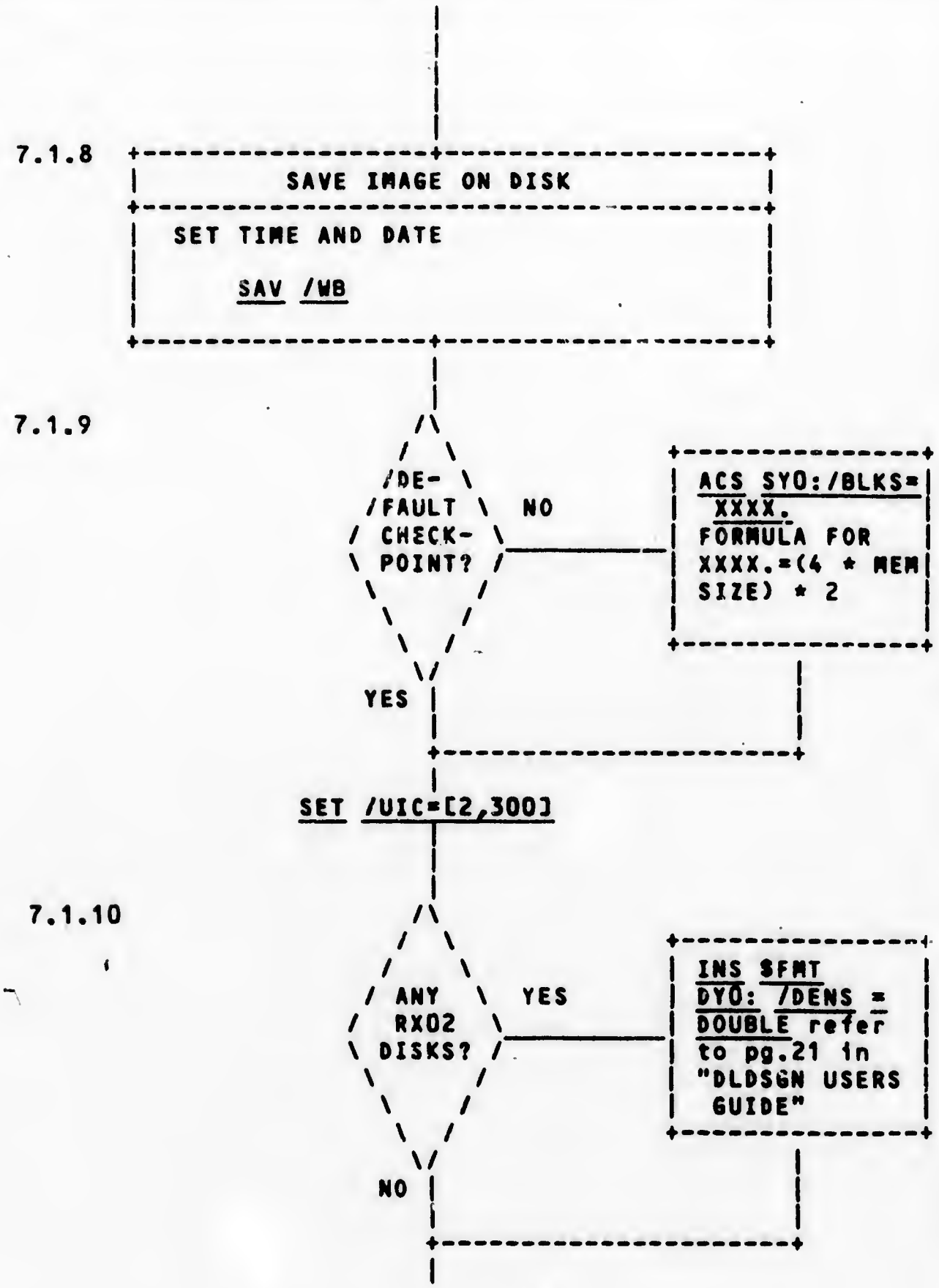
7.1.6

ENTER DEVICES THAT DID NOT NEED TO BE REBUILT IN 7.1.5

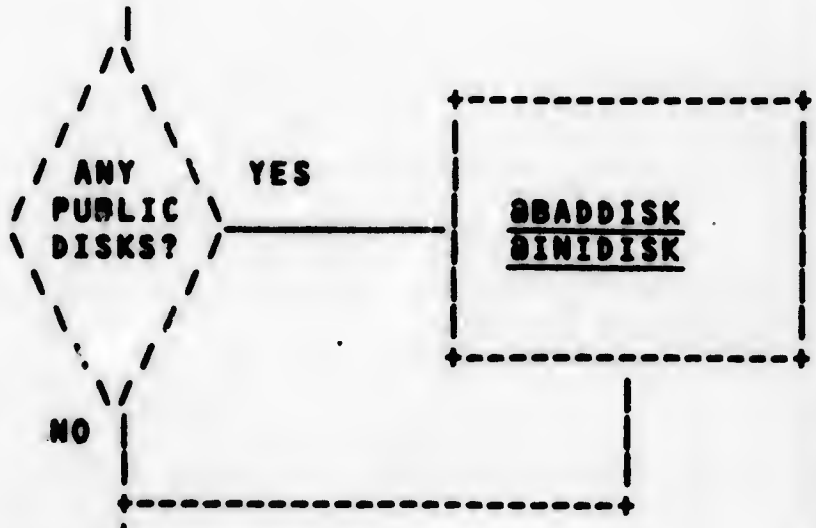
CONSULT CONFIGURATION SHEET FOR EXISTING DEVICES.

7.1.7




7.1.8
SAVE IMAGE ON DISK
SET TIME AND DATE
SAV /WB
7.1.9
/DE- \
/FAULT \ NO
/ CHECK- \
\ POINT? /
\ /
\/
YES
ACS SY0:/BLKS=XXXX.
FORMULA FOR XXXX.=(4 * MEM SIZE) * 2
SET /UIC=[2,300]
7.1.10
/ ANY \ YES
/ RX02 \
\ DISKS? /
\ /
\/
NO
INS $FMT DY0: /DENS = DOUBLE refer to pg.21 in "DLDSGN USERS GUIDE"

7.1.11



7.1.12

DELETE ERROR LOG

TYPE ERF
PIP TI: [1,6]*.*;*/DE
RUN ERRLOG

7.1.13

START U.E.T.P.

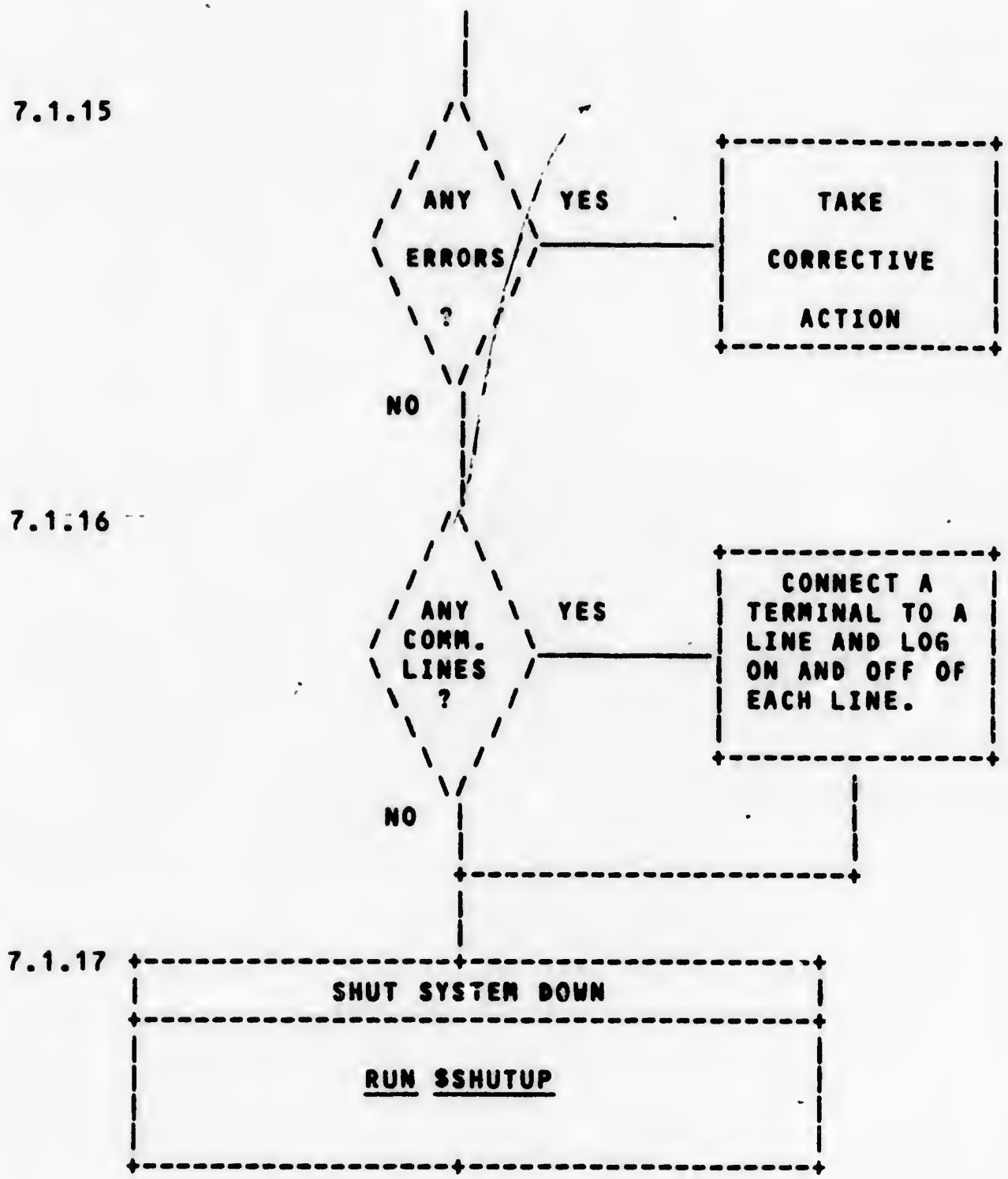
TYPE @DLDUETP

RUN U.E.T.P. FOR EIGHT HOURS OR TWO PASSES MINIMUM.

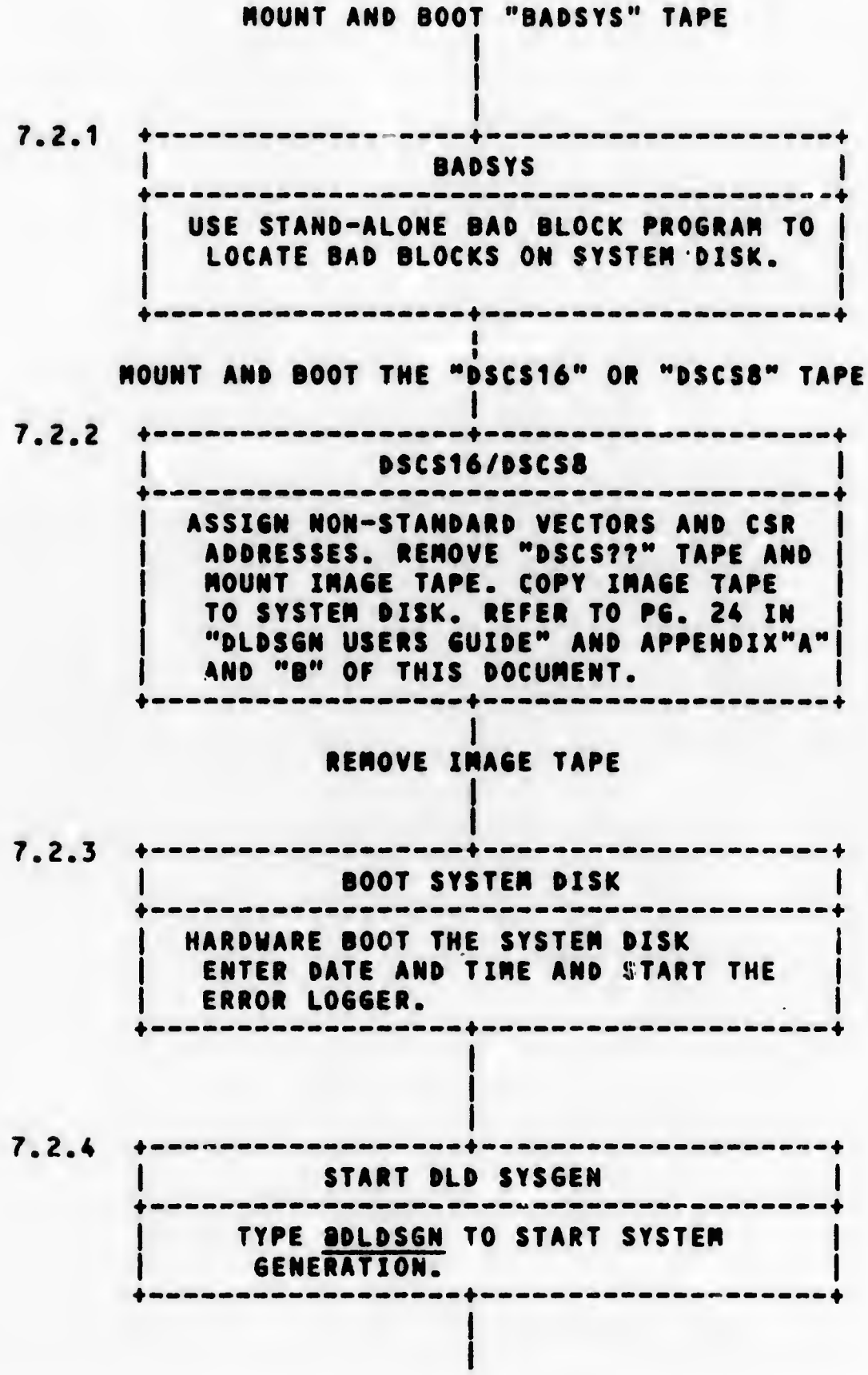
7.1.14

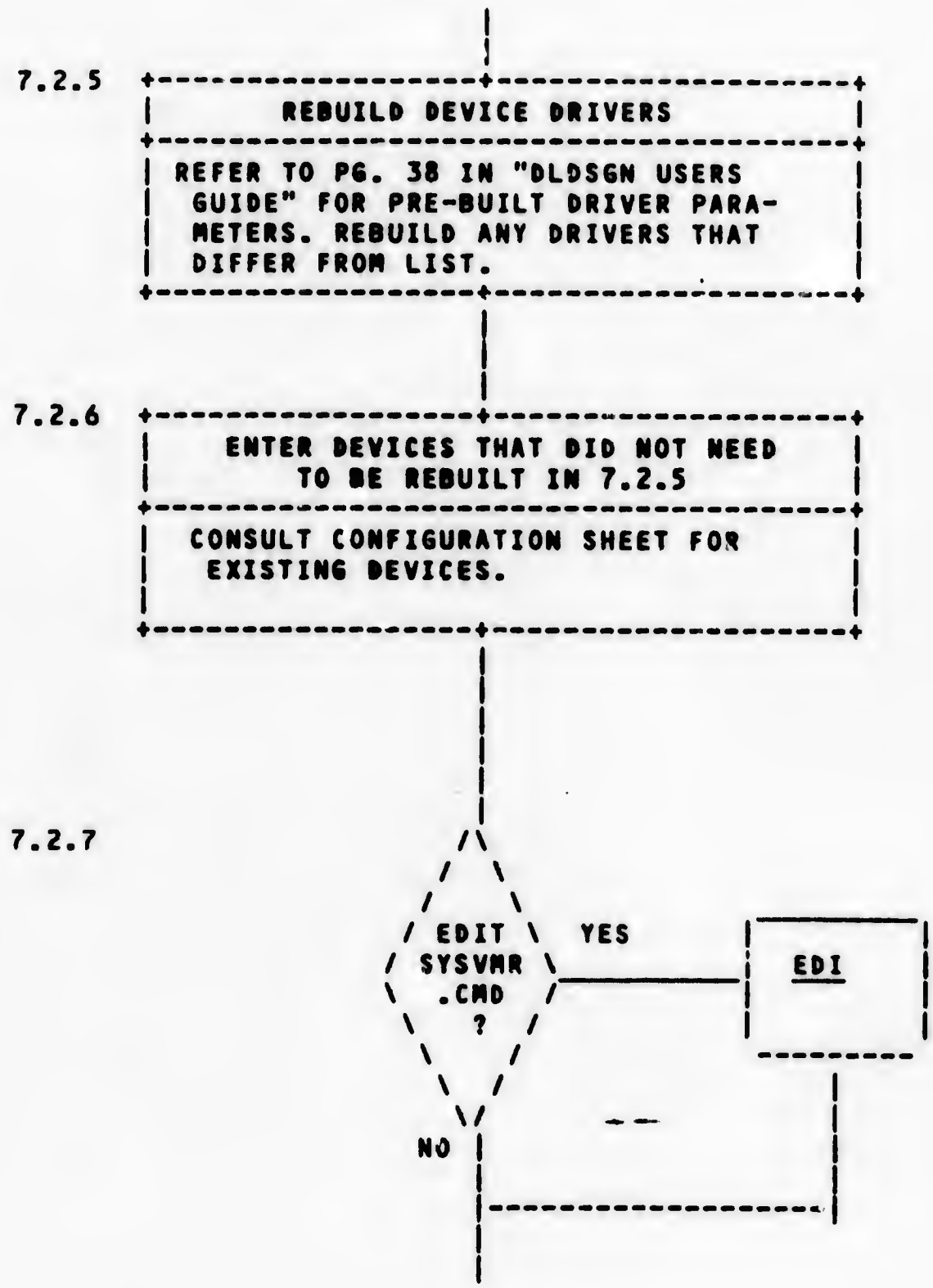
CHECK FOR ERRORS

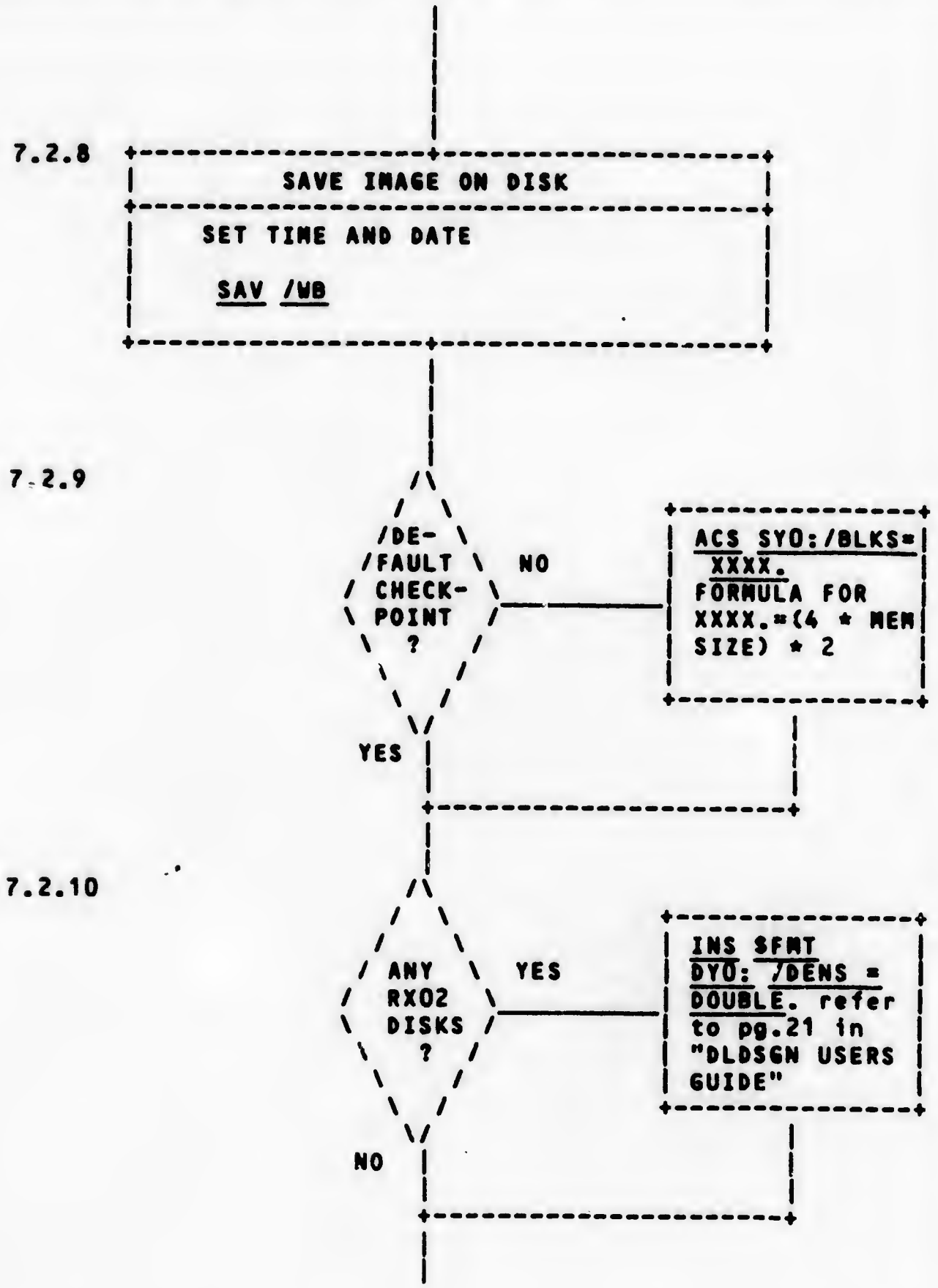
IF U.E.T.P. HAS COMPLETED THE REQUESTED AMOUNT OF PASSES, TYPE :
PIP TI:=[2,300]ERRLOG.LST
IF NOT, TYPE:
SET /UIC=[1,6]
THEN RUN "PSE" AND "SYE"
" refer to pg.27 in "DLOSGN USERS GUIDE"

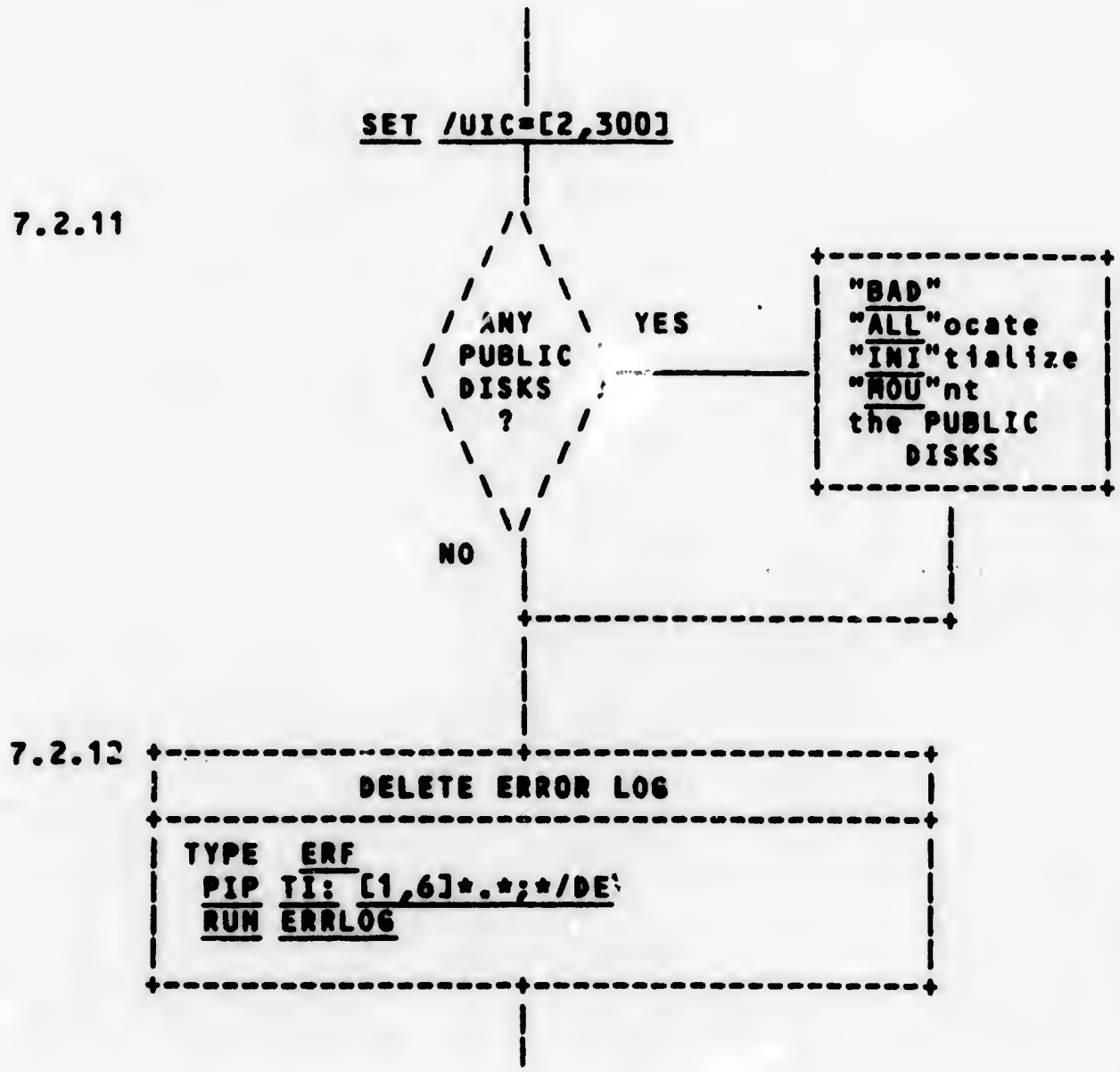

7.1.15
ANY ERRORS ?
YES
TAKE CORRECTIVE ACTION
NO
7.1.16
ANY COMM. LINES ?
YES
CONNECT A TERMINAL TO A LINE AND LOG ON AND OFF OF EACH LINE.
NO
7.1.17
SHUT SYSTEM DOWN
RUN $SHUTUP

7.2 RSX11-M DLD V3.2 FOR TAPE TO DISK




7.2.5
REBUILD DEVICE DRIVERS
REFER TO PG. 38 IN "DLDSGN USERS GUIDE" FOR PRE-BUILT DRIVER PARAMETERS. REBUILD ANY DRIVERS THAT DIFFER FROM LIST.
7.2.6
ENTER DEVICES THAT DID NOT NEED TO BE REBUILT IN 7.2.5
CONSULT CONFIGURATION SHEET FOR EXISTING DEVICES.
7.2.7
EDIT SYSVMR .CMD ?
YES
EDI
NO


7.2.8
SAVE IMAGE ON DISK
SET TIME AND DATE
SAV /WB
7.2.9
/DE- FAULT CHECK- POINT ?
NO
ACS SYO:/BLKS= XXXX.
FORMULA FOR XXXX.=(4 * MEM SIZE) * 2
YES
7.2.10
ANY RX02 DISKS ?
YES
INS $FMT DYO: /DENS = DOUBLE. refer to pg.21 in "DLDSGN USERS GUIDE"
NO


SET /UIC=[2,300]
7.2.11
ANY PUBLIC DISKS ?
YES
"BAD" "ALL"ocate "INI"tialize "MOU"nt the PUBLIC DISKS
NO
7.2.12
DELETE ERROR LOG
TYPE ERF
PIP TI: [1,6]*.*;*/DE
RUN ERRLOG

7.2.13 ANY DVS 11's TO TEST?

YES

MOUNT "DVS" TAPE.
FLX SY0: =
MM0:*.*
@DVS
RUN U.E.T.P.

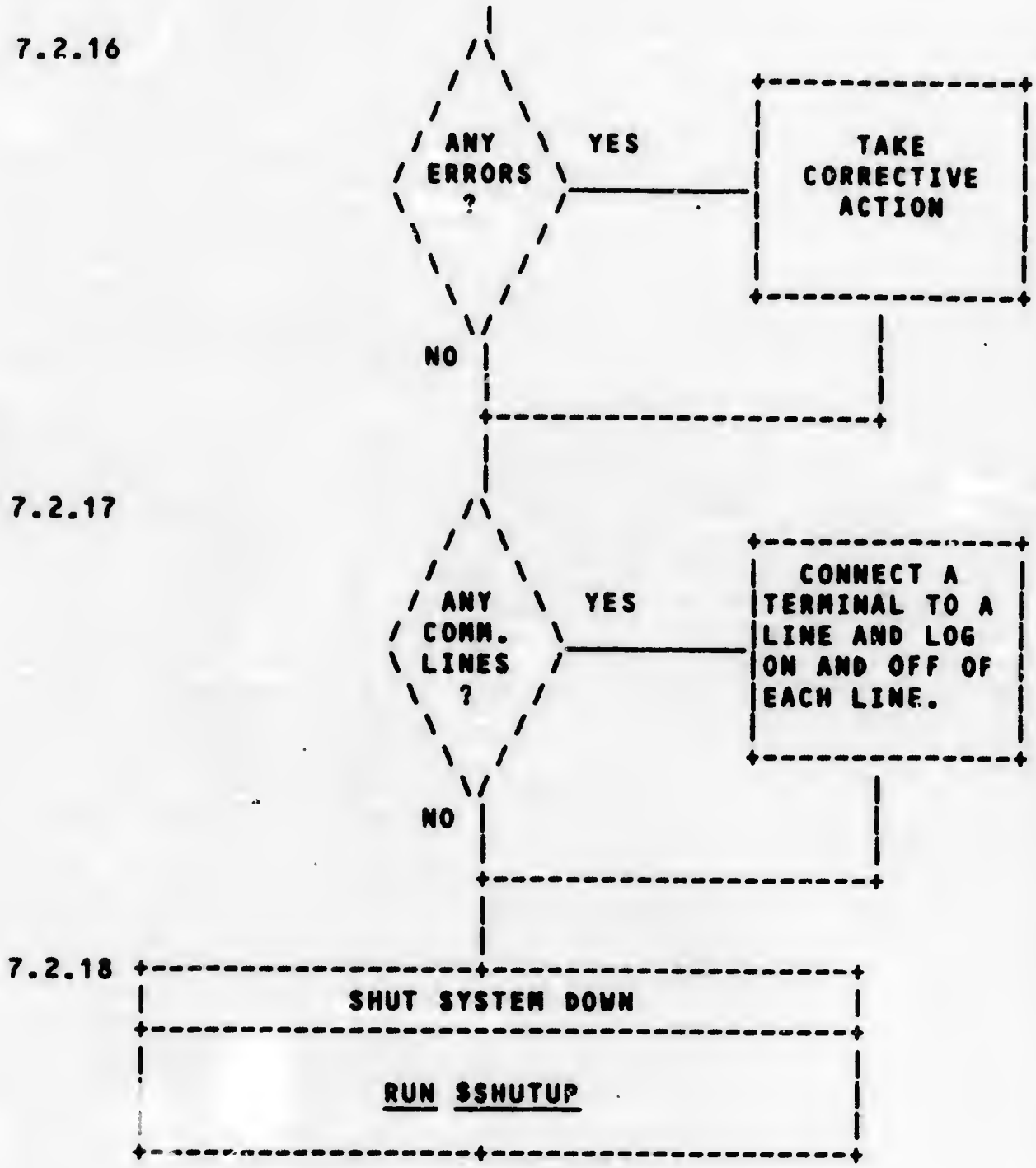
NO

7.2.14 START UETP

@DLDUETP
RUN U.E.T.P. FOR EIGHT HOURS OR TWO PASSES MINIMUM

7.2.15 CHECK FOR ERRORS

IF U.E.T.P. HAS COMPLETED THE REQUESTED AMOUNT OF PASSES, TYPE:
PIP TI:=[2,300]ERRLOG.LST
IF NOT, TYPE:
SET /UIC=[1,6]
THEN RUN "PSE" AND "SYE" refer to pg. 27 in "DLDSGN USERS GUIDE."


7.2.16
ANY ERRORS ?
YES
TAKE CORRECTIVE ACTION
NO
7.2.17
ANY COMM. LINES ?
YES
CONNECT A TERMINAL TO A LINE AND LOG ON AND OFF OF EACH LINE.
NO
7.2.18
SHUT SYSTEM DOWN
RUN SSHUTUP

8.0 SAMPLE SYSGENS AND UETP PRINTOUTS

8.1 This section starts on the next page. The text is printed with reduced character size and spacing due to space restrictions on the MANUFACTURING SPEC. paper.

8.2 These are SAMPLES ONLY, your particular SYSGEN may be different.

8.1 RSX11-M DLD SYSGEN FROM DISK TO DISK

NOTE: This example was generated for an 11/34, with 124KW of memory, 2 RL02 disk drives, 2 RX02 disk drives and 2 DZ11's. User responses are underlined. Explanatory comments are on the right hand margin.

```
@DL1 <CR>                                          hardware boot the
                                                   distribution media

 RSX-11M V3.2 BL26   124K   MAPPED                 rsx identification
                                                   header
>RED DL1:=SY:
>RED DL1:=LB:
>MOU DL1:DLDBL26

@[1,2]DLDSTART.CMD
>* Please enter time and date (DD-MMM-YY HH:MM) [S]: <CR>      not necessary here


>TIM
08:35:52 25-MAR-80
>INS $BIGMAC/PAR=GEN
>INS $BIGTKB/PAR=GEN
>INS $ERL
>INS $ERF
>* Do you want to run the Errorlogger? [Y/N]:N <CR>          not necessary here


>@ <EOF>                                           at this point the
                                                   operating system
                                                   waits for a response
                                                   from you
```

```
>@[2,300]BADDISK <CR>
>;
>;
>* How many disks do you want to BAD [D R:1.-17. D:1.]: <CR>
>INS $BAD/TASK=...BA1
>* Disk to run BAD on [S R:3-5]: DL0 <CR>

>[A1 DL0:
>@ <EOF>
BAD — DL0: TOTAL BAD BLOCKS- 1.

>BOO [1,51]DSCS8 <CR>

RSX11S V2.2 BL26   DISK SAVE AND COMPRESS UTIL.TY V 3.0

DSCS8>DL0:/VEC=160 <CR>

DSCS8>DL0:=DL1: <CR>

DSCS8>

  @DL <CR>

  RSX-11M V3.2 BL26   124K   MAPPED
>RED DL:=SY:
>RED DL:=LB:
>MOU DL:DLDBL26
@[1,2]DLDSTART.CMD
```

[STEP 1]
this command file will allow you to check your disks for bad blocks

disk mnemonics:
DB = RP04/05/06
DK = RK05
DL = RL01/02
DM = RK06/07
DR = RM02/03
DX = RX01
DY = RX02

[STEP 2]
refer to APPENDIX B for proper DSC to use. refer to APPENDIX A for device vectors and addresses. boot in the DSC program

assigns RL02 vector to 160

copies dist. media on DL1 to DL0

refer to pg.24 in "DLDSGN USERS GUIDE" for more information on DSC.

[STEP 3]
hardware boot the system disk

```
>* Please enter time and date (DD-MMM-YY HH:MM) [S]: 08:37 25-MAR-80 <CR>    24 hr.  format
>TIM 08:37 25-MAR-80
>INS $BIGMAC/PAR=GEN
>INS $BIGTKB/PAR=GEN
>INS $ERL
>INS $ERF
>* Do you want to run the Errorlogger? [Y/N]:Y <CR>                          always "YES" during
                                                                             sysgen session
>RUN ERRLOG
>@ <EOF>
>
ERL -- ERROR LOG INITIALIZED



>RDLDSGN <CR>                                                               [STEP 4]
                                                                             this command starts
                                                                             the sysgen session

>TIM
08:25:51 25-MAR-80
>;
>; Dynamic Loadable Driver Sysgen.                                          Typing a <CR> in
                                                                             response to a
                                                                             question, results in
                                                                             a "NO" or the
                                                                             default answer for
                                                                             that question.
>;
>; By Ken Williams      2/29/80
>;
>; Dept:  Salem Manufacturing Product Support
>;
>SET /UIC=[1,54]
>* Is this an RL01 system? [Y/N]: <CR>
>* Does this system have the Floating Point Unit? [Y/N]: <CR>                consult sytems tech
>* Do you want long dialogue ? [Y/N]: <CR>
>PIP [11,10]RSXMC.MAC;*/DE/NM
>PIP [1,24]RSXBLD.CMD;*/DE/NM,RSX11M.OLB;*
>PIP [1,34]RSX11M.MAP;*/DE/NM
>PIP [11,10]/FO=[1,54]RSXMC.MAC
>PIP [1,24]/FO=[1,54]RSXBLD.CMD,RSX11M.OLB
>PIP [1,34]/FO=[1,54]RSX11M.MAP
>;
```

```
>;       Begin Peripheral Options.
>;
>* Expanded comments desired for peripheral options? [Y/N]: <CR>
>SET /UIC=[1,54]
>* Are you running on a system with a line printer? [Y/N]: <CR>
>* Assemb'y listing files desired? [Y/N]: <CR>
>* Task builder map(s) desired? [Y/N]: <CR>
>PIP [11,10]DLDMCO.MAC;*/DE/NM,DLDMC;*
>PIP [11,24]DLDASM.CMD;*/DE/NM
>PIP [1,24]DLDBLD.CMD;*/DE/NM,DLDLBR;*
>* Which device driver do you want to rebuild [S]: TT <CR>          [STEP 5]

>* Do you have any DH11's? [Y/N]: <CR>
>* Do you have any DJ11's? [Y/N]: <CR>
>* Do you have any DZ11's? [Y/N]:Y <CR>
>;
>; If you have an LA120 or LA180S, you must answer Yes to the next
>; question.
>;
>* Do you want form feeds passed directly to terminals? [Y/N]: <CR>
>;
>; Include console in the answer to the next question.
>;
>* Enter number of DL11 line interfaces [D R:1.-16. D:1.]: <CR>
>* Enter vector address of the first DL11 [O R:60-774 D:60]: <CR>
>* What is its CSR address? [O R:160000-177700 D:177560]: <CR>
>* Enter number of DZ11 asynchronous multiplexers [D R:1.-16. D:1.]: 2 <CR>
>* Do any of the lines require modem support? [Y/N]: <CR>
>* Enter vector address of the first DZ11 [O R:300-774]: 300 <CR>
>* What is its CSR address? [O R:160010-177700]: 160010 <CR>
>* How many lines does it have? [D R:1.-8. D:8.]: <CR>
>* Enter vector address of the next DZ11 [O R:300-774]: 310 <CR>
>* What is its CSR address? [O R:160010-177700]: 160020 <CR>
>* How many lines does it have? [D R:1.-8. D:8.]: <CR>
>* Which device driver do you want to rebuild [S]: <CR>
```

For an explanation of each question individually, press the <ESC> or <ALT> key in response to the question.

consult systems tech for device addresses and vectors.

type <CR> if you have no more drivers to be rebuilt.

```
>PIP [11,10]DLDMC.MAC/FO=[11,10]RSXMC.MAC,DLDMCO.MAC,RSXMCO.MAC
>SET /UIC=[11,24]
>TIM
08:27:52 25-MAR-80
>MAC @DLDASM
>TIM
08:29:20 25-MAR-80
>SET /UIC=[1,24]
>PIP [11,34]*.*/PU/NM
>TKB @[1,24]DLDBLD
>PIP [11,24]*.OBJ;*/DE/NM
>PIP [1,34]*.MAP/PU/NM
>SET /UIC=[1,54]

>* Do you have any Card Readers? [Y/N]: <CR>

>* Do you have any TA11 Cassettes? [Y/N]: <CR>
>* Do you have any RJP/RWP04/05/06's? [Y/N]: <CR>
>* Do you have any TU58's? [Y/N]: <CR>
>* Do you have any RF11's? [Y/N]: <CR>
>* Do you have any RK11/RK05's? [Y/N]: <CR>
>* Do you have any RK611/RK06/RK07's? [Y/N]: <CR>
>* Do you have any RP11/RPRC2/RP03's? [Y/N]: <CR>
>* Do you have any RJ/RWK02/03's? [Y/N]: <CR>
>* Do you have any RJS/RWS03/04's? [Y/N]: <CR>
>* Do you have any TC11/TU56's? [Y/N]: <CR>
>* Do you have any RX11/RX01 Floppy's? [Y/N]: <CR>
>* Do you have any RX211/RX02 Floppy's? [Y/N]:Y <CR>
>* Do you have any LP11/LS11/LV11/LA180's? [Y/N]: <CR>
>* Do you have any TJU/TWU16/TE16/45/77's? [Y/N]: <CR>
>* Do you have any,TS11/TS04'S? [Y/N]: <CR>
>* Do you have any TM11/TU10/TE10/TS03's? [Y/N]: <CR>
>* Do you have a PC11 (Paper Tape Reader/Punch)? [Y/N]: <CR>
>* Do you have a PR11 (Paper Tape Reader)? [Y/N]: <CR>
>;
>; The FCP which will be used is MIDDLE.
>;
>* Do you want to set up the terminals? [Y/N]:Y <CR>
>* Do you want to set up all the terminals the same? [Y/N]:Y <CR>
>;
>; Note: DZ11 lines must have both the receiver & the transmitter
>;       baud rates set up the same speed.
>;
>; Your first local terminal is TT1:
>; Your last local terminal is TT20:
```

[STEP 6]
if you have built a driver for each device on your system, you can hit <ESC> to bypass this section.

```
>* Do you want the default values? [Y/N]: <ESC>
>;
>; The default values are VT52, 80. characters per line,
>; 9600:9600 baud rate, and lower case enabled.
>;
>* Do you want the default values? [Y/N]:Y <CR>
>PIP [1,54]SYSVMR.CMD;*/DE/NM
>;
>; [1,54]SYSVMR.CMD will now be created.
>;
>INS SVMR
>PIP [1,54]SYSVMR.CMD=[200,200]TTY.CMD/AP
>SET /UIC=[1,54]
>* Enter size in K words for the system image? [D R:48.-124. D:48.]: <CR>
>PIP [1,54]RSX11M.SYS/NV/CO/BL:194.=[1,54]RSX11M.TSK
>* Do you wish to edit [1,54]SYSVMR.CMD? [Y/N]: <CR>
>;
>;
>; VMR is now being performed.
>;
>VMR @[1,54]SYSVMR.CMD
VMR -- INSTALLED TASKS MAY NO LONGER FIT IN PARTITION
SET /TOP=DRVPAR:-*
>;
>; The account UETP; password UETP; has been set up.
>;
>BOO RSX11M


RSX11M V3.2 BL26

>TIM 09:02 25-MAR-80 <CR>


>SAV /MB <CR>
```

type <ESC> if you want to see the default values

[STEP 7]
usual answer is "NO or <cr>. only answer "YES" if you want to change partition sizes,install additional tasks,etc..

normal warning

at this point the new executive is booted automatically,and waits for a response from you.

[STEP 8]
set the correct time and date

this command will save and boot the new system image.

```
 RSX-11M V3.2 BL26   124K   MAPPED
```

ensure memory size is correct.

```
>RED DL:=SY:
>RED DL:=LB:
>MOU DL:DLDBL26
>@[1,2]STARTUP
>* Please enter time and date (DD-MMM-YY HH:MM) [S]: <CR>
```

if you entered the correct time in step 8, it is not necessary to do so again.

```
>TIM
09:02:17 25-MAR-80
>SET /SYSUIC=[1,54]
>INS $BIGMAC /PAR=GEN
>INS $BIGTKB /PAR=GEN
>PIP SY:/FR

DL0: HAS 3773. BLOCKS FREE, 16707. BLOCKS USED OUT OF 20480.
LARGEST CONTIGUOUS SPACE = 2422. BLOCKS

>* Do you want the default checkpoint file size [992]? [Y/N]:Y
```

[STEP 9]
use default checkpoint file size, ONLY if the number of contiguous blocks is greater than the default size

```
>ACS SY:/BLKS=992.
>RUN ERRLOG
>BRO ALL:RSX11M IS NOW ON THE AIR !!!!!
ERL -- ERROR LOG INITIALIZED
>@ <EOF>
>
>SET /UIC=[2,300] <CR>
```

this is the account that U.E.T.P. resides in

```
>INS $FMT <CR>
```

[STEP 10]
this installs the format task

```
>FMT <CR>
```

this runs the format task

```
FMT>DY0:/DENS=DOUBLE <CR>
```

this tells the FMT task that you are formatting RX02's refer to pg. 21 in "DLDSGN USERS GUIDE".

```
FMT>DY1:/DENS=DOUBLE <CR>
```

```
^Z <CTRL Z>                                          this exits the FMT
                                                     task

>@BADDISK <CR>                                       [STEP 11]
                                                      check for bad
                                                     blocks on remaining
                                                     disks

>; Bad the Disk Command File
>;
>* How many disks do you want to BAD [D R:1.-17. D:1.]: 3 <CR>
>INS SBAD/TASK=...BA1
>INS SBAD/TASK=...BA2
>INS SBAD/TASK=...BA3
>* Device to run BAD on [S R:3-5]: DL1 <CR>
>BA1 DL1:
>* Device to run BAD on [S R:3-5]: DY0 <CR>
>BA2 DY0:
>* Device to run BAD on [S R:3-5]: DY1 <CR>
>BA3 DY1:
>@ <EOF>
BAD -- DL1: TOTAL BAD BLOCKS- 0.
BAD -- DY0: TOTAL BAD BLOCKS- 0.
BAD -- DY1: TOTAL BAD BLOCKS- 0.

>@INIDISK <CR>                                       [STEP 12]
                                                     this command file
                                                     allows you to
                                                     initialize the
                                                     remaining disks

>; Disk Initializing Command file
>;
>; Please enter the name of the disk to be initialized
>; type a <RETURN> when all disks have been entered.
>* what disk is to be initialized [DDN:] [S]: DL1 <CR>
>ALL DL1:
>INI DL1:SCRATCH/INDX=BEG/BAD=AUTO]
>* what disk is to be initialized [DDN:] [S]: DY0 <CR>
>ALL DY0:
>INI DY0:SCRATCH/INDX=BEG/BAD=[AUTO]
>* what disk is to be initialized [DDN:] [S]: DY1 <CR>
>ALL DY1:
>INI DY1:SCRATCH/INDX=BEG/BAD=[AUTO]
>* what disk is to be initialized [DDN:] [S]: <CR>
>;
>;* Do you want to run a quick pass of IOX (the I/O exerciser)
>* on the disks that have just be initialized ? [Y/N]:Y <CR>          optional
>* How many minutes do you want it to run [0 R:0-5 D:1]: <CR>
>* Do you want to run IOX on any other devices? [Y/N]:Y <CR>
>; Please enter the name of the device to be tested;
>; type a <RETURN> when all the devices have been entered.
>* What device is to be tested [S]: DL0 <CR>
>* What device is to be tested [S]: <CR>
```

```
MOU DL1:/OVR                                                    the disks are
                                                                mounted
                                                                automatically.
>MOU DY0:/OVR
>MOU DY1:/OVR
>MOU DL0:/OVR
>IOX @DISKTEST
IOX -- UNIT ALREADY CONFIGURED
IOX -- UNIT ALREADY CONFIGURED

IOX -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 08:41:01
  TIME -- RUN: 1 MIN.   ELAPSED: 1 MIN.   REMAINING: 0 MIN.
  DL0: -- 1,992. REQUESTS TOTALING 1,992. BLOCKS WITH NO ERRORS
  DL1: -- 1,985. REQUESTS TOTALING 1,985. BLOCKS WITH NO ERRORS
  DY0: --   546. REQUESTS TOTALING   546. BLOCKS WITH NO ERRORS
  DY1: --   492. REQUESTS TOTALING   492. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 199. ITERATIONS

A C C U M U L A T E D   T O T A L S :
- - - - - - - - - - -   - - - - - - -
  TIME -- RUN: 1 MIN.   ELAPSED: 1 MIN.   REMAINING: 0 MIN.
  DL0: -- 1,993. REQUESTS TOTALING 1,993. BLOCKS WITH NO ERRORS
  DL1: -- 1,985. REQUESTS TOTALING 1,985. BLOCKS WITH NO ERRORS
  DY0: --   546. REQUESTS TOTALING   546. BLOCKS WITH NO ERRORS
  DY1: --   492. REQUESTS TOTALING   492. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 199. ITERATIONS


>DMO DL1:                                                       the disks are
>DMO DY0:                                                       dismounted auto-
>DMO DY1:                                                       matically.
>DMO DL0:
>;
>@ <EOF>                                                        at this point the
                                                                operating system
                                                                waits for a response
                                                                from you.
```

```
>@DLDUETP                                                    [STEP 13]
                                                             this will start the
                                                             U.E.T.P. session
>;
>;      **********************************************************
>;      *                                                        *
>;      *   RSX-11M INSTALLATION VERIFICATION PACKAGE            *
>;      *                                                        *
>;      **********************************************************
>;
>SET /UIC=[2,300]
>RUN ERRLOG
>
>;
>* DO YOU WISH TO RUN RMDEMO? [Y/N]: <CR>
>;
>* ENTER VERSION OF UETP TO BE RUN (SAM, SUB, MFG, ENG) [S]: MFG <CR>    always MFG
>* ENTER UNIT NUMBER OF TERMINAL [S]: 0 <CR>
>;
>;
>* ENTER INPUT DEVICE (DDNN) OR <CR> [S]: <CR>                  press <cr> if UETP
                                                                resides on system
                                                                disk.
>;
>;
>;
>;
>;                **** NOTE ****
>;
>; TEST MEDIA MUST BE LOADED ON ALL TAPE AND DISK DRIVES.  USE SCRATCH TAPES
>; AND FILES-11 FORMAT DISKS.
>;
>; ALL MAGTAPES BEING TESTED ARE OVER-WRITTEN.  THE DISKS ARE
>; TESTED WITH FILE-STRUCTURED I/O WITH NO NEGATIVE EFFECT ON DATA
>; OR STRUCTURE.
>;
>; BEFORE PERFORMING THE FILE-STRUCTURED I/O TEST, ALL UNMOUNTED
>; DISKS ARE MOUNTED AUTOMATICALLY.
>;
>* DO YOU NEED TO INITIALIZE ANY DISKS? [Y/N]: <CR>             if you forgot to
                                                                INIT any disks, type
                                                                "YES".
>;
>TIM
09:10:31 25-MAR-80
```

```
>;ONE COMPLETE PASS OF THIS UETP WILL TAKE 4 HOURS
>;
>* HOW MANY PASSES DO YOU WISH TO RUN [D R:1.-6. D:1.]: 2 <CR>

>;
>;THE 2 PASS(ES) YOU HAVE SELECTED, WILL TAKE 8 HOURS TO RUN.
>;

>; NEEDED UTILITIES WILL BE INSTALLED NOW.
>; **********
>; ************************************************************
>PIP TAILOR.DAT=DEVM.SAV/AP
>MAC DEFINE=LB:[11,10]DLDMC.MAC/PA:1,SY:[2,300]DEFINE
>TKB DEFINE/PR/CP=DEFINE,LB:[1,54]RSX11M.STB,[1,1]EXELIB/LB
>INS DEFINE/TASK=DEFINE
>PIP *.*/PU
>RUN DEFINE
>;
>;START OF UETP PASS #1
>;
>;
>;
>;       * CPU-BOUND LOAD TEST *
>;
>INS DUMMY/TASK=DUM00/PRI=40.
>INS LOGGER/TASK=LOG00
>INS QTRUN /TASK=QTR00
>RUN DUM00
>;
>; FOR THE NEXT FEW MINUTES A NUMBER OF COMPUTE-BOUND TASKS WILL BE
>; EXERCISING THE MEMORY, THE MULTI-TASKING CAPABILITIES OF THE
>; SYSTEM AND, IF INCLUDED IN THIS SYSTEM, THE ROUND-ROBIN SCHEDULER,
>; THE SHUFFLER AND CHECKPOINTING.  THE ACTION OF THESE LAST THREE
>; FEATURES CAN BE SEEN ON THE RMDEMO SCREEN.  IF THE SYSTEM IS
>; PERFORMING PROPERLY, ALL OF THE "GEN" PARTITION IS USED AND THE "QT"
>; TASKS ARE SHARING SYSTEM RESOURCES IN A MANNER CONSISTENT
>; WITH THE FEATURES AVAILABLE.  NOTE THAT CHECKPOINTING IS DISABLED
>; FOR THE SECOND HALF OF THE TEST.
>;
>;       *** THIS TEST RUNS FOR A MAXIMUM OF 120. MINUTES ***
>;
>RUN QTR00
>
>TIM
09:11:27 25-MAR-80
>INS NUL2/TASK=QT0000
>INS NUL2/TASK=QT0100
>INS NUL2/TASK=QT0200
>INS NUL2/TASK=QT0300
```

	SIZE	CODE	NUMBER	REV
	A	SP	MA-E1000-0-0	A

at least 2 passes for minimum MAST requirements

AT THIS POINT THE U.E.T.P. WILL RUN UNATTENDED FOR 2 PASSES OR 8 HOURS.

```
>;      >>>>>> THE LOAD TEST IS RUNNING <<<<<<
>TIM
11:11:22 25-MAR-80
>REM QT0000
>REM QT0100
>REM QT0200
>REM QT0300
>;
>;       * TEST COMPLETED *
>;
>;
>;
>;       * SYSTEM I/O EXERCISER *
>;
>; THE FOLLOWING DEVICES HAVE BEEN GENERATED INTO YOUR SYSTEM.  THOSE
>; LISTED AS "OFFLINE" ARE NOT PHYSICALLY PRESENT AND ARE NOT
>; TESTED.  INDIVIDUAL MAG TAPE, DEC TAPE AND RK05 UNITS CAN
>; ERRONEOUSLY BE SHOWN AS ONLINE WHEN THE CONTROLLER IS ONLINE.
>; THEY ARE TESTED AND THE TEST FAILS AFTER SEVERAL MINUTES
>; OF ERROR MESSAGES.
>;
>DEV
DL0:      PUBLIC MOUNTED LOADED LABEL=RSX11/APBL6 TYPE=RL02
DL1:      LOADED TYPE RL02
DY0:      LOADED
DY1:      LOADED
CO0:      TT0: LOADED
TT0:      LOADED
TT1:      LOADED
TT2:      LOADED
TT3:      LOADED
TT4:      LOADED
TT5:      LOADED
TT6:      LOADED
TT7:      LOADED
TT10:     LOADED
TT11:     LOADED
TT12:     LOADED
TT13:     LOADED
TT14:     LOADED
TT15:     LOADED
TT16:     LOADED
TT17:     LOADED
TT20:     LOADED
NL0:      LOADED
RD0:      LOADED
TI0:
CL0:      TT0:
LB0:      DL0:
SY0:      DL0:
>;
```

```
>;
>; IF ANY DRIVERS ARE UNLOADED, THEY WILL BE LOADED NOW.
>;
>; **********
>; ************************************************************
>INS $IOX/TASK=...SIO
>;
>MOU DL1:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DL1:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = □
ACP NAME   = F11ACP
>MOU DY0:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DY0:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = □
ACP NAME   = F11ACP
>MOU DY1:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DY1:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = □
ACP NAME   = F11ACP
>;
```

```
>;  THE SYSTEM I/O EXERCISER WILL RUN FOR 120 MINUTES
>;
>TIM
11:12:12 25-MAR-80
>SIO @IOXCNF

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 11:42:14
  TIME -- RUN: 30 MIN.   ELAPSED: 30 MIN.   REMAINING: 90 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 12:12:16
  TIME -- RUN: 30 MIN.   ELAPSED: 60 MIN.   REMAINING: 60 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 12:42:18
  TIME -- RUN: 30 MIN.   ELAPSED: 90 MIN.   REMAINING:30 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 13:12:20
  TIME -- RUN: 30 MIN.   ELAPSED: 120 MIN.   REMAINING: 0 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

A C C U M U L A T E D   T O T A L S :
- - - - - - - - - - - -   - - - - - - -
  TIME -- RUN: 120 MIN.   ELAPSED: 120 MIN.   REMAINING: 0 MIN.
  DL0: -- 103,692. REQUESTS TOTALING 103,692. BLOCKS WITH NO ERRORS
  DL1: -- 100,136. REQUESTS TOTALING 100,136. BLOCKS WITH NO ERRORS
  DY0: -- 41,016. REQUESTS TOTALING 41,016. BLOCKS WITH NO ERRORS
  DY1: -- 41,016. REQUESTS TOTALING 41,016. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 26,680. ITERATIONS
```

```
>REM SIO
>TIM
13:12:54 25-MAR-80
>;
>;        * TEST COMPLETED *
>;
>;
>;END OF UETP PASS #1
>;
>;
>;
>;START OF UETP PASS #2
>;
>;
>;
>;        * CPU-BOUND LOAD TEST *
>;
>RUN DUMOO
>;
>;        *** THIS TEST RUNS FOR A MAXIMUM OF 120. MINUTES ***
>;
>RUN QTROO
>
>TIM
13:13:11 25-MAR-80
>INS NUL2/TASK=QT0000
>INS NUL2/TASK=QT0100
>INS NUL2/TASK=QT0200
>INS NUL2/TASK=QT0300
>;       >>>>>> THE LOAD TEST IS RUNNING <<<<<<
>TIM
15:13:22 25-MAR-80
>REM QT0000
>REM QT0100
>REM QT0200
>REM QT0300
>;
>;        * TEST COMPLETED *
>;
```

```
>;       * SYSTEM I/O EXERCISER *
>;
>; IF ANY DRIVERS ARE UNLOADED, THEY WILL BE LOADED NOW.
>;
>; **********
>; ************************************************************
>INS $IOX/TASK=...SIO
>;
>MOU DL1:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DL1:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = □
ACP NAME   = F11ACP
>MOU DY0:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DY0:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = □
ACP NAME   = F11ACP
>MOU DY1:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DY1:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = □
ACP NAME   = F11ACP
>;
>;  THE SYSTEM I/O EXERCISER WILL RUN FOR 120 MINUTES
>;
>TIM
15:13:57 25-MAR-80
>SIO @IOXCNF
SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 15:43:59
  TIME -- RUN: 30 MIN.   ELAPSED: 30 MIN.   REMAINING: 90 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS
```

```
SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 16:14:01
  TIME -- RUN: 30 MIN.   ELAPSED: 60 MIN.   REMAINING: 60 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 16:44:03
  TIME -- RUN: 30 MIN.   ELAPSED: 90 MIN.   REMAINING: 30 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 17:14:05
  TIME -- RUN: 30 MIN.   ELAPSED: 120 MIN.   REMAINING: 0 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

A C C U M U L A T E D   T O T A L S :
- - - - - - - - - - -   - - - - - - -
  TIME -- RUN: 120 MIN.   ELAPSED: 120 MIN.   REMAINING: 0 MIN.
  DL0: -- 103,692. REQUESTS TOTALING 103,692. BLOCKS WITH NO ERRORS
  DL1: -- 100,136. REQUESTS TOTALING 100,136. BLOCKS WITH NO ERRORS
  DY0: -- 41,016. REQUESTS TOTALING 41,016. BLOCKS WITH NO ERRORS
  DY1: -- 41,016. REQUESTS TOTALING 41,016. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 26,680. ITERATIONS


>REM SIO
>TIM
17:14:23 25-MAR-80

>;
>;       * TEST COMPLETED *
>;
>;
>;END OF UETP PASS #2
>;
>;>;
```

```
>;
>PIP *.DAT;*/DE
>;
>; IF ANY ERRORS HAVE BEEN LOGGED BY ERROR LOGGER, WHEN THE COMMAND FILE
>; EXITS YOU SHOULD PRINT [2,300]ERRLOG.LST AND INVESTIGATE THE ERRORS.
>;
>ERF
ERF -- REQUESTED "ERRLOG" TO STOP LOGGING
>PSE SY:=SY:
ERL -- LOGGING ENDED AFTER 0 ERRORS
>SYE SY:=SY:/-SP
SYE -- 1. PAGES IN REPORT
>;
>RUN ERRLOG
ERL -- ERROR LOG INITIALIZED
>
>;
>;
>;
>; ************************************************************************
>;
>TIM
17:14:53 25-MAR-80
>;
>;                          *** END OF RSX-11M   INSTALLATION VERIFICATION ***
>;
>; ************************************************************************
>
>@ <EOF>
>
>PIP TI:=[2,300]ERRLOG.LST <CR>
```

[STEP 14]
type this to see any errors that have been logged. further information on the ERROR LOGGER can be found on page 27 of the "DLDSGN USERS GUIDE".

8.2 RSX11-M DLD SYSGEN - MAGTAPE TO DISK

NOTE:
This example was generated on an 11/70, with Floating Point, 640K words of MEMORY, a TE16 magtape, an RP06 disk drive and no comm. devices.
User responses are underlined. Explanatory comments on right margin.

```
RSX11S V2.1 BL22     BAD BLOCK LOCATOR

BAD>DB0:/LI/CSR=176700/VEC=254/WCHK <CR>

BAD -- BAD BLOCK FOUND - LBN= 1292.

BAD -- TOTAL NO. OF BAD BLOCKS = 1.

BAD>
```

[STEP 1]
mount and boot "BADSYS" tape

refer to pg. 23 in "DLDSGN USERS GUIDE" for more info. on "BAD".

remove "BADSYS" tape.

```
RSX11S V2.2 BL260 DISK SAVE AND COMPRESS UTILITY V 3.0

DSCS16>MM0: /VEC=224 <CR>
DSCS16>DB0: /VEC=254 <CR>

DSCS16>DB0:=MM0: <CR>

DSC -- *WARNING* 59-DB0:

DSCS16>
```

[STEP 2]
refer to APPENDIX B for proper "DSC" to use. refer to APPENDIX A for device addresses and vectors.
mount and boot a "DSC" tape.

assigns vector add. to devices

copies image tape to disk

refer to pg. 24 in "DLDSGN USERS GUIDE" for more info. on "DSC".

```
 RSX11M V3.2 BL26   124K   MAPPED
```

[STEP 3]
hardware boot the system disk.

```
>RED DB:=SY:
>RED DB:=LB:
>MOU DB:DLDBL26
>@DB:[1,2]STARTUP
>* Please enter time and date ( DD-MMM-YY HH:MM ) [S]: 9-JUN-80 11:06<CR>  24 hr. time format
>TIM 9-JUN-80 11:06
>INS $CDA
>INS $BIGMAC/PAR=GEN
>INS $BIGTKB/PAR=GEN
>INS $ERL
>INS $ERF
>RUN ERRLOG
>@ <EOF>
ERL -- ERROR LOG INITIALIZED


>@DLDSGN <CR>
```

[STEP 4]
this command starts the sysgen session.

```
>TIM
11:06:13 09-JUN-80
>;
>; Dynamic Loadable Driver Sysgen.
```

typing a <CR> in response to a query, results in a "NO " or the default answer for that query.

```
>;
>; By Ken Williams      9/10/79
>;
>; Dept:  Salem Manufacturing Product Support
>;
>SET /UIC=[1,54]
>* Is this an 11/70 system? [Y/N]: Y <CR>
>* Does this system have the Floating Point Unit? [Y/N]: Y <CR>
```

consult systems tech.

```
>INS $LBR
>INS $PIP
>INS $EDI
>* Do you want long dialogue ? [Y/N]: <CR>
```

for an explanation of each question individually, press the <esc> or <alt> key in response to the question.

```
>PIP [11,10]RSXMC.MAC;*/DE/NM
>PIP [1,24]RSXBLD.CMD;*/DE/NM,RSX11M.OLB;*
>PIP [1,34]RSX11M.MAP;*/DE/NM
>PIP [11,10]/FO=[1,57]RSXMC.MAC
>PIP [1,24]/FO=[1,57]RSXBLD.CMD,RSX11M.OLB
>PIP [1,34]/FO=[1,57]RSX11M.MAP
PIP -- NO SUCH FILE(S)
SY0:[1,57]RSX11M.MAP
>;
>;       Bugin Peripheral Options
>;
>* Expanded comments desired for peripheral options? [Y/N]: <CR>
>SET /UIC=[1,54]
>* Are you running on a system with a line printer? [Y/N]: <CR>
>* Assembly listing files desired? [Y/N]: <CR>
>* Task builder map(s) desired? [Y/N]: <CR>
>PIP [11,10]DLDMC0.MAC;*/DE/NM,DLDMC;*
>PIP [11,24]DLDASM.CMD;*/DE/NM                                    [STEP 5]
                                                                  consult systems tech
                                                                  for vectors and
                                                                  addresses.

>PIP [1,24]DLDBLD.CMD;*/DE/NM,DLDBDR;*
>* Which device driver do you want to rebuild [S]: DB <CR>
>* How many RJ/RMP04/5/6 disk pack cont. have you [D R:0.-16. D:1.]: <CR>
>* Enter vector address of the first RJ/RMP04-05-06 [O R:60-774 D:254]: <CR>
>* What is its CSR address? [O R:160000-177700 D:176700]: <CR>
>* How many drives does it have? [D R:1.-8. D:1.]: <CR>
>* Enter physical unit number of the first drive [O D:0]: <CR>
>* Is contr. 0 unit 0 an RP04 or RP05? [Y/N]: <CR>
>* Which device driver do want to rebuild [S]: MM <CR>
>* How many TJ/TMU16-45 magtape cont. do you have [D R:0.-16. D:1.]: <CR>
>* Enter vector address of the first TJ/TMU16-45 [O R:60-774 D:224]: <CR>
>* What is its CSR address? [O R:160000-177700 D:172440]: <CR>
>* How many drives does it have? [D R:1.-8. D:1.]: 2 <CR>
>* Enter physical unit number of the TM03 formatter [O D:0]: <CR>
>* Which device driver do you want to rebuild [S]: <CR>            press <CR> if there
                                                                  are no more drivers
                                                                  to be rebuilt

>PIP [11,10]DLDMC.MAC/FO=[11,10]RSXMC.MAC,DLDMC0.MAC,RSXMC0.MAC
>PIP [1,24]DLDLBR.CMD=[1,24]*.LBR
>PIP [1,24]*.LBR;*/DE/NM
>SET /UIC=[11,24]
```

```
>TIM
11:09:02 09-JUN-80
>MAC @DLDASM
>TIM
11:09:28 09-JUN-80
>SET /UIC=[1,24]
>PIP [11,34]*.*/PU/NM
>LBR @[1,24]DLDLBR
MODULE "DBTAB " REPLACED

MODULE "MMTAB " REPLACED

>TKB @[1,24]DLDBLD
>PIP [11,24]*.OBJ;*/DE/NM
>PIP [1,34]*.MAP/PU/NM
>SET /UIC=[1,54]
>SET /UIC=[1,57]
>* Do you have any Card Readers? [Y/N]: <esc>
```

[STEP 6]
if you have built a driver for each device on your system, you can press <esc> to bypass this section.

```
>;
>; The FCP which will be used is MIDDLE.
>;
>PIP [1,57]SYSVMR.CMD;*/DE/NM
>;
>; [1,57]SYSVMR.CMD will now be created.
>;
>INS SVMR
>SET /UIC=[1,57]
>*  Enter size in K words for the system image [D R:48.-124. D:48.]: <CR>
>PIP [1,57]RSX11M.SYS/NV/CO/BL:498.=[1,57]RSX11M.TSK
>* Do you wish to edit [1,57]SYSVMR.CMD? [Y/N]: <CR>
```

[STEP 7]
usual answer is "NO "or <CR>. only answer "YES" if you have to change partition sizes, install additional tasks, etc.

```
;>
>; VMR is now being performed.
>;
>VMR @[1,57]SYSVMR.CMD
VMR -- INSTALLED TASKS MAY NO LONGER FIT IN PARTITION
```

normal warning - disregard at this time.

```
SET /TOP=DRVPAR:-*
>;
>; Don't forget to create an account file with SACNT.
>;
>TIM
11:12:21 09-JUN-80
>;
>;
>BOO RSX11M
```

at this point, the new executive is booted automatically and waits for a response from you.

```
RSX11M V3.2 BL26
```

```
>TIM 11:14 09-JUN-80 <CR>
```

[STEP 8] set the correct time and date

```
>SAV /MB <CR>
```

this command will save and boot the new system image.

```
  RSX-11M V3.2 BL26   640K   MAPPED
```

ensure that memory size is correct.

```
>RED DB:=SY:
>RED DB:=LB:
>MOU DB:DLDBL26
>@DB:[1,2]STARTUP
>* Please enter time and date (DD-MMM-YY HH:MM) [S]: <CR>
```

if you have set the correct time and date in step 8, it is not necessary to do so again.

```
>TIM
11:14:19 09-JUN-80
```

```
 SET /SYSUIC=[1,57]
>INS $CDA
>INS $DIGMAC /PAR=GEN
>INS $DIGTKB /PAR=GEN
>INS $FLX
>PIP SY:/FR
```

[STEP 9]

```
DB0: HAS 101793. BLOCKS FREE, 29887. BLOCKS USED OUT OF 131680.
LARGEST CONTIGUOUS SPACE = 74786. BLOCKS
```

use default checkpoint file size, ONLY if the number of contiguous blocks is greater than the default size.

```
>* Do you want the default checkpoint file size [5120]? [Y/N]: <Y> <CR>
> ACS SY:/BLKS=5120.
>RUN ERRLOG
>BRO ALL:RSX11M IS NOW ON THE AIR !!!!!
ERL -- ERROR LOG INITIALIZED
>^Z <EOF>
```

```
>SET /UIC=[2,300] <CR>                                          [STEP 10]

>@LBUETP <CR>                                                   this command will
                                                                start the UETP
                                                                session.
>;
>;      ************************************************
>;      *                                              *
>;      *   RSX-11M V3.2 INSTALLATION VERIFICATION PACKAGE   *
>;      *                                              *
>;      ************************************************
>;
>SET /UIC=[2,300]
>RUN ERRLOG
>;
>* DO YOU WISH TO RUN RMDEMO? [Y/N]: <CR>
>;
>* ENTER VERSION OF UETP TO BE RUN (SAM, SUB, MFG, ENG) [S]: MFG <CR>    always "MFG"
>* ENTER UNIT NUMBER OF TERMINAL [S]: 0 <CR>
>;
>;
>* ENTER INPUT DEVICE (DDNN) OR <cr>  [S]: <CR>                  press <cr> if UETP
                                                                resides on system
                                                                disk, if not, then
                                                                enter device it
                                                                resides on.
>;
>;
>;
>;              **** NOTE ****
>;
>; TEST MEDIA MUST BE LOADED ON ALL TAPE AND DISK DRIVES. USE SCRATCH TAPES
>; AND FILES-11 FORMAT DISKS.
>;
>; ALL MAGTAPES BEING TESTED ARE OVER-WRITTEN. THE DISKS ARE
>; TESTED WITH FILE-STRUCTURED I/O WITH NO NEGATIVE EFFECT ON DATA
>; OR STRUCTURE.
>;
>; BEFORE PERFORMING THE FILE-STRUCTURED I/O TEST, ALL UNMOUNTED
>; DISKS ARE MOUNTED AUTOMATICALLY.
>;
>* DO YOU NEED TO INITIALIZE ANY DISKS? [Y/N]: <CR>              if you forgot to
                                                                "init" any disks,
                                                                type "YES"
```

```
>;
>TIM
11:21:14 09-JUN-80
>;
>;
>; ONE COMPLETE PASS OF THIS UETP WILL TAKE 4 HOURS
>;
>* HOW MANY PASSES DO YOU WISH TO RUN [D R:1.-6. D:1.]: 2 <CR>
>;
>;
>;THE 2 PASS(ES) YOU HAVE SELECTED, WILL TAKE 8 HOURS TO RUN.
>;
>; NEEDED UTILITIES WILL BE INSTALLED NOW.
>; ************************************************************
>INS LB:SCMP
>; ************************************************************
>PIP TAILOR.DAT=DEVM.SAM/AP
>MAC DEFINE=LB:[11,10]DLDMC.MAC/PA:1,SY:[2,300]DEFINE
>TKB DEFINE/PR/CP=DEFINE,LB:[1,57]RSX11M.STB,[1,1]EXELIB/LB
>INS DEFINE/TASK=DEFINE
>PIP *.*/PU
>RUN DEFINE
>;
>;START OF UETP PASS #1
>;
>;
>;
>;       * CPU-BOUND LOAD TEST *
>;
>INS DUMMY/TASK=DUM00/PRI=40.
>INS LOGGER/TASK=LOG00
>INS GTRUN /TASK=GTR00
>RUN DUM00
>;
>; FOR THE NEXT FEW MINUTES A NUMBER.....ETC.   At this point the
    U.E.T.P. will run for the selected amount of time.
    The CPU tests are run first, for 2 HOURS, followed by 2 HOURS of
    IO EXERCISER, and then recreated until the pass count is satisfied.
```

	SIZE	CODE	NUMBER	REV
	A	SP	MA-E1000-0-0	A

```
>REM SIO
>TIM
19:21:25 09-JUN-80

>;
>;      *TEST COMPLETED*
>;
>;
>;END OF UETP PASS #2
>;
>;
>PIP *.DAT;*/DE
>;
>; IF ANY ERRORS HAVE BEEN LOGGED BY ERROR LOGGER, WHEN THE COMMAND FILE
>; EXITS YOU SHOULD PRINT [2,300]ERRLOG.LST AND INVESTIGATE THE ERRORS.
>;
>ERF
ERF -- REQUESTED "ERRLOG" TO STOP LOGGING
>PSE SY:=SY:
ERL -- LOGGING ENDED AFTER 0 ERRORS
>SYE SY:=SY:/-SP
SYE -- 1. PAGES IN REPORT
>;
>RUN ERRLOG
ERL -- ERROR LOG INITIALIZED
>
>;
>;
>;
>; ************************************************************************
>;
>TIM
17:14:53 25-MAR-80
>;
>;       *** END OF RSX-11M   INSTALLATION VERIFICATION ***
>;
>; ************************************************************************
>/
>^Z <EOF>
>
>PIP TI:=[2,300]ERRLOG.LST <CR>
```

[STEP 11]
type this to see any errors that have been logged. further information on the ERROR LOGGER can be found on page 27 of the "DLDSGN USERS GUIDE".

9.0 APPENDIX

9.1 APPENDIX A

CSR and VECTOR addresses supported
by stand-alone DSC

System-Generated CSR and Vector Addresses

DEVICE TYPE	CSR	VECTOR
DB:	176700	254
DK:	177404	220
DL:	174400	160
DM:	177440	210
DP:	176714	300 *
DR:	176700	320 *
MM:	172440	224
MT:	172522	320 *
MS:	172522	224

* Indicates nonstandard vector address

9.2 APPENDIX B

DEVICES SUPPORTED BY "DSC" VARIATIONS

DSCS8	DSCS16
RP04/05/06	RP04/05/06
RK05	RK05
RL01/02	RL01/02
RK06/07	RK06/07
RP02/03	RM02/03
RM02/03	TE16
TE10/16	TS11/TS04
TU45/77	TU45/77


F105D

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION **DATE** 10/30/80

TITLE M.A.S.T. WPS-8/211 PHASE III USER'S GUIDE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	New Release	MA-A0000-ML011			[signature]	6/26/81

ENG	APRD	SIZE	CODE	NUMBER	REV
Dominic Pischetola	Kevin Kelcher	A	SP	MA-F1050-0-0	A

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1.0 SCOPE

This document is an attempt to provide WORD PROCESSING operators and technicians direction in running PHASE III on the WS211 Series systems. It does not try to explain how to run Word Processing Software in any environment other than F.A.& T.

The WPS-8/211 Phase III is a software/hardware system verification test designed to simulate the environment in which Word Processing Systems are used. This WPS-8/211 Phase III Package is written to provide an easy to use, consistent method of exercising WS211 Series Systems.

1.1 HARDWARE REQUIREMENTS

- 32K of memory
- A console terminal (VT100)
- RX02 Dual Floppy Drive

The Optional Hardware supported by this test package is as follows:

- Communication Lines (KL8-A IOT 46,47)

1.2 SOFTWARE REQUIREMENTS

- WPS-8/211 Phase III Test Package
  This Test package can be obtained by contacting the Salem Systems Manufacturing Engineering Group.

2.0 REFERENCE DOCUMENTATION

MP00780	WS211 Field Maintenance Print Set
QF711-HZ	WPS Documentation Kit

3.0 RESPONSIBILITY

The SALEM SYSTEMS MANUFACTURING ENGINEERING GROUP is responsible for maintaining this document.

4.0 SPECIAL INSTRUCTIONS

4.1 This Test Package is designed to exercise the following only:

- RX02 dual floppy drive
- Memory
- KL8-A Communication Lines (KL8-A IOT 46,47)

4.2 If system has an H326 panel, move all switches to the "OFF" position.

4.3 Connect a VT100 to the console terminal port located on the static filter bracket.

4.4 Throughout this document the user responses are underlined. Preceding the underlined response are the words Press or Type. Example: Press -> GOLD MENU (in respone to this example the user must press the GOLD key, located on the top left hand side of the mini-keypad, then the letter M). Example: Type -> E 2 <CR> (in respone to this example the user must type the letter E, space, number 2, carriage return).

5.0 GENERAL OVERVIEW

5.1 WPS-8/211 EXERCISER PROGRAM CONTENTS

The WPS-8/211 Phase III Exerciser Program consists of the following files:

Doc #	Name	
2	ABREV....	File that contains stored text that will be called from an abbreviation code.
3	LIST.....	Used to perform List Processing.
4	SPEC.....	Used as the Selection Specification File during List Processing.
5	FORM.....	Output format of List Processing.
6	UDK1.....	139 block document. Used to exercise the RX floppy drives.
7	COMM TEST.	Document that is sent to the Host Terminal during the communication line test.

The WPS-8/211 Phase III Exerciser Program was designed to minimize operator intervention time. This was done by using the Software's "User Define Keys" (UDK's). The UDK's that are used are numbered from 1 thru 9. The following section includes a summary and a listing of each UDK.

UDK 1 - will initialize the diskette in Drive 1 as a document diskette and create a file named PASS on Drive 1. The PASS file is used to log the software features as they are performed to the hardware. The user will then be asked to type the System's DEC number.

M C RETURN D RETURN RETURN GOLD:M C SPACE P A S S RETURN GOLD:=ST

UDK 2 - will run the complete WPS-8/211 Phase III Test Package without operator intervention. This UDK will perform UDK 3 thru UDK 7 and UDK 9 for the required two (2) passes.

GOLD:3 GOLD:3 GOLD:9

UDK 3 - will perform one pass, instead of the required two(2) passes one would get by pressing UDK 2.

GOLD:4 GOLD:5 GOLD:6 GOLD:7

UDK 4 - will exercise the RX Drive 1. It will perform a GET document of 139 blocks from Drive 0 to Drive 1, it will then find the beginning of the document, then find the end of the document. When it finds the end of the document it will read the document backwards on the screen. Successful completion of this function will be logged into the Pass file.

C SPACE U D K 1 RETURN GOLD:G 0 . U D K 1 RETURN GOLD:T GOLD:B G-BACK GOLD:F D SPACE U D K 1 RETURN Y E S RETURN E SPACE 2 RETURN G-ADV GOLD:=DE GOLD:\ RETURN GOLD:F

UDK 5 - will perform a Diskette Verificiation check on Drive 1. Successful completion of this function will be logged into the Pass file.

M C RETURN V RETURN RETURN RETURN GOLD:M E SPACE 2 RETURN G-ADV GOLD:=DV GOLD:\ RETURN GOLD:F

UDK 6 - will perform a large List Processing function of selecting 49 records. The objective is to exercise memory. Successful completion of this function will be logged into the Pass file.

L P RETURN D RETURN Ø . 3 RETURN Ø . 4 RETURN Ø . 5 RETURN R RETURN G Ø RETURN GOLD:M E SPACE 2 RETURN G-ADV GOLD:=LP GOLD:\ RETURN GOLD:F D SPACE R RETURN YES RETURN

UDK 7 - will copy an index into a file. Successful completion of this function will be logged into the Pass file.

C I RETURN 1 SPACE X RETURN C I RETURN Ø SPACE X RETURN A RETURN E SPACE 2 RETURN G-ADV GOLD:=CI GOLD:\ RETURN GOLD:=EN GOLD:\ GOLD:F D SPACE X RETURN YES RETURN

UDK 8 - see section 5.2.

UDK 9 - if UDK 2 is used, UDK 8 will then log an END OF TEST into the Pass file.

E SPACE 2 RETURN G-ADV GOLD:=FF GOLD:F

5.2 UDK 8 COMMUNICATION TEST

The WPS-8/211 Phase III Communication Line Test was designed to minimize operator intervention time. This was done by using the Software's User Define Keys. This UDK 8 will perform the following functions:

-- Set User terminal in communication mode.

-- Transmit a document called COMM TEST to the Host terminal.

-- User terminal will receive characters from the Host terminal by operator intervention.

C X RETURN RUBWRD H S SPACE D H RETURN Ø . 7 RETURN GOLD:M

6.0 WPS-8/211 OPERATING PROCEDURES

6.1 PREREQUISITES

Before one attempts to run this procedure it is assumed that all diagnostics and DEC-X/8 have been successfully run to completion.

6.2 RUNNING THE WPS-8/211 PHASE III TEST

To begin the WPS-8/211 Phase III Test, the user must first:

6.2.1 Apply power to the equipment in the main cabinet. This is done by depressing the switch at the top of the cabinet marked "1".

6.2.2 Apply power to the console terminal.

6.2.3 Insert the WPS-8/211 Phase III Test Disk in Drive 0.

6.2.4 Depress the "BOOT" switch located at the top of the cabinet. The following message is displayed at the console terminal indicating that the boot floppy has successfully loaded into the system;

```
Digital Equipment Corporation

Version x.x

Make sure your system diskette is in drive 0

And press RETURN
```

6.2.5 Insert a single density scratch diskette in Drive 1.

6.2.6 Press the **RETURN** key on your console keyboard.

6.2.7 At this point the DATE/TIME MENU is displayed at the console terminal. The user must enter a valid date and time followed by a **RETURN.**

6.3 RUNNING WPS-8/211 EXERCISER PROGRAM

6.3.1 Press -> GOLD 1 -- Initialization of RX drive 1 will now take place.

6.3.2 Type -> DEC number of system that is being tested.

6.3.3 Press -> GOLD F

6.3.4 Press -> GOLD 2
this test will now exercise the system for approximately 30 mins. Upon completion the Main Menu will be displayed.

6.3.5 Type -> E 2 <CR>

6.3.6 Press -> PARA -- key until your VT100 sounds a beep. This will enable you to check the pass file to determine if there were any errors. See Appendix A.

6.3.7 Press -> GOLD F -- will file document.

6.4 TESTING COMMUNICATION LINES

6.4.1 Attach a VT100 to P6 (P6 is located on the Communication H326 Panel. This VT100 will be referenced as Host VT100. Set Host VT100 up to 1200 baud by:

a) Press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 Keyboard.

b) Press the number 5 to enter SET-UP B.

c) Press the Transmit (Key 7) and Receive (Key 8) Keys until the display reads 1200. Your Host VT100 should look like this on the screen:

1 0100 2 0101 3 0300 4 0010 T SPEED 1200 R SPEED 1200

d) To exit SET-UP B press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 keyboard.

e) Return to the console terminal and

6.4.2 Type -> SO <CR>

6.4.3 Type -> CL 1 <CR>

6.4.4 Press -> GOLD MENU

6.4.5 Press -> GOLD 8
now looking at the Host VT100 that is connected to P6, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal

6.4.6 Type -> THIS IS A TEST
The above message will then be displayed on the Console Terminal.

6.4.7 Type -> \R -- on the Console Terminal to exit.

6.4.8 Move P6 to P7. Set Host VT100 up to 300 baud, Data Bits = 7, Parity Sense = Even, and Parity = On by:

a) Press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 Keyboard.
b) Press the number 5 to enter SET-UP B.
c) Position the cursor above the feature switch to be changed by using the space bar. Change the feature settings by pressing the 6 key on the keyboard. Each time the key is pressed the feature will change to the opposite state.
d) Press the Transmit (Key 7) and Receive (Key 8) Keys until the display reads 300.

Your Host VT 100 Set-Up B should look like this:

1 0100 2 0101 3 0000 4 1100 T SPEED 300 R SPEED 300

e) To exit SET-UP B press the SET-UP key on your Host VT100.

f) Return to the console terminal and

6.4.9 Type -> SO <CR>

6.4.10 Type -> CL 2 <CR>

6.4.11 Press -> GOLD MENU

6.4.12 Press -> GOLD 8
now looking at the Host VT100 that is connected to P7, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal

6.4.13 Type -> THIS IS A TEST
The above message will then be displayed on the Console Terminal.

6.4.14 Hit -> \R -- on the Console Terminal to exit.

6.4.15 Move P7 to P8. Host VT 100 should still be at 300 baud. Change your Host VT 100 Set-Up B, Word 4, (follow steps a thru f in Section 6.4.8) to the following:

4 0010

6.4.16 Type -> SO <CR>

6.4.17 Type -> CL 3 <CR>

6.4.18 Press -> GOLD MENU

6.4.19 Press -> GOLD 8
now looking at the VT100 that is connected to P8, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal:

6.4.20 Type - > THIS IS A TEST
The above message will then be displayed on your Console Terminal.

6.4.21 Type -> \R -- on your Console Terminal to exit.

7.0 WPS-8/211 RUN SUMMARY

The WPS-8/211 Phase III Test was designed to report to the Pass file the name of the specific function it just completed. If one of the functions did not report to the Pass file, we then have an error.

Check the Run Summary Checklist (Appendix A) to determine if you have an error. If you found an error, perform the specific function separately. This is done by typing the following User Define Keys: GOLD n (n = either 1,4,5,6,7).

Error	Action
INITIALIZATION OF DRIVE 1	Press -> GOLD 1
COPY FROM DRIVE Ø TO DRIVE 1 EDIT HAS BEEN TESTED DELETE HAS BEEN TESTED	Press -> GOLD 4
DISKETTE VERIFICATION	Press -> GOLD 5
LIST PROCESSING	Press -> GOLD 6
CREATE INDEX	Press -> GOLD 7

If error persists advise the Manufacturing Engineering Group for technical assistance.

APPENDIX A

RUN SUMMARY CHECKLIST

In order to determine a successful completion of the Phase III Test, the following page contains an example of a successful run of Phase III testing. Your summary which is located in a file called PASS, must be exactly the same as the example on the next page. If not refer to section 7.0 WPS-8/211 Run Summary.

TITLE MODULAR APPROACH TO SYSTEM TESTS

SALEM SYSTEMS MANUFACTURING WPS-8/211 PHASE III TEST

VERSION 1.0

THIS IS THE START OF TESTING FOR
DEC # (The DEC # you originally typed in)

INITIALIZATION OF DRIVE 1 - PASS
COPY FROM DRIVE 0 TO DRIVE 1 - PASS
EDIT HAS BEEN TESTED - PASS
DELETE HAS BEEN TESTED - PASS (DATE,TIME)

DISKETTE VERIFICATION HAS BEEN TESTED - PASS (DATE,TIME)

LIST PROCESSING HAS BEEN TESTED - PASS (DATE, TIME)

CREATE INDEX TESTED - PASS (DATE, TIME)

---------- P A S S C O M P L E T E D (DATE, TIME)

INITIALIZATION OF DRIVE 1 - PASS
COPY FROM DRIVE 0 TO DRIVE 1 - PASS
EDIT HAS BEEN TEST - PASS
DELETE HAS BEEN TESTED - PASS (DATE,TIME)

DISKETTE VERIFICATION HAS BEEN TESTED - PASS (DATE,TIME)

LIST PROCESSING HAS BEEN TESTED - PASS (DATE, TIME)

CREATE INDEX TESTED - PASS (DATE, TIME)

---------- P A S S C O M P L E T E D (DATE, TIME)
IF SYSTEM HAS TWO (2) COMPLETED PASSES THEN

THIS IS THE END OF THE TEST


0505

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 10/30/80

TITLE M.A.S.T. WPS-8/212 PHASE III USER'S GUIDE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	New Release	MA-A0000-ML011			V Scuola	5/29/81

ENG	APPD	SIZE	CODE	NUMBER	REV
Dominic Pischetola	M. Kelemer	A	SP	MA-F2050-0-0	A

TABLE OF CONTENTS

1.0 SCOPE

This document is an attempt to provide WORD PROCESSING operators and technicians direction in running PHASE III on the WPS212 Series systems. It does not try to explain how to run Word Processing Software in any environment other than F.A.& T.

The WPS-8/212 Phase III is a software/hardware system verification test designed to simulate the environment in which Word Processing Systems are used. This WPS-8/212 Phase III Package is written to provide an easy to use, consistent method of exercising WS212 Series Systems.

1.1 HARDWARE REQUIREMENTS

- 32K of memory
- A console terminal (VT100)
- Two (2) Dual RX02 Floppy Drives

The Optional Hardware supported by this test package is as follows:

- Communication Lines (KL8-A IOT 46,47)
- User Lines (KL8-A 40,41)

1.2 SOFTWARE REQUIREMENTS

- WPS-8/212 Phase III Test Package
  This Test package can be obtained by contacting the Salem Systems Manufacturing Engineering Group.

2.0 REFERENCE DOCUMENTATION

MP00780	WS211 Field Maintenance Print Set
QF711-GZ	WPS Documentation Kit

3.0 RESPONSIBILITY

The SALEM SYSTEMS MANUFACTURING ENGINEERING GROUP is responsible for maintaining this document.

4.0 SPECIAL INSTRUCTIONS

4.1 This Test Package is designed to exercise the following only:

- Two (2) Dual RX FLOPPY DRIVES
- Memory
- KL8-A Communication Lines (IOT 46,47)
- KL8-A User Lines (IOT 40,41)

4.2 If the system has an H326 Panel, move all switches to the "OFF" position.

4.3 Connect a VT100 to the console terminal port located on the static filter bracket.

4.4 Throughout this document the user responses are underlined. Preceding the underlined response are the words Press or Type. Example: Press -> GOLD MENU (in respone to this example the user must press the GOLD key, located on the top left hand side of the mini-keypad, then the letter M).
Example: Type -> E 2 <CR> (in respone to this example the user must type the letter E, space, number 2, carriage return).

5.0 GENERAL OVERVIEW

5.1 WPS-8/212 EXERCISER PROGRAM CONTENTS

The WPS-8/212 Phase III EXERCISER PROGRAM CONSISTS OF THE Following files:

DOC #	NAME	
2	ABBREV....	File that contains stored text that will be called from an abbreviation code.
3	LIST.....	Used to perform List Processing.
4	SPEC.....	Used as the Selection Specification File during List Processing.
5	FORM.....	Output format of List Processing.
6	UDK1.....	120 block document. Used to exercise the RX floppy drives.
7	COMM TEST.	Document that is sent to the Host Terminal during the Communication Line test.
8	MESS1.....	Will display a procedure for initializing diskettes.
9	START.....	File that logs the System DEC number.

The WPS-8/212 Phase III Exerciser Program was designed to minimize operator intervention time. This was done by using the Software's "User Define Keys" (UDK's). The UDK's that are used are numbered from 1 thru 9. The following section includes a summary and a listing of each UDK.

UDK 1 - will edit the start file to delete the previous System's DEC number. The user will then be asked to type the System's DEC number.

E SPACE Ø . 9 RETURN GOLD:, GOLD:. ADVANC DELWRD

UDK 2 - will inform the user to hit GOLD 9 to initialize scratch diskettes.

E SPACE Ø.8 RETURN GOLD:B

UDK 3 - will create a file named PASS on Drive 1. The START file on Drive Ø will be copied into the PASS file on Drive 1 by the GET document command. The PASS file is used to log the software features as they are performed to the hardware.

This UDK will then proceed to exercise RX Drive Ø and 1 by performing a GET document of 12Ø blocks from Drive Ø to Drive 1, it will then find the beginning of the document, then find the end of the document. When it finds the end of the document it will read the document backwards on the screen. Successful completion of this function will be logged into the PASS file.

This UDK will then perform the above exerciser to RX Drive 2 from RX Drive 1, then to RX Drive 3 from RX Drive Ø.

C SPACE P A S S RETURN GOLD:G Ø . 9 RETURN GOLD:F C SPACE F RETURN GOLD:G Ø . 6 RETURN GOLD:T GOLD:B G-BACK GOLD:F E SPACE 2 RETURN G-ADV GOLD:AA GOLD:\ RETURN GOLD:F C SPACE 2 . F RETURN GOLD:G F RETURN GOLD:T GOLD:B G-BACK GOLD:F E SPACE 2 RETURN G-ADV GOLD:BB GOLD:\ RETURN GOLD:F C SPACE 3 . F RETURN GOLD:G Ø . 6 RETURN GOLD:T GOLD:B G-BACK GOLD:F E SPACE 2 RETURN G-ADV GOLD:CC GOLD:\ RETURN GOLD:F GOLD:4

UDK 4 - will perform a diskette verification check on Drive 1. Successful completion of this function will be logged into the PASS file.

M C RETURN V RETURN RETURN RETURN GOLD:M E SPACE 2 RETURN G-ADV GOLD:DV GOLD:\ RETURN GOLD:F GOLD:5

UDK 5 - will perform a large List Processing function of selecting 49 records. A GET Document will copy, FORM from Drive Ø to Drive 2, SPEC from Drive Ø to Drive 3. List Processing will then merge the documents LIST on Drive Ø, FORM on Drive 2, and SPEC on Drive 3 into a document named R on Drive 1. Successful completion of this function will be logged into the Pass file.

C SPACE 3 . S RETURN GOLD:G Ø . 4 RETURN GOLD:F C SPACE 2 . M RETURN GOLD:G Ø . 5 RETURN GOLD:F L P RETURN D RETURN Ø . 3 RETURN 3 . S RETURN 2 . M RETURN R RETURN G O RETURN GOLD:M E SPACE 2 RETURN G-ADV GOLD:LP GOLD:\ RETURN GOLD:F GOLD:6

UDK 6 - will log an END OF TEST into the PASS file.

UDK 7 - reserved for future use.

UDK 8 - see Section 5.2.

UDK 9 - will initialize diskettes as document diskettes. After initialization this UDK will go back to UDK #2.

M C RETURN D RETURN RETURN GOLD:M GOLD:2

5.2 UDK 8 COMMUNICATION TEST

The WPS-8/212 Phase III Communication Line Test was designed to minimize operator intervention time. This was done by using the Software's User Define Keys. This UDK 8 will perform the following functions:

-- Set User terminal in communication mode.

-- Transmit a document called COMM TEST to the Host terminal.

-- User terminal will receive characters from the Host terminal by operator intervention.

C X RETURN RUBWRD [illegible] SPACE D H RETURN Ø . 7 RETURN GOLD:M

6.0 WPS-8/212 OPERATING PROCEDURES

6.1 PREREQUISITES

Before one attempts to run this procedure it is assumed that all diagnostics and DEC X/8 have been successfully run to completion.

6.2 RUNNING THE WPS-8/212 PHASE III TEST

To begin the WPS-8/212 Phase III Test, the user must first:

6.2.1 Apply power to the equipment in the main cabinet. This is done by depressing the switch at the top of the cabinet marked "1".

6.2.2 Apply power to the console terminal.

6.2.3 Insert the WPS-8/212 Phase III Test Disk in Drive 0.

6.2.4 Depress the "BOOT" switch located at the top of the cabinet. The following message is displayed at the console terminal indicating that the boot floppy has successfully loaded into the system;

```
Digital Equipment Corporation

Version x.x

Make sure your system diskette is in drive 0

And press RETURN
```

6.2.5 Press the **RETURN** key on your console keyboard.

6.2.6 At this point the DATE/TIME MENU is displayed at the console terminal. The user must enter a valid date and time followed by a **RETURN.**

6.3 RUNNING WPS-8/?12 EXERCISER PROGRAM

6.3.1 Press -> GOLD 1

6.3.2 Type -> the DEC number of system that is being tested.

6.3.3 Press -> GOLD F

6.3.4 Press -> GOLD 2

6.3.5 ->INSERT A SINGLE DENSITY SCRATCH DISKETTE IN DRIVE 1.

6.3.6 Press -> GOLD F

6.3.7 Press -> GOLD 9

6.3.8 -> REMOVE DISKETTE FROM DRIVE 1 AND INSERT IT IN DRIVE 3.

6.3.9 -> INSERT ANOTHER SINGLE DENSITY SCRATCH DISKETTE IN DRIVE 1.

6.3.10 Press -> GOLD F

6.3.11 Press -> GOLD 9

6.3.12 -> REMOVE DISKETTE FROM DRIVE 1 AND INSERT IT IN DRIVE 2.

6.3.13 -> INSERT ANOTHER SINGLE DENSITY SCRATCH DISKETTE IN DRIVE 1.

6.3.14 Press -> GOLD F

6.3.15 Press -> GOLD 9

6.3.16 Press -> GOLD F

6.3.17 Press -> GOLD 3
this test will now exercise the system for approximately 30 mins. Upon completion the Main Menu will be displayed.

6.3.18 Type -> E 2 <CR>

6.3.19 Press -> PARA -- key until your VT100 sounds a beep. This will enable you to check the pass file to determine if there were any errors. See Appendix A.

6.3.20 Type -> GOLD F -- will file document.

6.4 TESTING COMMUNICATION LINES

6.4.1 Attach a VT100 to P6 (P6 is located on the communication H326 panel). This VT100 will be referenced as Host VT100. Set Host VT100 up to 1200 baud by:

a) Press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 Keyboard.

b) Press the number 5 to enter SET-UP B.

c) Press the Transmit (Key 7) and Receive (Key 8) Keys until the display reads 1200. Your Host VT100 should look like this on the screen:

1 0100 2 0101 3 0000 4 0010 T SPEED 1200 R SPEED 1200

d) To exit SET-UP B press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 keyboard.

e) Return to the console terminal and

6.4.2 Type -> SO <CR>

6.4.3 Type -> CL 1 <CR>

6.4.4 Press -> GOLD MENU

6.4.5 Press -> GOLD 8
now looking at the Host VT100 that is connected to P6, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal

6.4.6 Type -> THIS IS A TEST
The above message will then be displayed on the Console Terminal.

6.4.7 Type -> \R -- on the Console Terminal to exit.

6.4.8 Move P6 to P7. Set Host VT100 up to 300 baud, Data Bits = 7, Parity Sense = Even, and Parity = On by:

a) Press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 Keyboard.
b) Press the number 5 to enter SET-UP B.
c) Position the cursor above the feature switch to be changed by using the space bar. Change the feature settings by pressing the ó key on the keyboard. Each time the key is pressed the feature will change to the opposite state.
d) Press the Transmit (Key 7) and Receive (Key 8) Keys until the display reads 300.

Your Host VT 100 Set-Up B should look like this:

1 0100 2 0101 3 0000 4 1100 T SPEED 300 R SPEED 300

e) To exit SET-UP B press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 keyboard.

f) Return to the console terminal and

6.4.9 Type -> SO <CR>

6.4.10 Type -> CL 2 <CR>

6.4.11 Press -> GOLD MENU

6.4.12 Press -> GOLD 8
now looking at the Host VT100 that is connected to P7, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal

6.4.13 Type -> THIS IS A TEST
The above message will then be displayed on the Console Terminal.

6.4.14 Type -> \R -- on the Console Terminal to exit.

6.4.15 Move P7 to P8. Host VT100 should still be at 300 baud. Change your Host VT 100 Set-Up B, Word 4,(follow steps a thru f in Section 6.4.8) to the following:

4 0010

6.4.16 Type -> SO <CR>

6.4.17 Type -> CL 3 <CR>

6.4.18 Press -> GOLD MENU

6.4.19 Press -> GOLD 8
now looking at the VT100 that is connected to P8, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal:

6.4.20 Type -> THIS IS A TEST
The above message will then be displayed on your Console Terminal.

6.4.21 Type -> \R -- on your User Terminal to exit.

7.0 TESTING USER LINES

7.1 If your system has a KL8-A at IOT 40,41 or IOT 46,47 connect a VT100 to P5 (L0) on the H326 Panel. This VT100 is hereafter know as VT100 #2.

NOTE: If your system is configured for two (2) KL8-A's and two (2) H326 Distribution Panels -- IOT 40,41 and IOT 46,47, the KL8-A at IOT 40,41 is inoperative. In this situation, IOT 46,47 H326 Panel P5 (L0) is reserved for VT100 #2, and P6 - P8 are reserved for communications. In order to test out P5 (L0) your VT100 #2 must be set up for 9600 baud.

7.2 Remove scratch diskette from Drive 2.

7.3 Insert another WPS-8/212 PHASE III Test Disk in Drive 2.

7.4 Depress the "BOOT" switch located at the top of the cabinet. The following message should now appear on your VT100 #2:

```
Digital Equipment Corporation

Version x.x

Make sure your system diskette is in drive 2

And press RETURN
```

7.5 Press -> <CR> -- on VT100 #2

7.6 At this point the DATE/TIME MENU is displayed on the VT100 #2 terminal. The user must enter a valid date and time followed by a **RETURN.**

7.7 The MAIN MENU should now be displayed on the VT100 #2 terminal. Visually check that the date and time you typed into the DATE/TIME MENU now appears in the upper right-hand corner.

7.8 Type -> F <CR> - to log off system.

NOTE: If you have another KL8-A at IOT 40,41 power down system, unseat KL8-A IOT 46,47, plug VT100 #2 into P5 (L0) of the distribution panel (IOT 40,41). Power up system and follow the steps 7.4 though 7.8. After successful completion reseat KL8-A IOT 46,47.

8.0 WPS-8/212 RUN SUMMARY

The WPS-8/212 Phase III Test was designed to report to the Pass file the name of the specific function it just completed. If one of the functions did not report to the Pass file, we then have an error.

Check the Run Summary Checklist (Appendix A) to determine if you have an error. If you found an error, perform the specific function separately. This is done by typing the following User Define Keys: GOLD n (n = either 3,4,5).

Error	Action
COPY FROM DRIVE 0 TO DRIVE 1 COPY FROM DRIVE 1 TO DRIVE 2 COPY FROM DRIVE 0 TO DRIVE 3	Hit>GOLD 3
DISKETTE VERIFICATION	Hit>GOLD 4
LIST PROCESSING	Hit>GOLD 5

If error persists advise the Manufacturing Engineering Group for technical assistance.

APPENDIX A

RUN SUMMARY CHECKLIST

In order to determine a successful completion of the Phase III Test, the following page contains an example of a successful run of Phase III testing. Your summary which is located in a file called PASS, must be exactly the same as the example on the next page. If not refer to section 8.0 WPS-8/212 Run Summary.

SALEM SYSTEMS MANUFACTURING WPS-8/212 PHASE III TEST

VERSION 1.0

THIS IS THE START OF TESTING FOR
DEC # (The DEC # you originally typed in)

COPY FROM DRIVE 0 TO DRIVE 1 - PASS (DATE,TIME)

COPY FROM DRIVE 1 TO DRIVE 2 - PASS (DATE,TIME)

COPY FROM DRIVE 0 TO DRIVE 3 - PASS (DATE,TIME)

DRIVE 1 DISKETTE VERIFICATION - PASS (DATE,TIME)

LIST PROCESSING HAS BEEN TESTED - PASS (DATE,TIME)

---------- P A S S C O M P L E T E D (DATE, TIME)

THIS IS THE END OF THE TEST


V2100

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION	M.A.S.T.	DATE
TITLE	MODULAR APPROACH TO SYSTEMS TEST	

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A						
B	VAX 11780 CPU Procedure Update and rewrite	MLO13	Al Gauthier	3/14/81		

Al Gauthier

ENG	APPD	SIZE	CODE	NUMBER	REV
Al Gauthier	Bob Beck	A	SP	MAV2100-0-0	B

VAX 11780 CPU

1.0 INTRODUCTION

The VAX 11/780 CPU is a high-speed, microprogrammed 32-bit hexadecimal computer. The 11/780 executes VAX-11 variable length instructions in native mode, and non-privileged PDP-11 instructions in compatibility mode. The processor can directly address 4 gigabytes of virtual address space, and provides a complete and powerful instruction set that includes integral decimal, character string, and floating point instructions. The 11/780 CPU includes an 8KB memory cache, integral memory management, translation buffer, 8B instruction buffer, 16 general registers, 32 interrupt priority levels, and an intelligent console. (LSI-11)

2.0 REFERENCE DOCUMENTATION

2.1 Manuals

2.1.1	Micro Computer Handbook	EB-07948
2.1.2	PDP-11/03 Users Manual	EK-LSI11-TM
2.1.3	RXV11 Users Manual	EK-RXV11-OP
2.1.4	Floppy Disk System Maint. Man.	EK-RX01-MM
2.1.5	RX01 Floppy IPB	EK-RX01-IP
2.1.6	PDP 11/03 System Manual	EK-11V03-TM
2.1.7	CPU Processor Manual	EK-KA780-TD
2.1.8	TB/CACHE/SBI Control Manual	EK-MM780-TD
2.1.9	Console Manual	EK-KC780-TD
2.1.10	Power System Overview	EK-PS780-TD
2.1.11	Diagnostic System Manual	EK-DS780-TD
2.1.12	Hardware Users Guide	EK-UG780-UG
2.1.13	System Maint. Guide	EK-11780-PG

2.2 Reference Listings

2.2.1	Wirelist & Pin Sort	7013628-0-0
2.2.2	Micro Code Listing (Fiche)	EP-VAX-PCS
2.2.3	WCS Code Listing (Fiche)	EP-VAX-WCS
2.2.4	LSI-11 Programming Ref. Card	EJ-S2000
2.2.5	VAX Instruction Card	EJ-S2000
2.2.6	VAX 11780 Architecture Hndbk	EB-07466
2.2.7	VAX 11 Software Handbook	EB-08126

2.3 Maintenance Print Sets

2.3.1	KA780 Maint. Print Set	MP00496
2.3.2	MS780 Maint. Print Set	MP00498
2.3.3	DW780 Maint. Print Set (OPT)	MP00497
2.3.4	RH780 Maint. Print Set (OPT)	MP00499
2.3.5	FP780 Maint. Print Set (OPT)	MP00565

3.0 REQUIRED TEST EQUIPMENT

3.1 Diagnostic Diskettes

3.1.1	RX1 Floppy Diskette	AS-E633?-YE
3.1.2	RX2 Floppy Diskette	AS-E158?-DE
3.1.3	RX3 Floppy Diskette	AS-E159?-DE
3.1.4	RX7 Floppy Diskette	AS-E160?-YE
3.1.5	RX8 Floppy Diskette	AS-E161?-YE
3.1.6	RX25 Floppy Diskette	AS-F748?-YE

3.2 W9025 extender board

3.2 Assorted chip clips

3.3 Oscilloscope Tektronix 465 or equivalent

3.4 Voltmeter Tektronix DM44 or equivalent

3.5 Console Terminal

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 LEVEL 4 -The following Diagnostics do not require Diagnostic Supervisor.

ESKAH ---Microdiagnostic Test #1
ESKAJ ---Microdiagnostic Test #2

4.2 EVKAA ---This Diagnostic needs to be run only if operator experiences trouble with Diagnostic Supervisor.

4.3 LEVEL 3 -These Diagnostics run standalone under Diagnostic Supervisor.

EVKAB ---Basic Instruction Exerciser
EVKAC ---Floating Point Inst. Exerciser. Run this test whether Floating Point is installed or not
EVKAD ---Compatability Mode Instruction
EVKAE ---Privileged Architecture

4.4 LEVEL 2 -These Diagnostics run standalone under Diagnostic Supervisor or with Diagnostic Supervisor running under VMS.

4.5 LEVEL 1 -VMS must be running for these Diagnostics.

5.0 SPECIAL INSTRUCTIONS

5.1 CAUTION: No metallic jewelry should be worn while servicing this equipment, due to the high current capabilities of the power supplies.

5.2 Jumper conversion used is:

I = Jumper IN, O = Jumper Out, X = Unimportant

Jumper configurations are explicit or standard configuration is shown by an arow (------->).

5.3 To run floppy ZZ-ESZAC-X.X without the SBI connected to the CPU, jumper the following: (KA780 Backplane)

FROM	TO
E01F1	J5-T
E01F2	J5-J
E01H2	J5-R
E01J1	J5-Z
E01J2	J5-X
E01K2	J5-BB

5.4 In section 8.0, the user's response is underlined.

6.0 INSTALLATION AND TEST SET-UP INSTRUCTION

6.1 KC780 (11/03 Subsystem)

Module Utilization

M7264 KD11-F	
M7940 DLV-11	M7946 RXV-11
M7944 MSV-11B	M9400-YE
SPARE	SPARE

(Front View-Module Handle Side)

6.2 Jumper Configuration KD11-F (M7264) Refer to Figure 1

JUMPER	IN/OUT	RESULT
W1	O	Resident memory at bank 0
W2	I	Resident memory at bank 0
W3	O	LTC Interrupt enabled
W4	O	Memory Refresh enabled
W5	O	Power up at 173000
W6	I	Power up at 173000
W7	*	Preconfigured
W8	*	Preconfigured
W9	O	Disables resident memory
W10	O	BRPLYL
W11	I	Enables on board memory select

6.3 M9400-YE Cable Connection. Refer to Figure 2 Cables are BC05L-10

From M9400-YE	To Backpanel
(Stripe Left, Smooth side UP)	(Stripe Down, Ribbed side to backpanel)
J1	J8
J2	J7

6.4 Configuration of RXV-11 (M7946). Refer to Figure 3 Address Jumpers are set to: 177170-177172

ADDRESS	JUMPER	IN/OUT
A12	W17	O
A11	W16	O
A10	W15	O
A9	W14	O
A8	W13	I
A7	W12	I
A6	W11	O
A5	W10	O
A4	W9	O
A3	W8	O
A2	W7	I

Vector Jumpers are set: 264

VECTOR	JUMPER	IN/OUT
V7	W6	O
V6	W5	I
V5	W4	O
V4	W3	O
V3	W2	I
V2	W1	O

6.5 Configuration of DLV11 (M7940). Refer to Figure 4.

JUMPER	IN/OUT	RESULT
NP	O	No Parity
2SB	I	1 Stop Bit
NB2	O	8 Data Bits
NB1	O	8 Data Bits
PEV	X	Unimportant whether parity odd/even
FEH	O	No halt on framming error
EIA	O	EIA operation
FR3	O	Selects 300 Baud
FR2	O	Selects 300 Baud
FR1	I	Selects 300 Baud
FRØ	O	Selects 300 Baud
CL4-CLO	I	20MA Active Xmit and Receive

NOTE: When using an LA12Ø the Baud is set for 12ØØ. Refer to table below.

JUMPER	IN/OUT
EIA	I
FR2	I
FR1	O

6.5.1 Vector Jumpers set to 6Ø-64

Vector	In/Out
V7	I
V6	I
V5	O
V4	O
V3	I

6.5.2 Address Jumpers set to 177560-177566

Address	In/Out
A12	O
A11	O
A1Ø	O
A9	O
A8	O
A7	I
A6	O
A5	O
A4	O
A3	I

6.6 Configuration of MSV-11B (M7944). Refer to Figure 5

JUMPER	IN/OUT	RESULT
W1	I	Memory Bank select
W2	I	" " "
W3	O	" " "
W4	O	Enables BRPLY during refresh

6.7 KA780 Module Utilization Chart. Refer to Figure 6

6.8 Control Store Jumpers

6.8.1 PCS, M8234 - Backplane Slot 22 Bank Address, Select. For location and pinning of J12 refer to Figures 7 and 8, and to table below.

Bank Adds.	J12-L	J	F	D	B
8-4K	I	O	O	O	O
	J5	J4	J3	J2	J1

NOTE: J1-5 for cross ref. to module schematic only.

6.8.2 Update System I.D. Register to proper Rev level by installing/removing Jumpers on J12 & J13. Refer to Figure 8.

6.8.3 Optional WCS (M8233) or PCS (M8234). Slot 18 Bank Address Select. For location and pinning of J11, refer to Figures 7, 8 and table below.

NOTE: W23 and W24 needs to be installed in the M8232 Module for optional WCS/PCS.

Refer to Figure 9.

Bank Adds.	J11-FF Board J5 CV2	DD J4 CM1	BB J3 CL2	Z J2 CL1	X J1 CB1
1K	I	I	I	I	O
2K	I	I	I	O	I
3K	I	I	O	I	I
4K	I	O	I	I	I
5K	O	I	I	I	O
6K	O	I	I	O	I
7K	O	I	O	I	I
8K	O	O	I	I	I
	J5	J4	J3	J2	J1

NOTE: J1-5 for cross ref. to module schematic only.

6.8.4 Console Signals at 11/780 CPU backplane.

SIGNAL	J9 PIN	BACKPL
SCPA Boot SW H	B	A29A1
SCPA AUTO Restart H	D	A29B2
SCPA LOCK H	F	A29F1
SCPA REMOTE H	E	A29K1
CIBN Run H	K	A29D1
CIBN ATTN H	L	A29E1

6.9 TR Arbitration Level Selection. For locating and pinning of J10, refer to table below as well as Figures 7 and 8.

J10 -- J F D B	Backplane Wire F02M2 to ----	BUS TR Level
I I I I	----------	16
I I I O	F02U2	15
I I O I	F02U1	14
I I O O	F02T2	13
I O I I	F02S2	12
I O I O	F02P2	11
I O O I	F02P1	10
I O O O	F02N1	09
O I I I	F02M1	08
O I I O	F02J2	07
O I O I	F02J1	06
O I O O	F02H2	05
O O I I	F02F2	04
O O I O	F02E1	03
O O I O	F02D1	02
O O O O	F02C1	01

6.10 Perform visual inspection for obvious discrepancies, damage, or potential power problems.

6.11 Check to see that modules are in the proper slots. Refer to Figure 6.

6.12 Diskette Load

6.12.1 Release drive lock and swing out floppy drive assembly.

6.12.2 Insert diskette RX1 Floppy, (AS-E633?-YE) into RX01 drive assembly.

6.12.3 Close diskette slot cover.

6.13 Power on/Bootstrap

6.13.1 With Main Breaker OFF, plug power cord into proper power outlet.

6.13.2 Turn 869 Power Controller Function Switch to REMOTE position.

6.13.3. With the H7111 Time Of Day Power Supply, LSI-11 DC, and all H7100 CKT Breakers OFF, apply power to 869 Power Controller.

6.13.4 Middle blower should be ON, with air exiting from center exhaust.

6.13.5 Turn on H7111 Time Of Day Power Supply. Power ON indicator should light.

6.13.6 Power On System by Key Switch, and verify operation and air flow direction of the other two blowers.

6.13.7 Power on LSI-11, by placing DC ON/OFF Switch to ON. DC and LED should light. Place HALT/ENABLE Switch to ENABLE.

NOTE: If DC on LED is not lit, check power switch on rear of LSI-11 for on position.

6.13.8 Set CPU Control Panel AUTO/RESTART Switch to OFF.

6.13.9 Turn on H7100 CKT Breakers one at a time observing Power Indicator LED's. Should get green power normal indicators.

6.13.10 With Key in LOCAL position, Console program will boot.

6.13.11 Console Terminal will output message. CPU should now be ready to run diagnostics. Message is shown at 8.1.1 of this procedure.

7.0 POWER CHECK

7.1 Check D.C. voltages, observing safety rules, as follows

CAUTION: Remove rings and watches which could short across voltage points, resulting in severe burns.

VOLTAGE/SIGNAL	PIN	FROM-------TO
+5A (PS#1)	C24A2	4.9V ----- 5.2V
+5B (PS#2)	C01A2	4.9V ----- 5.2V
+5C (PS#3)	C04A2	4.9V ----- 5.2V
+5 T.O.D. CLK	J20-1	4.75V ---- 5.25V
-5 (PS#2)	J18-1 J18-2	-5.0V ----- 5.3V
-10 VOLT	J14-1	-8.0 ----- -11.0V
A	J14-2	-8.0 ----- -11.0V
C	J15-1	-8.0 ----- -11.0V
D	J15-2	-8.0 ----- -11.0V
C	J16-1	-8.0 ----- -11.0V
L	J16-2	-8.0 ----- -11.0V
O	J17-1	-8.0 ----- -11.0V
W	J17-2	-8.0 ----- -11.0V

NOTE: H7100 POWER Supplies are not adjustable and must be repaired or replaced if out of spec.

7.2 If there are no problems, CPU should boot. M8235 will display a UPC of FF. If a UBA is present, the M8271 will display an MPC of 3.

8.0 DIAGNOSTIC TEST PROCEDURE

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimun test criteria, e.g.: pass counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the CHECKLIST.

8.1 Console terminal will display the following message upon completion of boot.

8.1.1
```
CPU HALTED,SCMM CLEAR,STEP=NONE,
CLOCK=NORM,
RAD=HEX,ADD=PHYS,DAT=LONG,FILL=00,
REL=000000
INIT SEQ DONE
HALTED AT 00000000

RELOADING WCS)
LOAD DONE, 00003200 BYTES LOADED
VER: PCS=01  WCS=0D-12 FPLA=0D CON=V05-01-L

>>>
```

8.1.2 Remove RX1 Diskette in drive, and insert RX2 Diskette.

```
T<CR>

ZZ-ESKAB V12.0
01,02,03,04
NO. OF WCS MODULES = 0001
05,06,07,08,09,0A,0B<0C<0D<0E>0F<10,11,12,
13,1
,15,16,17,18,19,1A,1B,1C,1D,1E,1F,20,
SYS ID REG= 01200996
21,22,23,24,25,26,27,28,29,2A,2B,2C,2D,2E,
2F,
3,31,32,33,34,35,36,37,38,39,3A,3B,3C,3D,
END PASS 0001

MOUNT FLOPPY ZZ-ESSZAD & TYPE "DI"

MIC>
```

8.1.3 Remove RX2 Diskette in drive, and insert RX3 Diskette.

DI <CR>

```
3E,
CPU TR= 00000010
MS780 16K CHIP AT TR 01
MAX ADR+1= 00100000
DW780 AT TR 03
RH780 AT TR 08
RH780 AT TR 09
3F,40,41,42,43,44,45,46,47,48,49,4A,4B,4C,
4D,4E
MS780 16K CHIP AT TR 01
 ARRAY #: 00000000
 # SINGLE BIT ERRORS:                    00000000
 ARRAY #: 00000001
 # SINGLE BIT ERRORS:                    00000000
 ARRAY #: 00000002
 # SINGLE BIT ERRORS:                    00000000
 ARRAY #: 00000003
 # SINGLE BIT ERRORS:                    00000000
4F,
MS780 16K CHIP AT TR 01
  M8213 ROMS OK
50,51,52
MP FPA

END PASS 0001

    CPU HALTED,SOMM CLEAR,STEP=NONE,CLOCK=
    NORM
    RAD=HEX,ADD=PHYS,DAT=LONG,FILL=00,
    REL=00000000
    INIT SEQ DONE
    HALTED AT 00000000

    (RELOADING WCS)
    LOAD DONE, 00003200 BYTES LOADED
    VER: PCS=01 WCS=0D-12 FPLA=0D
    CON=V05-01-L


    >>>
```

8.1.4 Remove RX3 Diskette and mount VAX Instruction Diagnostic #1 RX8.

```
                BOOT<CR>

                        CPU HALTED
                        INIT SEQ DONE
                        LOAD DONE, 000142# BYTES LOADED
DIAGNOSTIC SUPERVISOR, ZZ-ESSAA-6.1-370
7-AUG-1980 04:57:54

DS> ATT KA780 SBI KA0 NO NO 0 0 <CR>
DS> SEL KA# <CR>
DS> SET HA <CR>
DS> RUN EVAKB <CR>

..    PROGRAM:    VAX    Basic    Instructions
Exerciser,ZZ-EVKAB,  REV  2.2,  10 TESTS,  AT
05:03:52.76.  TESTING: KA#
.. END OF RUN. # ERRORS DETECTED. PASS
COUNT:1
TIME: 5-AUG-1980  11:52:41.98

DS>
```

8.1.5 Remove RX8 Diskette and mount VAX INST. DIAG. Diskette #2, RX25.

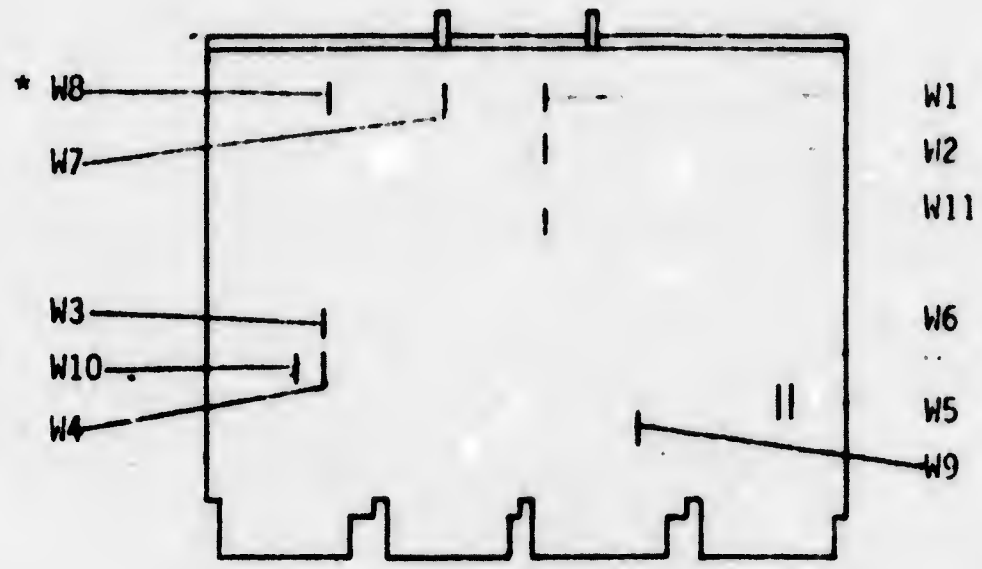
```
        RUN EVKAC <CR>

..PROGRAM: VAX Floating Point Instruction
Exerciser,  ZZ-EVKAC,  REV  2.#,  3 TESTS,  AT
05:06:34.89

TESTING:  _KA#

..  END OF RUN. # ERRORS DETECTED. PASS COUNT:
1. TIME: 7-AUG-1980 05:08:55.78.
DS> RUN EVKAD <CR>

..PROGRAM: VAX Compatibility Mode Instructions
Exerciser, EVKAD, REV 1.2 4 TESTS, AT TESTING:
-KA#

..END OF RUN. # ERRORS DETECTED. PASS  COUNT:1
TIME: 1-JAN-1980 01:43:55.53.
```

```
DS> RUN EVKAE <CR>
..PROGRAM:   VAX   Privileged   Architecture
Exerciser, EVKAE, REV 1.2, 9 TESTS, AT TESTING:
_KA8
..END OF RUN. 0 ERRORS DETECTED. PASS COUNT: 1.
TIME: 5-AUG-1988 11:34:56.48

DS>
```

8.1.6 Remove RX25 Diskette from the drive and mount VAX CHANNEL DIAG. RX7.

```
        ATT DW788 SBI DW8 3 4  <CR>
DS> SEL DW8 <CR>
DS> RUN ESCBA <CR>
..PROGRAM: ZZ - ESCBA - 7.1 DW788 REPAIR
DIAGNOSTIC, REV 7.1, 54 TESTS, AT   11:38:11.71

TESTING: _DW8

UBA UNIT UNDER TEST IS _DW8

..END OF RUN. 0 ERRORS DETECTED. PASS COUNT: 1.
TIME: 5 AUG-1988 11:39:14.58

DS> ATT RH788 SBI RH0 8 5 <CR>
DS> ATT RH788 SBI RH1 9 5 <CR>
DS> SEL RH0 <CR>
DS> SEL RH1 <CR>
DS> RUN ESCAA <CR>

..PROGRAM:  ESCAA-REV,6.2  RH788  DIAGNOSTIC,REV
6.2, 28 TESTS, AT 11:48:37.22.
TESTING: _RH8 _RH1

RH8 BASE ADDRESS IS: 20010888
DRIVE [0] RESPONDED
*******NO MBE PRESENT ON MASSBUS*******
RH1 BASE ADDRESS IS: 20012888
DRIVE [1] RESPONDED
..  END OF RUN. 0 ERRORS DETECTED. PASS COUNT:
1. TIME: 5-AUG-1988 11:42:02.54

DS>
```

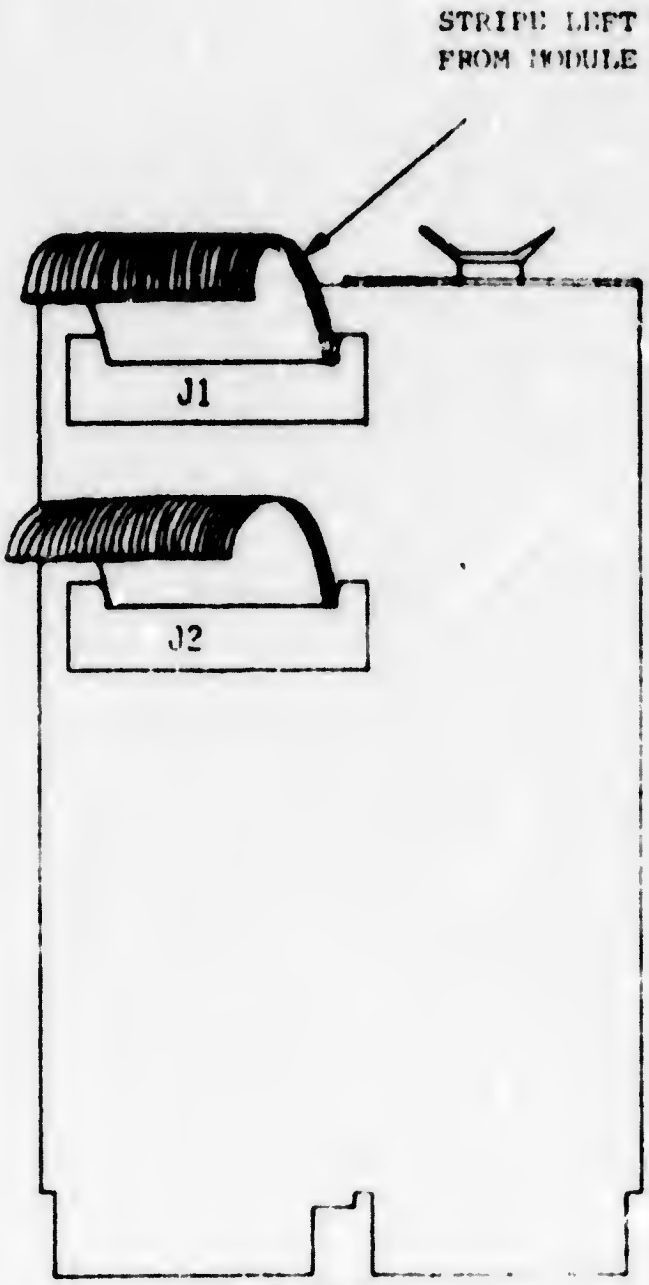
[END OF TEST]



M7264

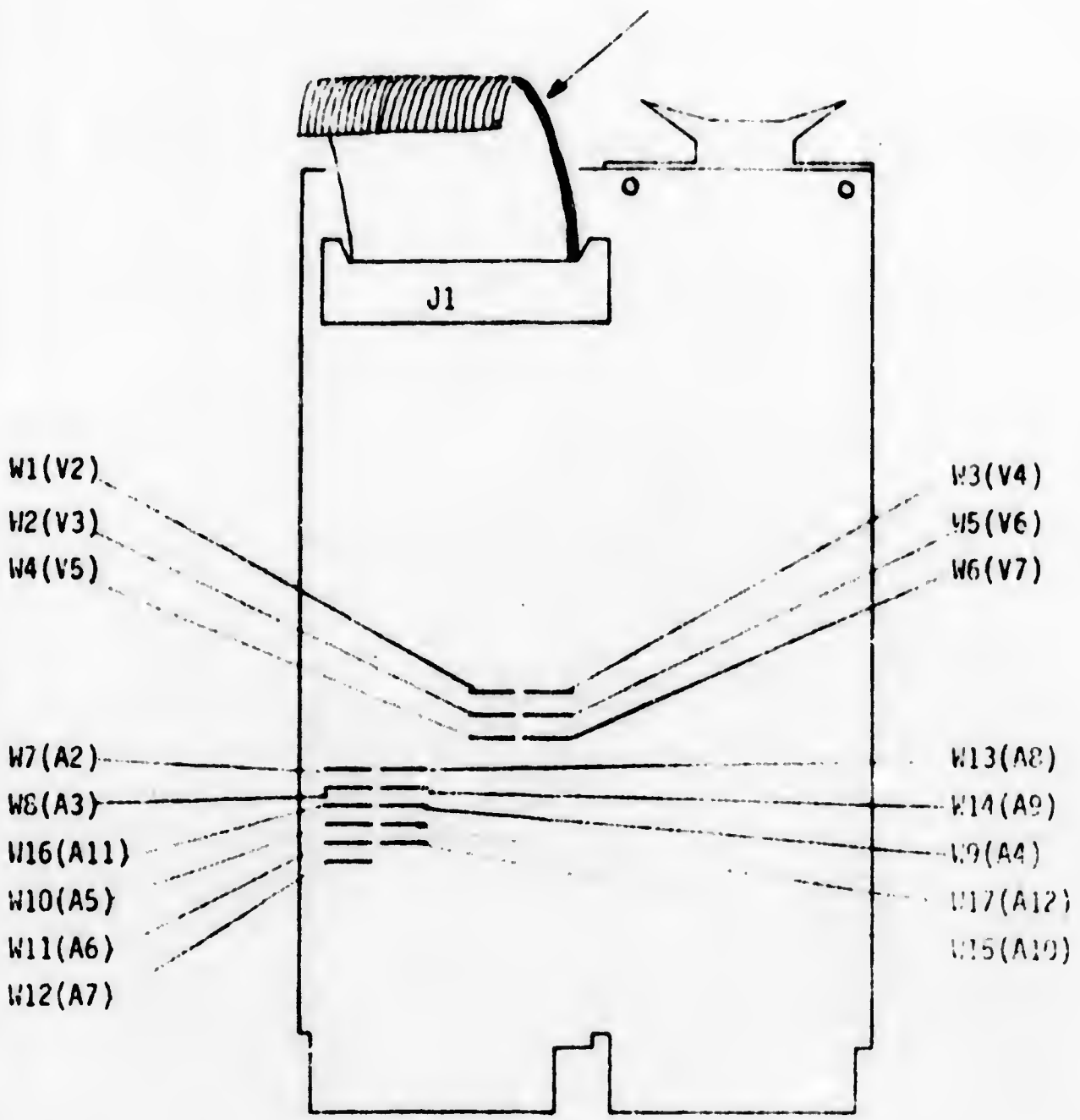
FIGURE 1

*PRECONFIGURED
DO NOT CHANGE (W7 & W8)



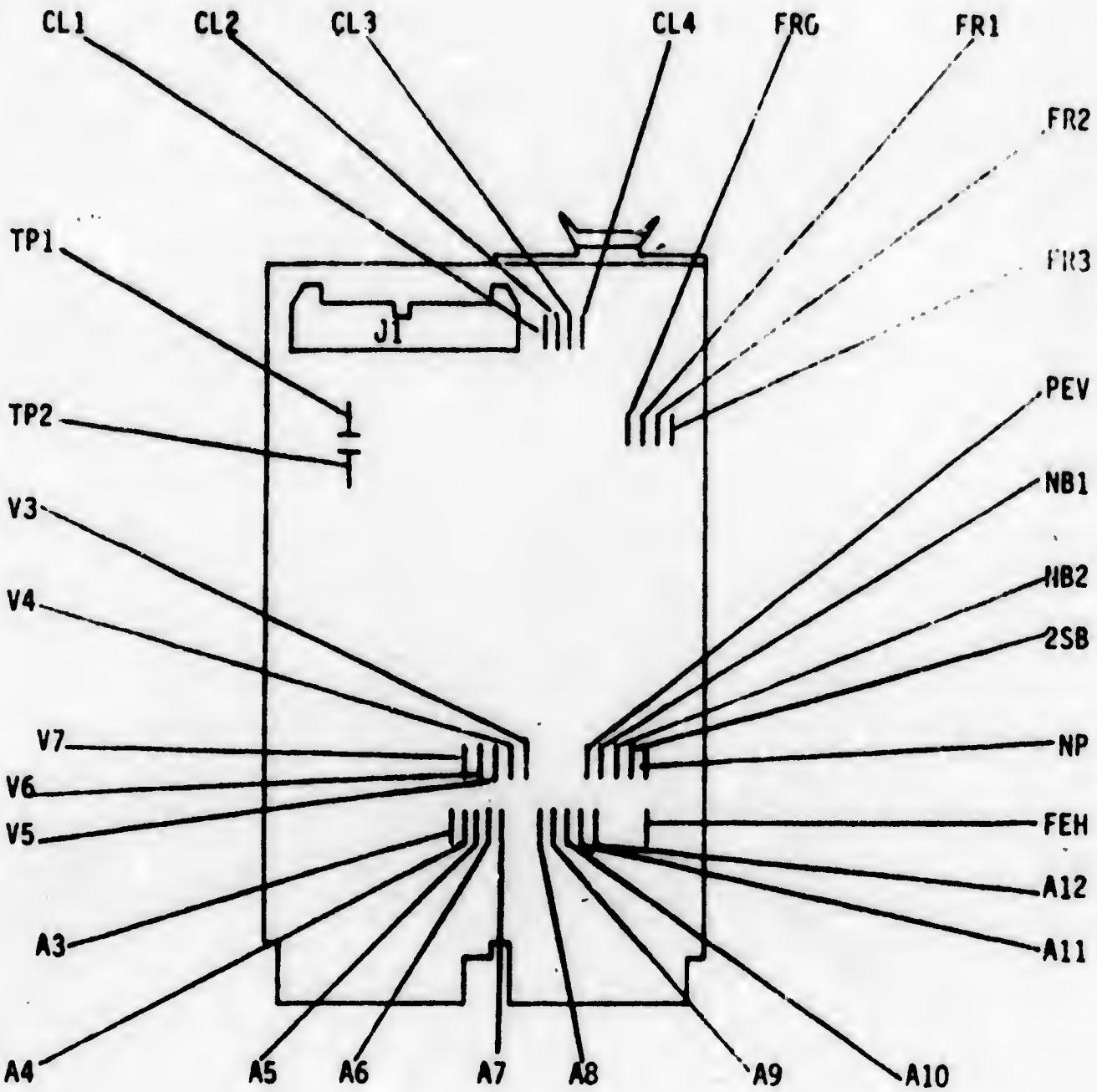
119400-YE

FIGURE 2



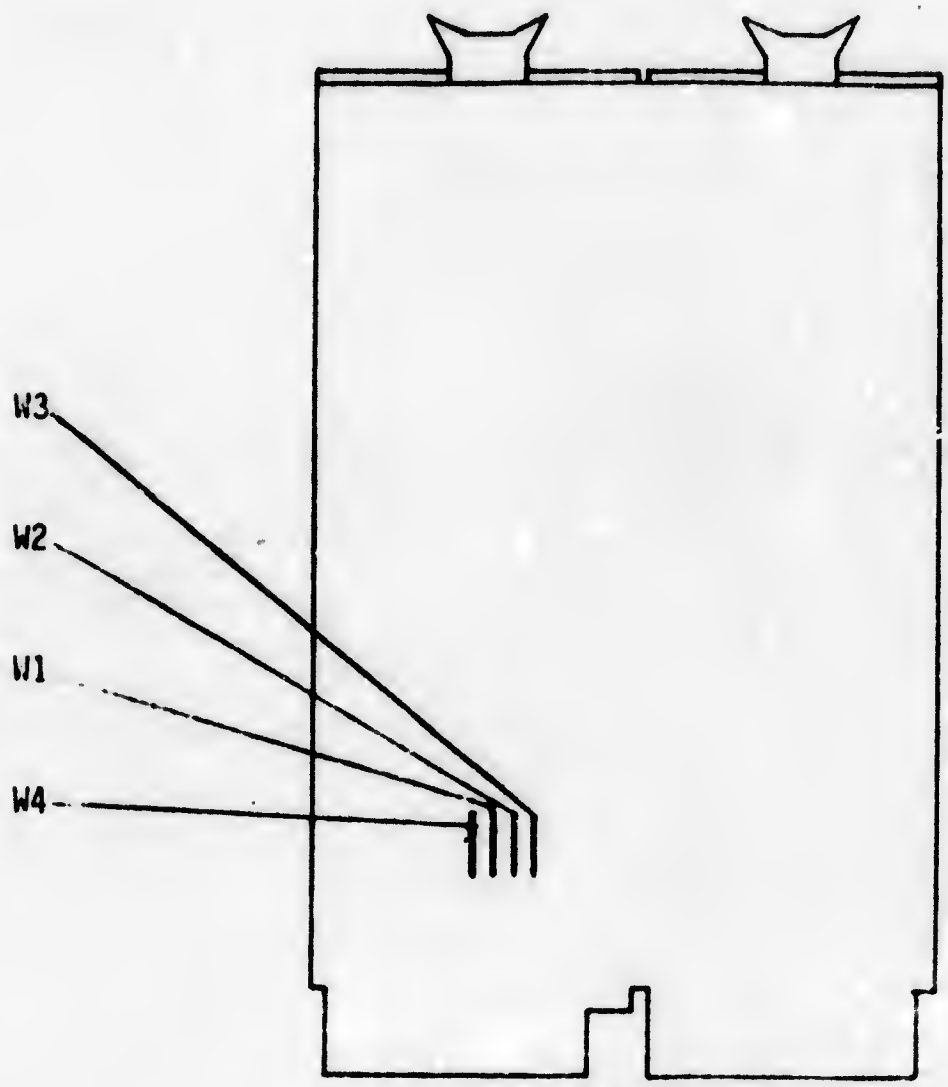
M7946

FIGURE 3



M7940

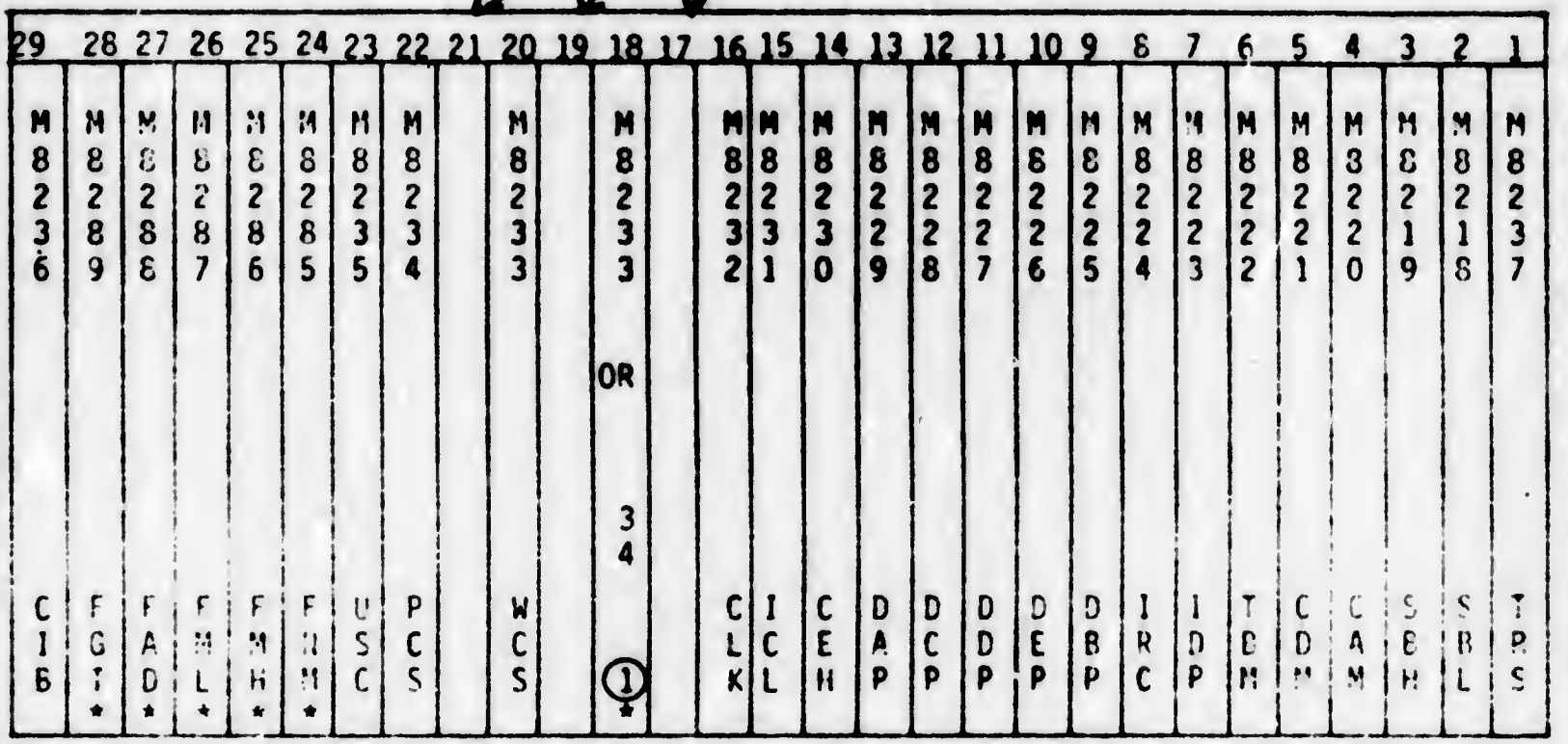
FIGURE 4



M7944

FIGURE 5

SLOTS DO NOT CONTAIN MODULE MOUNTING BLOCKS.



* OPTION OF BLANK MODULES (7014103)
(1) PCS or WCS

VIEW FROM MODULE SIDE

FIGURE 6

PINNING USED ON J10, J11, and J12.

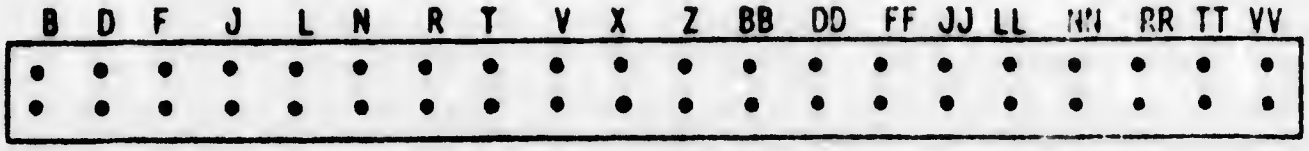


FIGURE 7

TR Select Pin

K780 Backpanel view

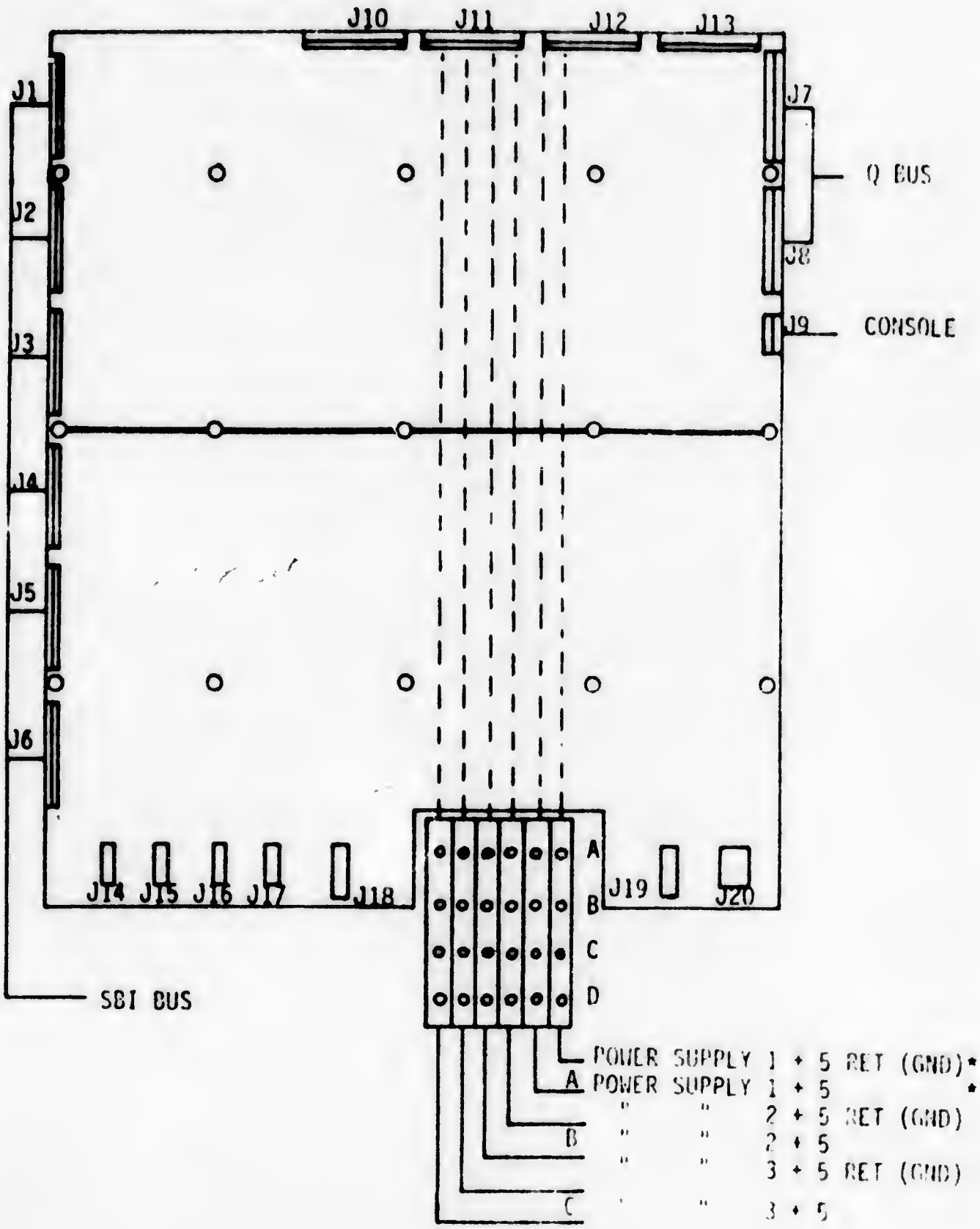


FIGURE 8

* OPTIONAL

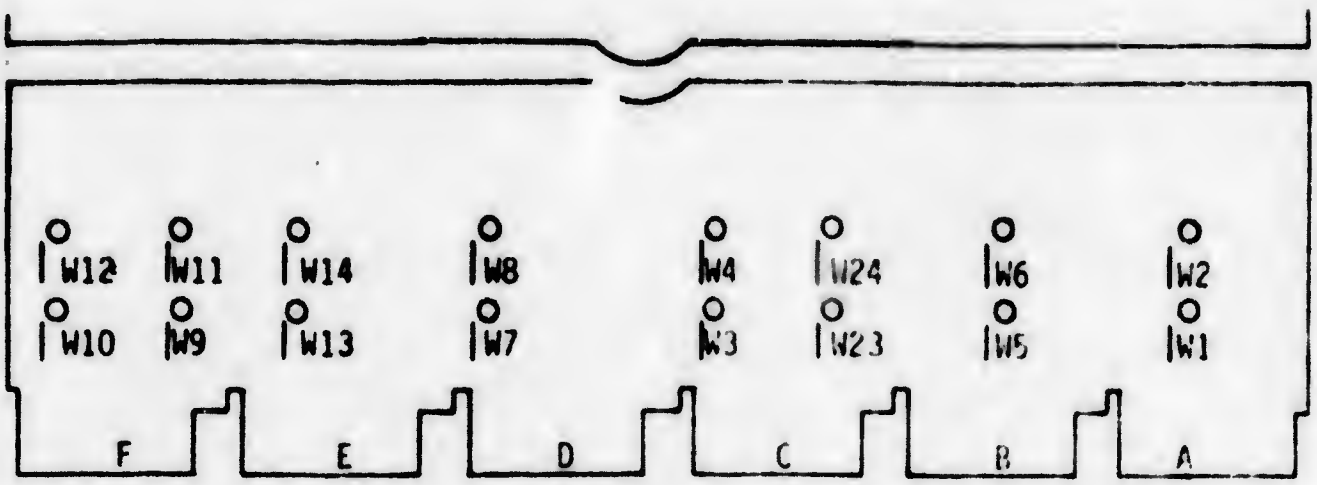


FIGURE 9 M8232

NOTE: W1 through W14=In for FPA
W23 and W24=In for WCS

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 12/30

TITLE 11/750 MAST I

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	NEW RELEASE	ML012	D. MONACO	8/19/81	David Lyttle	8/19/81

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1.0 INTRODUCTION:

1.1 The VAX-11/750 is the mid-range enhancement of the VAX-11 family. It carries with it all the architectural strengths of the VAX family including virtual addressing, both native mode and non-privileged PDP-11 compatibility mode instructions, and the VAX virtual memory operating system. The use of Gate Array Technology gives all this performance in a reliable compact 4 module CPU. The basic 11/750 is housed in a system cabinet 40in.H x 30in.D x 29in.W which includes the KA750, 256KB of memory, DD11-DK, DZ11 and TU-58 cassette tape drive.

1.2 The intent of this procedure is to establish the minimum test requirements necessary to test a VAX 11/750 CPU.

2.0 REFERENCE DOCUMENTATION:

2.1 Manuals

1.	750 Diagnostic System Overview	EK-VXD75-UG
2.	DZ11 User's Guide	EK-DZ110-UG
3.	TU58 User's Guide	EK-OTU58-UG
4.	Hardware Handbook	EB_17281-20
5.	VAX11 Architecture Handbook	EB-17580-18
6.	VAX11 Software Handbook	EB-18057-20
7.	VAX11 Technical Summary	EB-18816-20
8.	VAX Instruction Card	AV-D627A-TE
9.	750 Technical Description	EK-KA750-TD
10.	UBI Technical Description	EK-DW750-TD
11.	Memory System Tech. Des.	EK-MS750-TD
12.	Power System Tech. Des.	EK-PS750-TD
13.	750 Install. & Accept. Man.	EK-SI750-IN
14.	KC750 Microdiagnostic Tech. Man.	EK-KC750-TM
15.	Remote Diagnostics Users Guide	EK-KC750-UG

2.2 Prints

1.	11750	Field Maintenance Print Set	MP-00838
2.	KA750	Field Maintenance Print Set	MP-01024
3.	L0011	Field Maintenance Print Set	MP-00858
4.	M8728	Field Maintenance Print Set	MP-00857
5.	875	Field Maintenance Print Set	MP-01022
6.	H7104C	Field Maintenance Print Set	MP-01020
7.	H7104D	Field Maintenance Print Set	MP-01021
8.	DZ11	Field Maintenance Print Set	MP-00132

3.0 REQUIRED TEST EQUIPMENT:

3.1 VAX 11/750 with 256KB of memory.
3.2 Console terminal with E.I.A. such as an LA36 or LA120 or equivalent.
3.3 Appropriate load media.
3.4 H325 Test Connector
3.5 H3271 or H327 Test Connector
3.6 Optional test equipment

1. Oscilloscope Tektronix 465 or equivalent
2. D.V.M. accurate to .1 Vdc. at 15 Vdc..
3. KC750 (RDM module).
4. L9101 Comet Extender Module
5. W9048 Hex Extender Module

4.0 REQUIRED DIAGNOSTICS

4.1	VAX11 Hardcore Diagnostic	EVKAA.EXE
4.2	VAX11 Basic Instruction Exerciser	EVKAB.EXE
4.3	VAX11 Floating Point Instruction Exerciser	EVKAC.EXE
4.4	VAX11 Compatibility Mode Instruction Exe.	EVKAD.EXE
4.5	VAX11 Privileged Architecture CPU Cluster	EVKAE.EXE
4.6	11750 Specific CPU Cluster Exerciser	ECKAX.EXE
4.7	KA750 Cache T.B. Test	ECKAL.EXE
4.8	MS750 Memory Diagnostic	ECKAM.EXE
4.9	DW750 Diagnostic	ECCMA.EXE
4.10	Configuration Command File	CONFIG.COM
4.11	Diagnostic Supervisor	ECSAA.EXE
4.12	DZ11 8 Line Async Mux Test	EVDAA.EXE

4.13 Optional Microdiagnostics

VAX 11/750 Microdiagnostic Monitor	ECKAA.EXE
KC750 Microdiagnostic Test	ECKAF.EXE
VAX 11/750 Data Paths Microdiagnostic	ECKAH.EXE
VAX 11/750 Memory Interconnect Microdiag.	ECKAC.EXE
VAX 11/750 Memory Controller Microdiag.	ECKAD.EXE

5.0 SPECIAL INSTRUCTIONS:

5.1 Throughout this procedure, it is assumed that the user is familiar with DEC hardware, and the VAX 11/750.

5.2 Caution, no metallic jewelry should be worn while servicing this equipment, due to the high current capabilities of the power supply.

5.3 With battery backup installed, only loss of input power will invoke battery backup (turning off main breaker).

6.0 INSTALLATION & TEST SET-UP INSTRUCTIONS:

6.1 Unpacking instructions as received from High-Volume.

6.1.1 Save all boxes and packing material if it is needed to re-package a unit for shipment.

6.2 Visual checks:

6.2.1 With CPU unboxed check for problems such as (ref DEC standard 116):

A. Structural damage to cab and panels.

B. Bent or damaged backplane pins.

C. Loose power connections and broken wires.

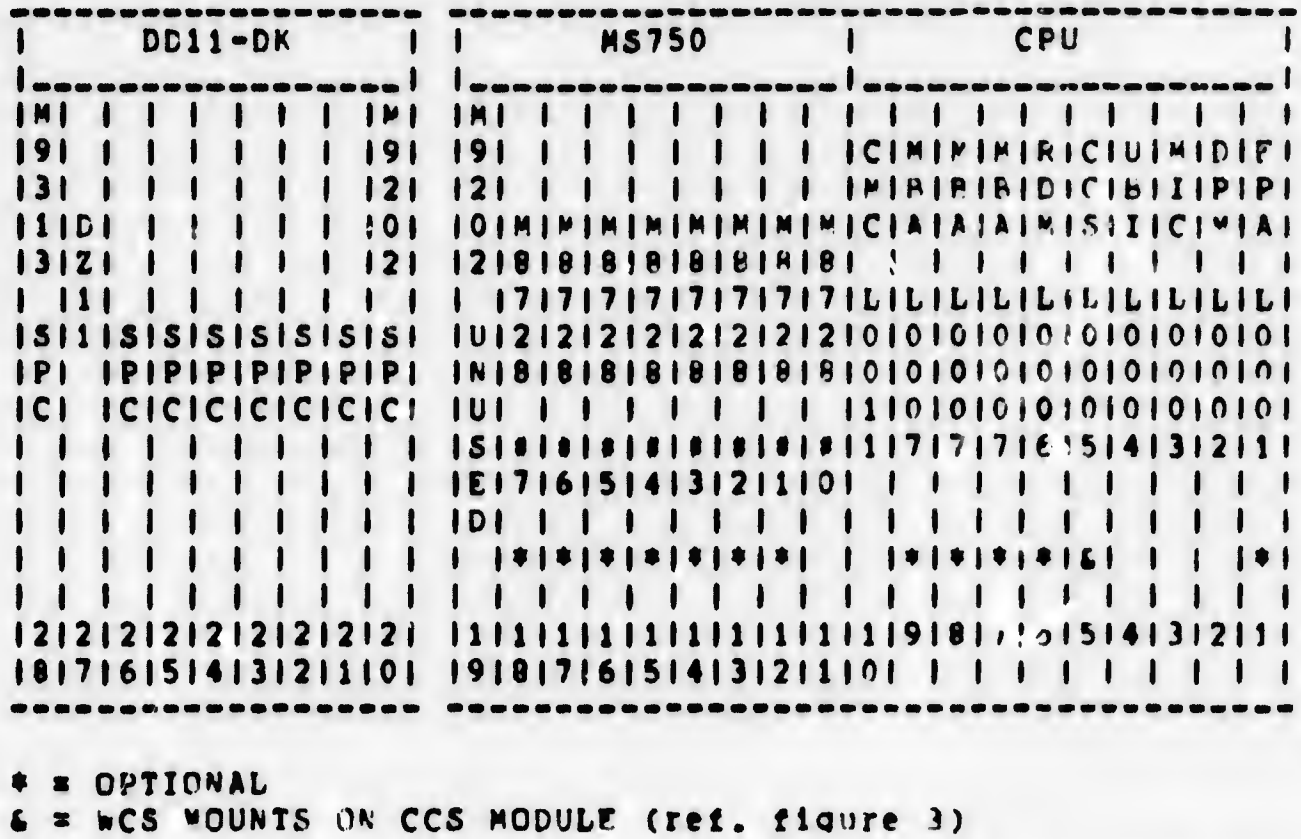
D. Loose hardware (e.g. mounting screws, cable hold downs, etc).

6.3 Hardware set up

6.3.1 KA750 Set Up

6.3.1.1 Module Utilization

11/750 MODULE UTILIZATION (module side)



* = OPTIONAL
& = WCS MOUNTS ON CCS MODULE (ref. figure 3)

NOTE: There are three methods of pin numbering and placement used in 11/750 CPU's.

PIN NUMBERING EXAMPLES:

DD11-DK	MS750	11/750
A01A1. . A01A2	A01A1. .A01A2	A0101. .A0102
A01B1 . .A01B2	A01B1. .A01B2	A0103. .A0104
A01C1. . A01C2	A01C1. .A01C2	A0105. .A0106
A01D1 . .A01D2	A01D1. .A01D2	A0107. .A0109.
A01V1. . A01V2	A01V1. .A01V2	A0193. .A0194

6.3.2 BAUD RATE SELECTION JUMPERS (ref. figure 1)

	RATE	A	B	C	D
*	300	0	0	1	0
	600	0	1	1	0
	1200	1	1	1	0
	2400	0	0	0	1
	3600	1	0	0	1
	4800	1	1	0	1
	9600	1	0	1	1
	19200	0	1	1	1
	38400	1	1	1	1
	PIN #	C00645	C00646	C00649	C00650
	JUMPER TO GND	C00643	C00644	C00651	C00652

jumper in = 1

* Denotes standard console baud rate of 11/750 as shipped from manufacturing.

6.3.3 OPTION SLOT BUS GRANT JUMPERS (ref. figure 1)

TO SELECT	REMOVE JUMPER
BG4	A00X 67
BG5	A00X 69
BG6	A00X 73
BG7	A00X 77

X=SLOT 7,8,OR 9

5.4 HARDWARE REVISION LEVEL OF SYSTEM ID

(Undefined, for future reference)

BIT	PIN
0	B00456
1	B00455
2	B00454
3	B00453
4	B00450
5	B00449
6	B00448
7	B00446

6.3.5 Verify that the TOY (Time of Year) Clock battery backup is connected to of CPU backplane. (ref. figure 6)

6.3.6 L0011 CMC Module contains 4 IC sockets for the 11/750 boot roms.(ref. figure 2)

LOCATION	DEVICE	DEVICE SELECT
* E81	TU58	A
* E82	RK07	A
* E83	RL02	C
E84	XXXX	D

*Denotes installed in High Volume.

6.3.7 DZ11 Installation (ref. figure 4 and M.A.S.T. MAV 5145).

M7819 Switch Settings

E81 Address = 160100

1	2	3	4	5	6	7	8	9	10
off	off	off	on	off	off	off	off	off	off

E11 Vector = 300

1	2	3	4	5	6	7	8
on	on	on	on	off	off	on	on

6.4 Power Conversions (ref. figure 6)

All 11/750's will be shipped from High Volume as a 11/750-AA 120 volt 50/60 HZ. Because of this the following procedure is needed to convert the 11/750-AA to a 11/750-AB 230 volt 50/60 HZ.

NOTE:
HYPOT TESTING IS REQUIRED ON UNITS THAT ARE CONVERTED. Removal of the 11/750 side panel will make access to power plugs easier.

6.4.1 Required Material

70-16707-03	Power Conversion Kit
90-07880-00	Tie Wrap (x3)
36-15180-00	Blank serial Tag (x2)
36-15946-00	Product Variation Tag (x2)

6.4.2 Required Tools

#2 Phillips Screwdriver
Allen Wrench Set
Nut Driver or Socket Set
Tie wrap Tool

6.4.3 Work Steps For Conversion

Caution:
Due to high current capability of the power supplies, disconnect from power source before proceeding.

1. Open rear door on 11/750.
2. Remove rear power supply cover.
3. Remove rear access panel.
4. Remove left side panel on 11/750.
5. Disconnect P1, P2, P3 on the top of the Power Controller, and P1 , P2 on the rear of the Power Controller, then disconnect the 2.5 volt sense cable and unplug the 70-16908-00 (115 Volt)Blower Cord.
6. Cut the Line Cord free of shipping tie wraps.
7. Remove screws securing the 70-159[illegible]-00 (115 Volt) Power Controller.
8. Remove controller by sliding it out of the rear of the cab.
7. Install the 70-15929-01 (230 Volt) Power Controller with the hardware removed in the previous steps.

8. Disconnect the 70-16908-00 (115 Volt) Blower Cord from J1 of the Blower Assembly.
9. Connect the 70-16908-01 (220 Volt) Blower Cord to J1 of the blower assembly.
10. Connect P1, P2, P3 on the top of the Power Controller, and P1 , P2 on the rear of the Power Controller, then connect the 2.5 volt sense cable and plug in the 70-16908-01 (220 Volt)Blower Cord.
11 Tie wrap Line Cord in place for shipment.
12. Replace rear power supply cover.
13. Replace 11/750 side panel.
14. Replace Rear Access Cover.
15. Change Serial Tags and install Product Variation Tags (rear door and front rail) to reflect the new version.
16. Change 11/750 ECO Status Sheet to reflect new version.

7.0 POWER CHECKS (ref. figures 5 and 7)

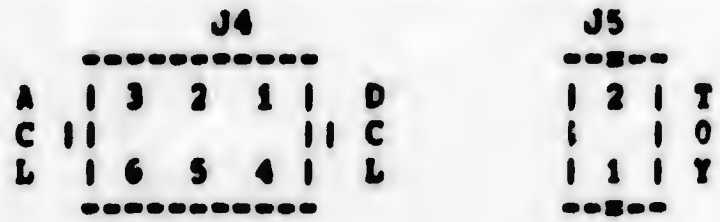
7.1 With power applied and the Rotary Key Switch on LOCAL. the following power indicators should be lit.

1. Green Power On located on Console Panel.
2. Orange power indicator on power controller.
3. Green DC OK indicator on power controller.
4. Green power indicator on memory arrays.
5. Green power indicator on memory controller.

7.2 Voltages Supplied by H7104 Power Supply. (Non adjusteble self monitored)

+2.5	V.D.C. at	85.0 amps.
+5.0	V.D.C. at	135.0 amps.
+5.0	V.D.C. at	10.0 amps.
+12.0	V.D.C. at	10.0 amps.
+15.0	V.D.C. at	2.0 amps.
-5.0	V.D.C. at	1.5 amps.
-15.0	V.D.C. at	3.5 amps.

POWER REF. FOR J1,J2,J3



7.3 Optional Battery Backup (if applicable) (ref. figure 7)

7.3.1 Optional Battery Backup is installed as shown in figure 7.

1. Mount H7112 Battery Backup on volume installed brackets in lower left of CPU cab, as viewed from the front of the CPU.
2. Connect Battery Backup cable harness to J1 (battery backup harness plate).
3. Connect P4 of Harness assembly to J11 of H7112.
4. Connect H7112 line cord to J16 (unswitched) socket of power controller.

7.3.2 There are no indicators showing the state of the Battery Backup.
The only quick check is to deposit data into memory and then shut off the main breaker (CB1), wait 60 sec then apply power and check memory contents. During the power down, power indicators on memory arrays should be lit.

7.3.3 See section 8.10 of this document for more detail testing of Battery Backup.

8.0 DIAGNOSTIC TEST PROCEDURES:

NOTE:
Reference KC750 Microdiagnostics and Technical Manual EK-KC750-TM and the Microdiagnostic listings, for detail information on installation and use of KC750 and Microdiagnostics.

For the specific sequence of diagnostics to be run in any situation, or for the current MAST minimum test criteria, e.g.: pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are the detailed step-by-step instructions for executing individual diagnostics contained in the CHECKLIST.

NO ERRORS allowed on diagnostics.

Operator inputs will be underlined.

8.1 Stand alone diagnostic cassette load (ref. figure 5)

NOTE:
It is assumed that the CPU is in a power down state.

8.1.1 Set Boot Device Selection Switch to position A (Selects TU58)

8.1.2 Set Power On Action Switch to Boot on power up.

8.1.3 Insert cassette with EVKAA.EXF HARDCORE into the TU58 located in the 11/750 console panel.

8.1.4 Set Rotary Key Switch to LOCAL.

System powers up, Power light is on Console should print %%. The first % indicates beginning the micro verify routine. The second % indicates successful completion of the micro verify. Tape motion light on TU58 comes on

8.1.5 EVKAA.EXE will load and begin running, if successfully run, console will print.

EVKAA-5.0 done!

8.1.6 Insert cassette containing ECKAL.FXE Cache TB into TU58.

8.1.7 Press the Reset Button located on the 11/750 console panel.

Console should print %% tape motion light on TU58 will turn on and tape will begin loading.

8.1.8 ECKAL.EXE will load and begin running, if successfully run, console will print.

ECKAL-2.0 DONE!

8.2 Cassette Load of Diagnostic Supervisor

8.2.1 Insert cassette containing ECSAA.EXF Diagnostic Supervisor, into the TU58.

8.2.2 Press the Reset Button located on the 11/750 console panel.

When boot is complete console will respond with the following.

```
DIAGNOSTIC SUPERVISOR, ZZ-ECSAA-5.4-121  DD-MMM-YYY
DS>
```

8.3 System Disk Load of Diagnostic Supervisor

8.3.1 Place correct media in system disk and spin disk up.

8.3.2 Set the Console Power on Action Switch to the Halt position.

8.3.3 Set the Device Select to A, B, C or D. whichever is your system device.

8.3.4 Depress the Console Reset Button, and wait for the console prompt.

8.3.5 Now type "B/10 DDCU" <CR>

Example:

```
>>>B/10 DMA0 <CR>
   --------------
```

When boot is complete console will print the following message.

```
DIAGNOSTIC SUPERVISOR, ZZ-ECSAA-5.4-121 DD-MMM-YYYY
DS>
```

8.4 Running The Diagnostic Supervisor

8.4.1 Before running any diagnostic the Diagnostic Supervisor must be configured. Following is an example of a dual RK07 11/750 system.

```
DS> ATTACH KA750 CMI KA0 NO NO YES 0 0 <CR>
    ---------------------------------------
DS> ATTACH DW750 CMI DW0 <CR>
    ------------------------
DS> ATTACH RK611 DW0 DMA 777440 210 5 <CR>
    -------------------------------------
DS> ATTACH RK07 DMA DMA0 <CR>
    ------------------------
DS> ATTACH RK07 DMA DMA1 <CR>
    ------------------------
DS> ATTACH DZ11 DW0 TTA 760100 300 5 FIA <CR>
    ----------------------------------------
DS> ATTACH VT100 TTA TTA0 <CR>
    -------------------------
```

NOTE:

These ATTACH Commands may be located in a config command procedure. To run the command procedure input the following to attach devices.

```
DS> @CONFIG <CR>
    -----------
```

8.4.2 With devices to be tested configured into the system, type the following to select all devices for test.

```
DS> SEL ALL <CR>
    ------------
```

NOTE:

It is assumed that the proper diagnostics are located on the load media being used. The following format will be used to illustrate running diagnostics under the Diagnostic Supervisor.

8.X Diagnostic name

```
DS> RUN XXXX <CR>          (how to start diagnostic.)
    -------------          (operator input indicator)
XXXXXXXXXXX                (beginning of run print out)
XXXXXXXXXXX                (special instructions)
XXXXXXXXXXX                (end of run print out)
```

8.5 EVKAB.EXE VAX Basic Instruction Exerciser.

```
DS> RUN EVKAB <CR>
    --------------
..PROGRAM: VAX Basic Instruction Exerciser, ZZ-EVKAB,
rev 2.0, 10 tests, at HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.6 EVKAC.EXE VAX Floating Point Instruction Exerciser.

```
DS> RUN EVKAC <CR>
    --------------
..PROGRAM: VAX Floating Point Instruction Exerciser,
ZZ-EVKAC, REV 1.0, 2 TESTS, AT HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.7 EVKAD.EXE VAX Compatibility Mode Instruction Exerciser.

```
DS> RUN EVKAD <CR>
    --------------
..PROGRAM: VAX Compatibility Mode Instruction Exerciser,
ZZ-EVKAD, REV 1.2, 4 TESTS, AT HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.8 EVKAE.EXE VAX Privileged Architecture Exerciser.

```
DS> RUN EVKAE <CR>
    --------------
..PROGRAM: VAX Privileged Architecture Exerciser,
ZZ-EVKAE, REV 1.0, 9 TESTS, AT HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.9 ECCBA.EXE VAX 11/750(UBI), Dw750 Diagnostic

```
DS> RUN ECCBA <CR>
    --------------
..PROGRAM: ECCBA-REV 1.0 VAX 11/750(UBI), Dw750 Diagnostic
REV 1.0 32 TESTS, AT HH:MM:SS.
TESTING: _DW0
NO UBES SELECTED. SKIPPING TEST
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.10 ECKAX.EXE VAX 11/750 Specific CPU Cluster Exerciser.

NOTE:
Install a write enabled scratch tape into TU58
after ECKAX is loaded into memory.

```
DS> LOAD ECKAX <CR>
    -------------
DS> ST/SE:ALL <CR>
    ------------
```

```
..PROGRAM: VAX 11/750 Specific CPU Cluster Exerciser - ZZ-ECKAX-1
REV 1.0 9 TESTS, AT HH:MM:SS
TESTING: _KA0

Before continuing, set the front panel switch to HALT/RESTART

Good Restart Parameter Block Subtest - This subtest
will restart itself if the RPB is properly interpreted.
Push the init switch to power fail...
$$

Bad Checksum Subtest - This subtest will halt the processor
with a halt code of 11. After this has happened the subtest
is restarted by typing S 100 <CR> on the console terminal.
Push the init switch to power fail...

$$

00000000  11
>>>S 100 <CR>
   ---------

Search for Good RPB - This subtest will restart itself
if the good RPB is found and interpreted properly.
Push the init switch to power fail...
$$

Warm start Flag Subtest - This subtest will halt the processor
with a halt code of 12. After this has happened the subtest
is restarted by typing S 100 <CR> on the console terminal.
Push the init switch to power fail...

$$

00000000  12
>>>S 100 <CR>
   ----------
```

```
Is this system equipped with battery backup?
(if no, then set the front panel switch to the Halt position)
[(NO),YES]
WARNING: The front panel switch must be in HALT
         for this test to operate properly.

HALT expected with following printout:
00006136  06
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>

00006136
>>>D/G F 100 <CR>
   --------------
>>>C <CR>
   ------

HALT expected with following printout:
0000633F  04
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
0000633F  04

>>>D/G F 100 <CR>
   --------------

>>>C <CR>
   -----
HALT expected with following printout:
0000650C  04
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
0000650C 04

>>>D/G F 100 <CR>
   --------------
>>>C <CR>
   ------

HALT expected with following printout:
00006688 0A
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
00006688  0A

>>>D/G F 100 <CR>
   --------------
>>>C <CR>
   ------
```

```
HALT expected with following printout:
00006808  0A
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
00006808  0A

>>>D/G F 100 <CR>
   ----------------
>>>C <CR>
   ------

HALT expected with following printout:
00006988  0A
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
0006988  0A

>>>D/G F 100 <CR>
   ----------------
>>>C <CR>
   ------

HALT expected with following printout:
00006B08
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
00006B08

>>>D/G F 100 <CR>
   ----------------
>>>C <CR>
   ------
Exiting WCS test, WCS last address = 0.

Exiting WCS test, WCS last address = 0.


..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.11 ECKAM.EXE M8750 Memory Diagnostic.

NOTE:
First memory array is not tested, must have 512KB for test to run.

```
DS> RUN ECKAM <CR>
    --------------
.. PROGRAM: ECKAM-REV. 1.0 M8750 MEMORY DIAGNOSTIC, REV 1.0
11 TESTS, AT HH:MM:SS

HIGHEST LONG WORD ADDRESS IS :
MEMORY MAP VALID: 00003FFF (X)
SLOT[0] IS FULLY POPULATED (256KB)
SLOT[1] IS FULLY POPULATED (256KB)
SLOT[3] IS EMPTY
SLOT[4] IS EMPTY
SLOT[5] IS EMPTY
SLOT[6] IS EMPTY
SLOT[7] IS EMPTY
ROM NUMBER: A DEVICE TYPE: DD
ROM NUMBER: B DEVICE TYPE: DM
ROM NUMBER: C DEVICE TYPE: DL
ARRAY[1] SINGLE BIT ERRORS:
      ROW 0  -  0
      ROW 1  -  0
      ROW 2  -  0
      ROW 3  -  0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.12 EVDAA.EXE DZ11 8 Line Async Mux Test

NOTE: This is an example of running internal wrap around mode (reference M.A.S.T. SP-MAV-5145 for detail testing).

```
DS> RUN EVDAA <CR>
    --------------

..PROGRAM: DZ11 8 LINE ASYNC MUX TEST,REV 2.1 21 TESTS
TESTING: _TTA

DEVICE _TTA IS BEING TESTED AS A M7819  (EIA) MODULE
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

9.0 Console Routines

9.1 Console Commands

The console prompt is the same as the VAX 11/780 ">>>" and appears at the beginning of every line.

"^P" Enter 11/750 Console mode.

"^R" Enter RDM console mode.
RDM> (with RDM installed)

>>>E Examine command

>>>D Deposit command

>>>I<CR> Init command, invalidates TB, Cache, and does Processor Init and Unitus Init.

>>>T<CR> Test command, runs micro verify microroutine explained later.

>>>S ADR<CR> Start command, The command may have
>>>S <CR> an address argument following, or a carriage return if the PC is used. The start command does an init sequence before going to IRD1 of the macro instruction pointed to by the PC.

>>>C The continue command is the same as the Start command and starts macro execution at the address in the PC.

>>>N Next command is used to single step the macro instruction after the PC is loaded.

>>>B The Boot command in this example will boot the device selected by the front panel DEVICE switch.

>>>X APT load and dump command.

9.2 Command switches for examine and deposit commands.

Size Switches

/B	sets the data size to byte
/W	sets the data size to word
/L	sets the data size to long

Function Switches

/G	GPR
/I	IPR
/P	Physcial Memory
/V	Virtual Memory
<SP>P	PSL

9.3 Command Switches for Boot Console Command.

>>>B/X<CR>	Boot device selected by front panel DEVICE SELECT switch and innibit Micro Verify Test.
>>>B/nnnn<CR>	Boot device selected by front panel DEVICE SELECT switch and pass a four digit number as software control flags to VMB.EXE in R5.
>>>B DDCU<CR>	Boot device specified by operator.

Examples:

>>>D/G/L F 1000<CR>	Put 1000 in PC.
>>>D/P 1000 00525100	Put code in address 1000.
>>>E/I 25<CR>	Examine cache disable register.
>>>I<CR>	Do an Init sequence.
>>>B/10/X DMA0<CR>	Boot Diagnostic Supervisor without micro verify from DMA0.

9.4 Console Command Error Codes.

9.4.1 If an illegal console command is attempted or command is aborted because of a microtrap or or some other condition a two digit error code is typed out and the console waits for new input.

Example:

>>>E P<CR>	Examine PSL
>>>E<CR>	Implied examine next location (illegal)
?11	Error Code typed by console.
>>>	Ready for input

Error Codes:

20 = Deposit or examine of memory failed.
(access violation, translation not valid, bus error, TB or CS parity error.)
11 = Illegal access of an IPR or PSL.
29 = Binary transfer checksum error.
33 = Attempt to boot from unknown device type.
34 = Boot device not "A", "B", C", or "D".

9.5 Console Halt Error Codes

00 = Halt command typed at console.
02 = ^p halt or single macro instruction mode.
04 = Interrupt stack not valid.
06 = Halt instruction executed.
07 = Vector Bits <1:0>=3, Halt at vector
08 = Vector Bits <1:0>=2, WCS disabled or missing
0A = Change Mode Instruction executed on Interrupt Stack.
0B = Change Mode Instruction executed and Vector Bits <1:0> not = 0.
0F = Double Bus Write Error Halt.
11 = Power up and can't find RPB, FPSI at RESTART/HALT.
12 = Power up warm start flag false FPSI at RESTART/HALT.
13 = Power up can't find good 64k of memory.
14 = Power up and booting, but bad Boot ROM.
15 = Power up and cold start flag set during boot subroutine.
16 = Power up halt FPSI at HALT position.
FF = Micro Verify Test failure.

9.6 Micro Verify

9.6.1 The Micro Verify Routine is run at power up and during Init sequences to the 11/750. At the beginning of Micro Verify a % will be outputed to the console. A successful completion will yield another % . A failure will output one of the following failure codes.

NOTE:
Refer ce KC750 Microdiagnostics and Technical Manual EK-KC750-TM and t Microdiagnostic listings for detail information on insta ation and use of KC750 if microdiagnostics are to be run.

Test Number	Test Name	Failure Code
1	R-Bus, W-Bus, D Reg Tests	@
2	M-Bus, O-Reg Test	C
3	Scratchpad Test	E
4	Explicit Addr.Test Mtemp	F
5	Explicit Addr.Test Rtemp	I
6	Explicit Addr.Test IPRs	J
7	Explicit Addr.Test GPRs	K
8	XB, IR, and OSR Test	O
9	XB, PC, and PC+Isize Test	Q
10	RNUM/D-Size Tests	R
11	RNUM/D-Size Tests	T
12	Cache Parity Error Test	X
13	TB Parity Error Test	[
14	Control Store Parity Error Test	]
15	Cache Test	^

EXAMPLE: Micro Verify Failure

```
%F      This indicates a failure of Mtemp Scratchpad
00000XXX FF  PC contains loop count or point at which
>>>          test failed and FF indicates micro
             verify failure.
```

9.7 VAX 11/750 BOOT58 Console Emulator

9.7.1 General

<location> = <value> or <register>

<value> = <number> or <shorthand>

<number> = Any nonnegative HEXADECIMAL numbe

<register> = 0...F

<shorthand> = Any of the following:
- "#" = Use last <location> specified.
- "+" = Use last <location> +1.
- "-" = Use last <location> -1.
- "@" = Use contents of last <location>.

<loc_qual> = Any of the following:
- "/P" = Physical Memory Address.
- "/G" = General Register.
- "/I" = Internal Processor Register.

<size_qual> = Any of the following:
"/L" = Longword
"/W" = Word
"/B" = Byte

<devspec> = A device spec of the form DDCU
DD = Generic device type (eg. DR)
C = Controller designator (A or B)
U = Unit number 0...9

<filespec> = A legal RT-11 filename NAME.TYPE
NAME = Any alphanumeric string of not more than 6 chars.
TYPE = Any alphanumeric string of not more than 3 chars a null is acceptable.

9.7.2 BOOT5B COMMANDS

BOOT [<devspec>]
Boot from the device specified. If no device is specified boot from default boot device. This command cannot be in an indirect command file.

DEPOSIT [<loc_qual><size_qual>] <location> <value>
Deposit <value> at location specified by <location>. The <location> is interpreted according to the qualifiers.

EXAMINE [<loc_qual><size_qual>] <location>
Displays the contents of <location> according to the qualifiers.

HELP
Displays BOOT5B HELP FILE.

LOAD <filespec>[/START:<value>]
Load a file from the boot device into memory starting at the address specified <number>. If no starting location is specified, load the file beginning at the first free location in memory.

START <value>

JMP <value>

NOTE:

All BOOT58 commands may be abbreviated to the least amount of significant characters. Since the first character of each command is unique this means all commands may be abbreviated to one character. (BOOT may be entered as "B").

Some processor registers are either read or write only. Attempting the wrong operation on such a register will yield unpredictable results.

9.8 VMB Primary Boot

9.8.1 BOOT is the program name for VMB.EXE, which is used for booting of system devices for VMS and the Diagnostic Supervisor. Following is a list of VMB errors.

%BOOT-F- Unknown processor	This indicates that the CPU is not a 11/750 or 11/780 check SID register for proper jumper configuration in the CPU type field on the backplane.
%BOOT-F-Unexpected Exception	This indicates that one of the following exceptions occurred. 1 Access Violation 2 Breakpoint Opcode 3 Reserved Operand 4 TBit Trap 5 Page Fault (TNV)
%BOOT-F-Unexpected Machine Check	This indicates some sort of Machine Check occurred. Check all adapters using console examine and deposit commands. Probably a timeout occurred.
%BOOT-F-Nonexistant Drive	Self explanatory.

%BOOT-F-Unable to locate Boot file	VMB can't find [SYSEXE] SYSBOOT.EXE or if bit 4 in R5 is set, VMB can't find [SYSMAINT]DIAGBOOT .EXE .
%BOOT-F-Bootfile not contiguous	Indicates that [SYSEXE] SYSBOOT.EXE or if bit 4 in R5 is set, [SYSMAINT] DIAGBOOT.EXE is not contiguous on system disk.
%BOOT-F-I/O error reading boot file	Indicates problem reading boot file from disk by SOIO service.

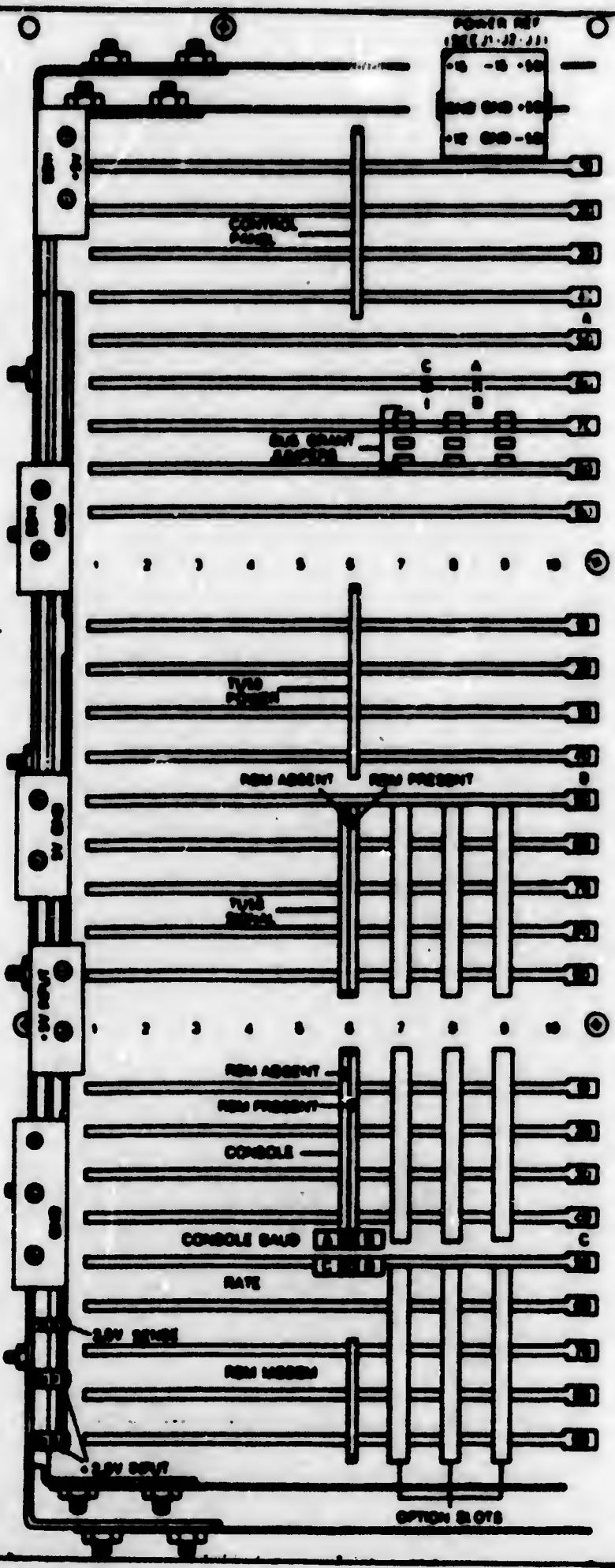


FIGURE 1
11/750 Backplane

L0011 C.M.C.

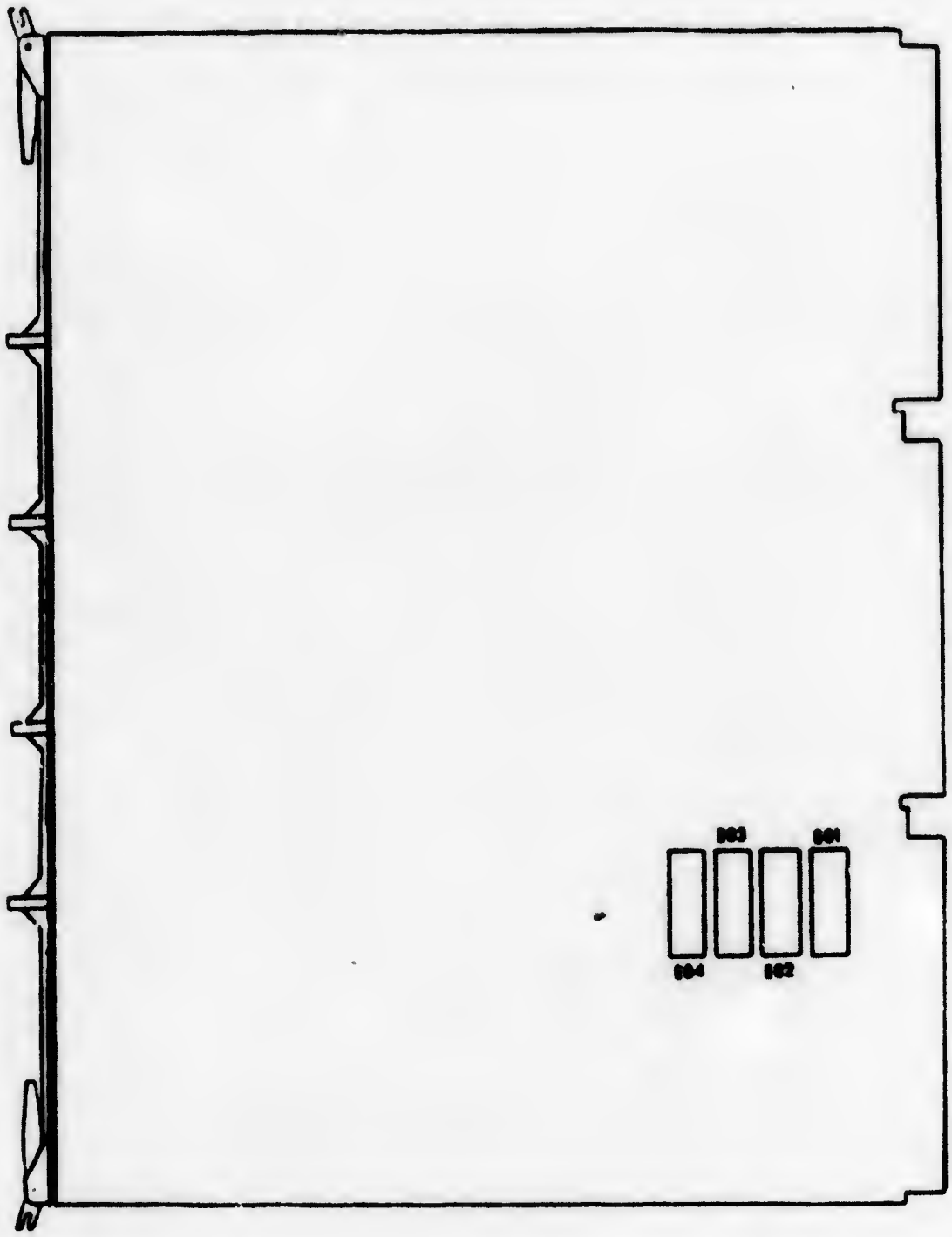


FIGURE 2
Comet Memory
Controller

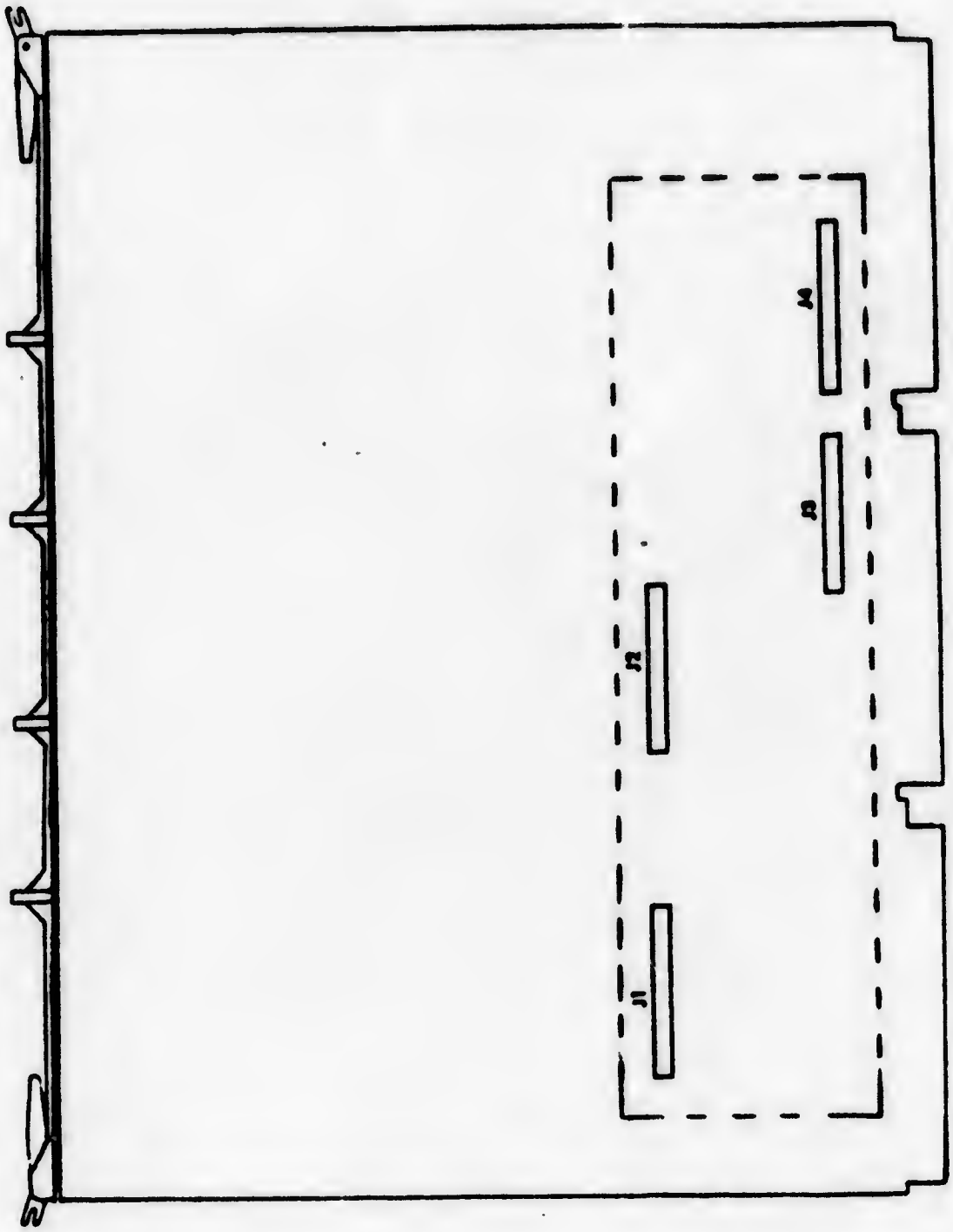


FIGURE 3
Comet Control Store
(WCS Mounted)

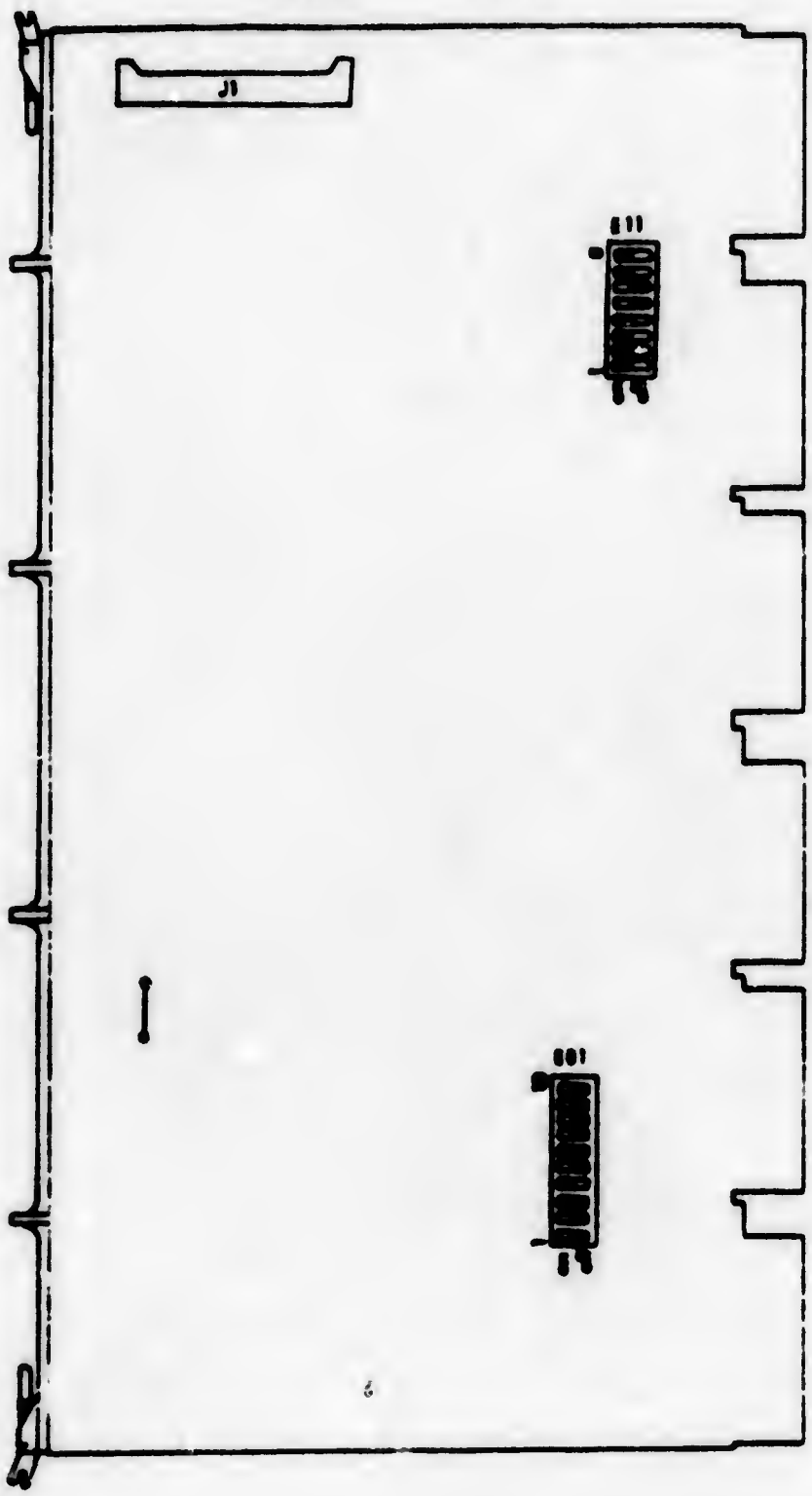


FIGURE 4
DB11-A Module

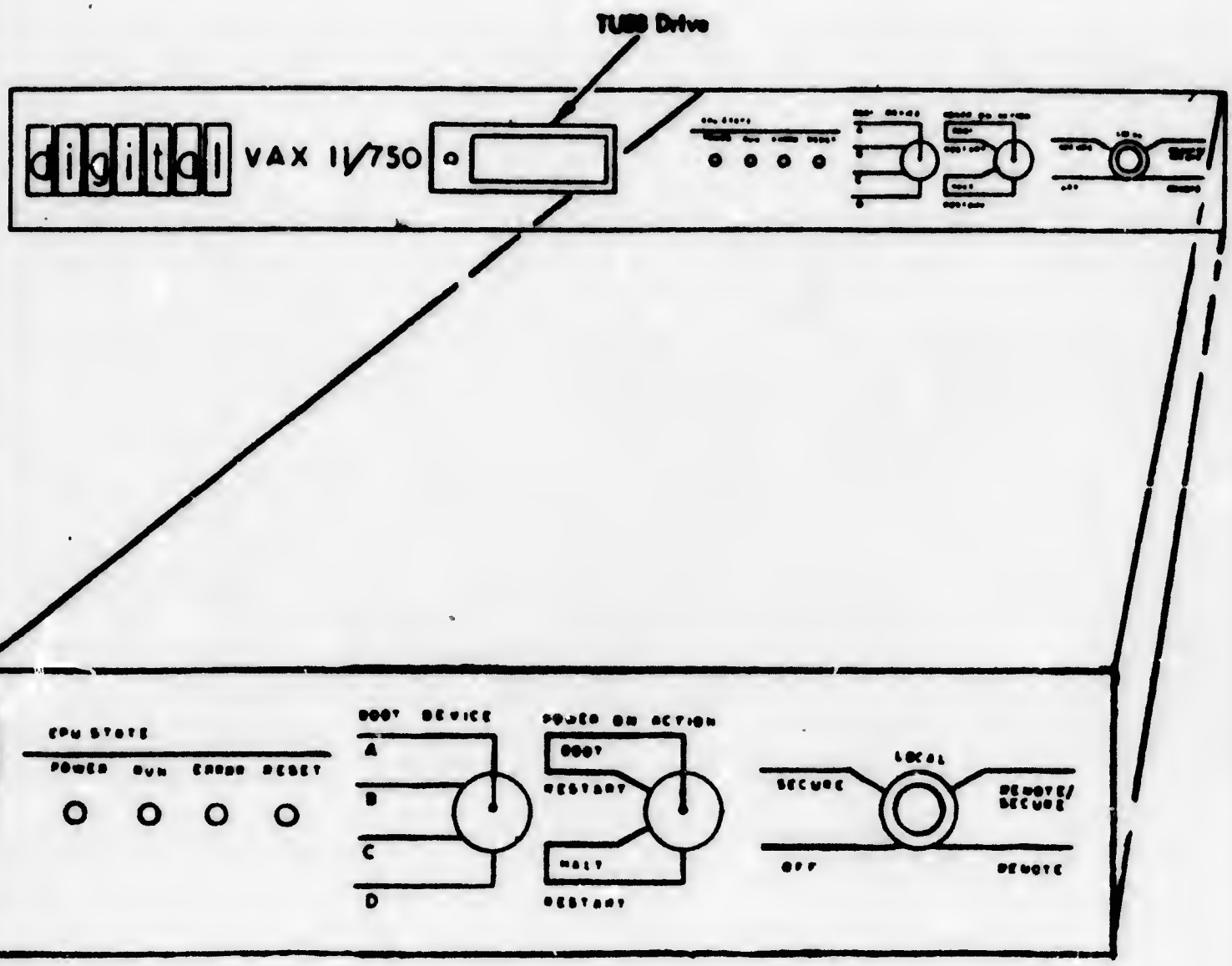


FIGURE 5
11/750 Control
Panel

TITLE MODULAR APPROACH TO SYSTEM TEST

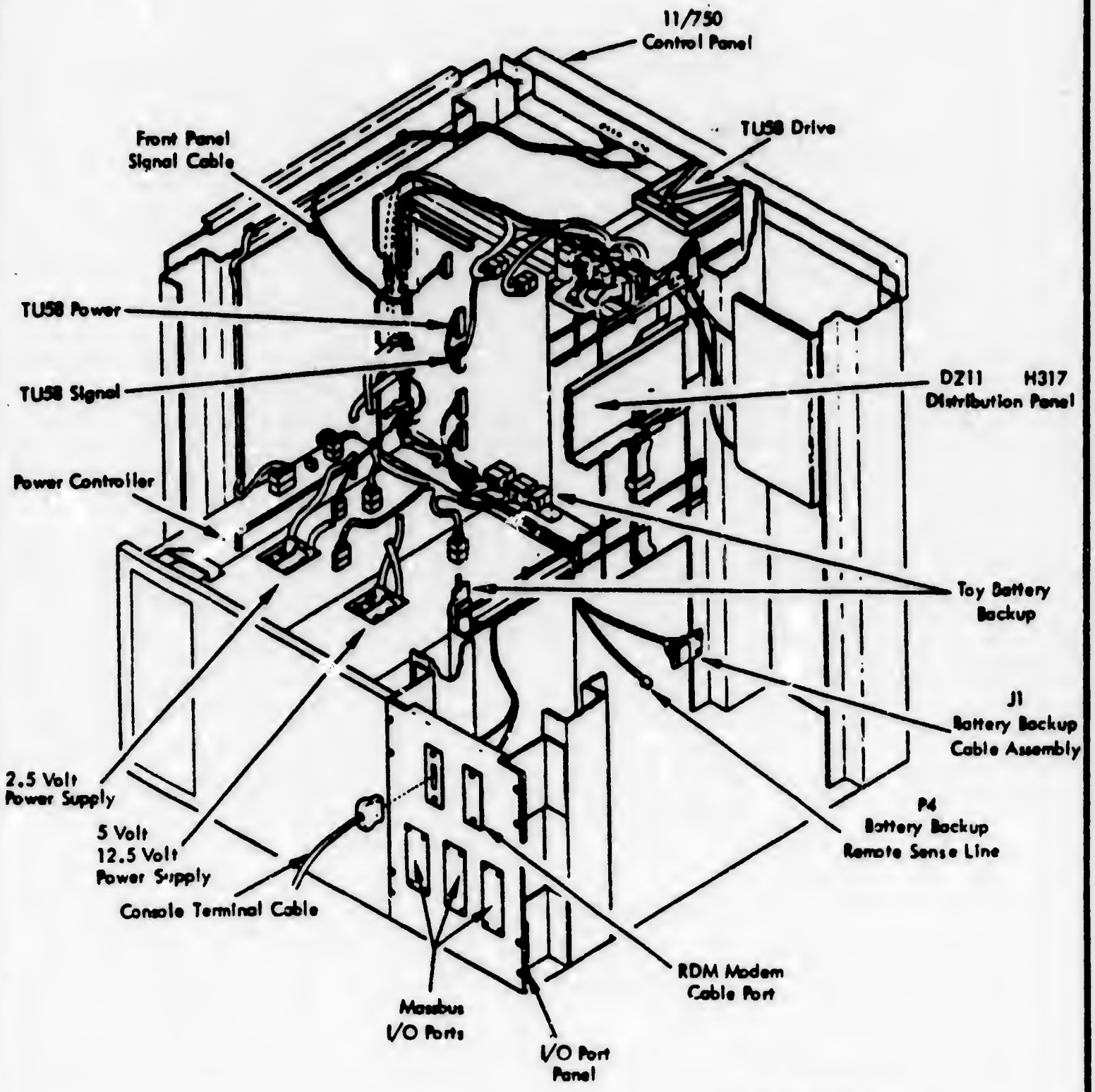


FIGURE 6
11/750 Rear View

	SIZE	CODE	NUMBER	REV
	A	SP	MAV 2102-0-0	A

DEC 16-(302)-1082-N672

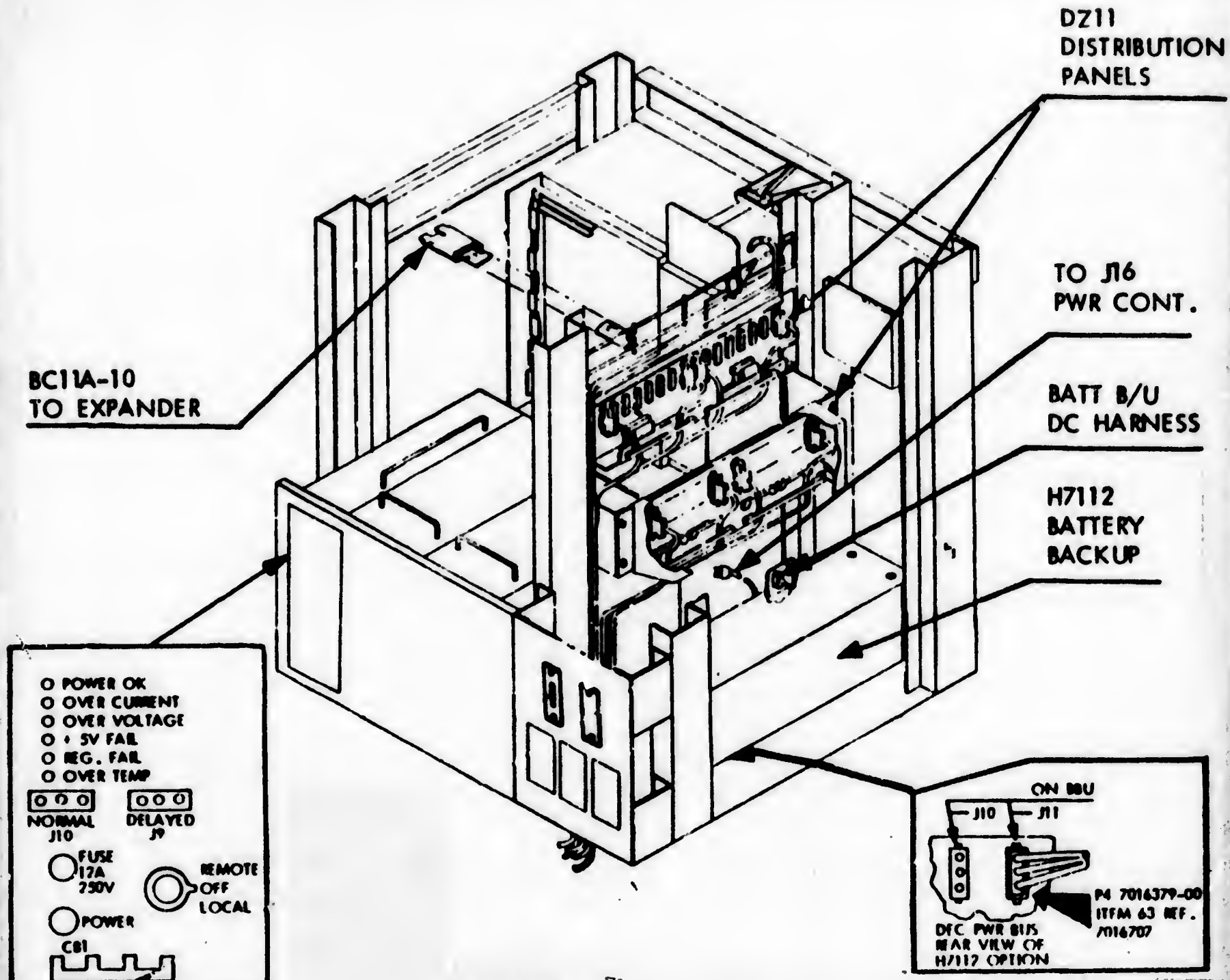


FIGURE 7

11/750 Side View
(Covers Removed)

V2-R103

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DATE 10/7/81

TITLE MAST PHASE I BACK-UP VAX 11/751 TEST

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
*	Preliminary release		D. Monaco	10/7/81	B. Beck	
A	Original release	[illegible] A0000 KL015	D. Monaco	11/9/81	B. Beck	

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Monaco	B. Beck	A	SP	MA-.2103-0-0	A

DEC FORM NO.
DRA 107A

TABLE OF CONTENTS

1.0 SCOPE:

1.1 The VAX-11/751 is an OEM version of the VAX-11/750 CPU. It carries with it all the architectural strengths of the VAX family including virtual addressing, both native mode and non-privileged PDP-11 compatibility mode instructions, and the VAX virtual memory operating system. The use of Gate Array Technology gives all this performance in a reliable compact 4 module CPU. The basic 11/751 is housed in a rack mountable unit which includes the KA750, 256KB of memory, DD11-DK, and TU-58 cassette tape drive.

1.2 The intent of this procedure is to establish the minimum test requirements necessary to test a VAX 11/751 CPU.

2.0 RESPONSIBILITY:

It is the responsibility of the of the orginator (if possible) to maintain this document. Changes should be requested through the originator, or his/her group or through MAST adminstration in SALEM (NI).

3.0 REFERENCE DOCUMENTATION:

3.1 Manuals

1.	750 Diagnostic System Overview	EK-VXD75-UG
2.	TU58 User's Guide	EK-OTU58-UG
3.	Hardware Handbook	EB_17281-20
4.	VAX11 Architecture Handbook	EB-17580-18
5.	VAX11 Software Handbook	EB-18057-20
6.	VAX11 Technical Summary	EB-18816-20
7.	VAX Instruction Card	AV-D827A-TE
8.	750 Technical Description	EK-KA750-TD
9.	UBI Technical Description	EK-DW750-TD
10.	Memory System Tech. Des.	EK-MS750-TD
11.	Power System Tech. Des.	EK-PS750-TD
12.	VAX 11/751 Users Guide	EK-11751-UG
13.	KC750 Microdiagnostic Tech. Man.	EK-KC750-TM
14.	Remote Diagnostics Users Guide	EK-KC750-UG

3.2 Prints

1. 11751 Field Maintenance Print Set MP-01258
2. KA750 Field Maintenance Print Set MP-01024
3. L0011 Field Maintenance Print Set MP-00858
4. M8728 Field Maintenance Print Set MP-00857
5. H7104C Field Maintenance Print Set MP-01020
6. H7104D Field Maintenance Print Set MP-01021

4.0 REQUIRED TEST EQUIPMENT:

4.1 Hardware and Media

4.1.1 VAX 11/751 with 256KB of memory.
4.1.2 Console terminal with E.I.A. such as an LA36 or LA120 or equivalent.
4.1.3 Appropriate load media.

4.2 Optional Equipment

4.2.1 Oscilloscope Tektronix 465 or equivalent
4.2.2 D.V.M. accurate to .1 Vdc. at 15 Vdc..
4.2.3 KC750 (RDM module).
4.2.4 L9101 Comet Extender Module
4.2.5 M9048 Hex Extender Module

5.0 REQUIRED DIAGNOSTICS:

5.1	VAX11 Hardcore Diagnostic	EVKAA.EXE
5.2	VAX11 Basic Instruction Exerciser	EVKAB.EXE
5.3	VAX11 Floating Point Instruction Exerciser	EVKAC.EXE
5.4	VAX11 Compatibility Mode Instruction Exe.	EVKAD.EXE
5.5	VAX11 Privileged Architecture CPU Cluster	EVKAE.EXE
5.6	11750 Specific CPU Cluster Exerciser	ECKAX.EXE
5.7	KA750 Cache T.B. Test	ECKAL.EXE
5.8	MS750 Memory Diagnostic	ECKAM.EXE
5.9	DW750 Diagnostic	ECCBA.EXE
5.10	Configuration Command File	CONFIG.COM
5.11	Diagnostic Supervisor	ECSAA.EXE
5.12	Optional Microdiagnostics	
	VAX 11/750 Microdiagnostic Monitor	ECKAA.EXE
	KC750 Microdiagnostic Test	ECKAF.EXE
	VAX 11/750 Data Paths Microdiagnostic	ECKAB.EXE
	VAX 11/750 Memory Interconnect Microdiag.	ECKAC.EXE
	VAX 11/750 Memory Controller Microdiag.	ECKAD.EXE

6.0 SPECIAL INSTRUCTIONS:

6.1 The 751 comes preconfigured from High Volume, minimum set up is necessary.

7.0 INSTALLATION & TEST SET-UP INSTRUCTIONS:

7.1 Unpacking instructions as received from High-Volume.

7.1.1 Save all boxes and packing material if it is needed to re-package a unit for shipment.

7.2 Visual checks:

7.2.1 With CPU unboxed check for problems such as (ref DEC standard 116):

A. Structural damage to cab and panels.

B. Bent or damaged backplane pins.

C. Loose power connections and broken wires.

D. Loose hardware (e.g. mounting screws, cable hold downs, etc).

7.3 KA750 Set Up

7.3.1 Verify Module Location.
Reference Figure 3 for Module Utilization.
Reference Figure 5 for Module Access.

NOTE: There are three methods of pin numbering used in 11/751 CPU's. (reference Table A)

TABLE A : PIN NUMBERING EXAMPLES:

DD11-DK				MS750				11/751			
A01A1	. .	A01A2		A01A1	. .	A01A2		A0101	. .	A0102	
A01B1	. .	A01B2		A01B1	. .	A01B2		A0103	. .	A0104	
A01C1	. .	A01C2		A01C1	. .	A01C2		A0105	. .	A0106	
A01D1	. .	A01D2		A01D1	. .	A01D2		A0107	. .	A0109.	
A01V1	. .	A01V2		A01V1	. .	A01V2		A0193	. .	A0194	

7.3.2 Verify BAUD RATE selection reference Table B.

TABLE B: BAUD RATE SELECTION JUMPERS:

	RATE	A	B	C	D
*	300	0	0	1	0
	600	0	1	1	0
	1200	1	1	1	0
	2400	0	0	0	1
	3600	1	0	0	1
	4800	1	1	0	1
	9600	1	0	1	1
	19200	0	1	1	1
	38400	1	1	1	1
	PIN #	C00645	C00646	C00649	C00650
	JUMPER TO GND	C00643	C00644	C00651	C00652

jumper in = 1

* Denotes standard console baud rate of 11/751
as shipped from manufacturing.
(Reference Figure 1 and Table A for backplane location)

7.3.3 Verify L0011 CMC Module contains boot roms.
(reference Table C and Figure 2) to verify.

TABLE C: BOOT ROM TABLE:

	LOCATION	DEVICE	DEVICE SELECT
*	E81	TU58	A
*	E82	RK07	B
*	E83	RL02	C
	E84	XXXX	D

*Denotes installed in High Volume.

7.3.4 Connect console terminal to CPU reference figure 8.

7.4 Power Conversions (ref. figure 6)

All 11/751's will be shipped from High Volume as a 11/751-AA 120 volt 50/60 HZ. Because of this the following procedure is needed to convert the 11/751-AA to a 11/751-AB 230 volt 50/60 HZ.

7.4.1 Required Material

70-16940-01	AC input Box
36-15180-00	Blank serial Tag (x2)
36-15946-00	Product Variation Tag (x2)

Caution:
Disconnect from power source before proceeding.

7.4.2 Conversion steps

1. Unlock CPU by loosening the shipping screw on the right side of the console panel reference figure 4.

2. Slide the 11/751 foward on it's chassis tracks until the left side of of the AC Input box is exposed.

3. In the following steps all hardware should be saved for reuse during installation.

4. Remove the the lower section of the front panel by removing the 2 screws on each side that secure it to the chassis.

5. Remove the screws securing the AC Input Box reference figure 7.

6. Disconnect power harness connections on the left side of the AC Input Box.

7. Gently slide the power controller foward being careful not to catch wires.

8. Slide the 50HZ AC Input Box into the chassis.

9. Reconnect power harness to AC Input Box.

10. Secure AC Input Box with screws previously removed.

11. Reinstall the lower front panel being careful that tabs are properly aligned.

12. Slide 11/751 back into its shipping frame and secure it with shipping screw on right side of console panel.

13. HYPOT Testing should now be done if required on converted unit, ONLY personnel TRAINED in the use of the tester should do the testing. Reference HYPOT document #7665277-0-0.

14. Change Serial Tags and install Product Variation Tags to reflect new version of CPU, reference figure 6.

15. Change 11/751 ECO Status Sheet to reflect new version 11/751-AA to 11/751-AB.

8.0 POWER CHECKS:

8.1 With power applied and the Rotary Key Switch on LOCAL. the following power indicators should be lit. These are the only power checks necessary (ref. figures 4 and 9).

1. Green Power On located on Console Panel.
2. Orange power indicator on power controller.
3. Green DC OK indicator on power controller.
4. Green power indicator on memory arrays.
5. Green power indicator on memory controller (L0011). (memory indicators are visible on modules with Module Access Covers open ref. figures 5 and 3)

8.2 Voltages Supplied by H7104 Power Supply. (reference Table D)

TABLE D 751 VOLTAGES (NON ADJUSTABLE)

VOLTAGE	TOLERANCE	CURRENT
+2.5 V.D.C.	+/- 5%	85.0 amps.
+5.0 V.D.C.	+/- 5%	135.0 amps.
+5.0 V.D.C.	+/- 5%	10.0 amps.
+12.0 V.D.C.	+/- 5%	10.0 amps.
+15.0 V.D.C.	+/- 5%	2.0 amps.
-5.0 V.D.C.	+/- 5%	1.5 amps.
-15.0 V.D.C.	+/- 5%	3.5 amps.

9.0 DIAGNOSTIC TEST PROCEDURES:

NOTE:
Reference KC750 Microdiagnostics and Technical Manual EK-KC750-TM and the Microdiagnostic listings, for detail information on installation and use of KC750 and Microdiagnostics.

NOTE:
For the specific sequence of diagnostics to be run in any particular situation, and for current M.A.S.T. minimum test criteria; pass-counts etc., refer to the appropriate M.A.S.T. CHECKLIST. Listed below are the detailed step-by-step instructions for executing individual diagnostics contained in the CHECKLIST.

NO ERRORS allowed on diagnostics.

Operator inputs will be underlined.

9.1 Stand alone diagnostic cassette load (ref. figure 9)

NOTE:
It is assumed that the CPU is in a powered down state.

9.1.1 Set Root Device Selection Switch to position A (Selects TU58)

9.1.2 Set Power On Action Switch to Boot on power up.

9.1.3 Insert cassette with EVKAA.EXE HARDCOPY into the TU58 located on the front of the 11/751.

9.1.4 Set Rotary Key Switch to LOCAL.

System powers up, Power light is on Console should print %%. The first % indicates beginning the micro verify routine. The second % indicates successful completion of the micro verify. Tape motion light on TU58 comes on

9.1.5 EVKAA.EXE will load and begin running, if successfully run, console will print.

EVKAA-5.0 done!

9.1.6 Insert cassette containing ECKAL.EXE Cache TB into TU58.

9.1.7 Press the Reset Button located on the 11/751 console panel.

Console should print %% tape motion light on TU58 will turn on and tape will begin loading.

9.1.8 ECKAL.EXE will load and begin running, if successfully run, console will print.

ECKAL-2.0 DONE!

9.2 Cassette Load of Diagnostic Supervisor

9.2.1 Insert cassette containing ECSAA.EXE Diagnostic Supervisor, into the TU58.

9.2.2 Press the Reset Button located on the 11/751 console panel.

When boot is complete console will respond with the following.

```
DIAGNOSTIC SUPERVISOR, ZZ-ECSAA-5.4-121  DD-MMM-YYY
DS>
```

9.4 Configuring The Diagnostic Supervisor

9.4.1 Before running any diagnostic the Diagnostic Supervisor must be configured. Following is an example.

```
DS> ATTACH KA750 CMI KA0 NO NO YES 0 0 <CR>
    ------------------------------------
DS> ATTACH DW750 CMI DW0 <CR>
    ------------------------
```

9.4.2 With devices to be tested configured into the system, type the following to select all devices for test.

```
DS> SEL ALL <CR>
    -----------
```

NOTE:
It is assumed that the proper diagnostics are located on the load media being used. The following format will be used to illustrate running diagnostics under the Diagnostic Supervisor.

9.X Diagnostic name

```
DS> RUN XXXX <CR>          (how to start diagnostic.)
    -------------          (operator input indicator)
XXXXXXXXXXX                (beginning of run print out)
XXXXXXXXXXX                (special instructions)
XXXXXXXXXXX                (end of run print out)
```

9.5 EVKAB.EXE VAX Basic Instruction Exerciser.

```
DS> RUN EVKAB <CR>
    -------------
..PROGRAM: VAX Basic Instruction Exerciser, ZZ-EVKAB,
rev 2.0, 10 tests, at HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

9.6 EVKAC.EXE VAX Floating Point Instruction Exerciser.

```
DS> RUN EVKAC <CR>
    -------------
..PROGRAM: VAX Floating Point Instruction Exerciser,
ZZ-EVKAC, REV 1.0, 2 TESTS, AT HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

9.7 EVKAD.EXE VAX Compatibility Mode Instruction Exerciser.

```
DS> RUN EVKAD <CR>
    -------------
..PROGRAM: VAX Compatibility Mode Instruction Exerciser,
ZZ-EVKAD, REV 1.2, 4 TESTS, AT HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

9.8 EVKAE.EXE VAX Privileged Architecture Exerciser.

```
DS> RUN EVKAE <CR>
    -------------
..PROGRAM: VAX Privileged Architecture Exerciser,
ZZ-EVKAE, REV 1.0, 9 TESTS, AT HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

9.9 ECCBA.EXE VAX 11/750(UBI), DW750 Diagnostic

```
DS> RUN ECCBA <CR>
    --------------
..PROGRAM: ECCBA-REV 1.0 VAX 11/750(UBI), DW750 Diagnostic
REV 1.0 32 TESTS, AT HH:MM:SS.
TESTING: _DW0
NO UBES SELECTED. SKIPPING TEST
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

9.10 ECKAX.EXE VAX 11/750 Specific CPU Cluster Exerciser.

NOTE:
Install a write enabled scratch tape into TU58 after ECKAX is loaded into memory.

```
DS> LOAD ECKAX <CR>
    --------------
DS> ST/SE:ALL <CR>
    -------------

..PROGRAM: VAX 11/750 Specific CPU Cluster Exerciser - ZZ-ECKAX-1
REV 1.0 9 TESTS, AT HH:MM:SS
TESTING: _KA0

Before continuing, set the front panel switch to HALT/RESTART

Good Restart Parameter Block Subtest - This subtest
will restart itself if the RPB is properly interpreted.
Push the reset switch to power fail...
%%

Bad Checksum Subtest - This subtest will halt the processor
with a halt code of 11. After this has happened the subtest
is restarted by typing S 100 <CR> on the console terminal.
Push the reset switch to power fail...

%%

00000000  11
>>>S 100 <CR>
   ---------

Search for Good RPB - This subtest will restart itself
if the good RPB is found and interpreted properly.
Push the reset switch to power fail...
%%
```

Warm start Flag Subtest - This subtest will halt the processor with a halt code of 12. After this has happened the subtest is restarted by typing S 100 <CR> on the console terminal. Push the reset switch to power fail...

%%

00000000 12
>>>S 100 <CR>

Is this system equipped with battery backup?
(if no, then set the front panel switch to the Halt position)
[(NO),YES]
WARNING: The front panel switch must be in HALT
for this test to operate properly.

HALT expected with following printout:
00006136 06
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>

00006136
>>>D/G F 100 <CR>

>>>C <CR>

HALT expected with following printout:
0000633F 04
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
0000633F 04

>>>D/G F 100 <CR>

>>>C <CR>

HALT expected with following printout:
0000650C 04
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
0000650C 04

>>>D/G F 100 <CR>

>>>C <CR>

```
HALT expected with following printout:
00006688 0A
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
00006688  0A

>>>D/G F 100 <CR>
   ---------------
>>>C <CR>
   ------

HALT expected with following printout:
00006808  0A
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
00006808  0A

>>>D/G F 100 <CR>
   ---------------
>>>C <CR>
   ------

HALT expected with following printout:
00006988  0A
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
0006988  0A

>>>D/G F 100 <CR>
   ---------------
>>>C <CR>
   ------

HALT expected with following printout:
00006B08
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
00006D09

>>>D/G F 100 <CR>
   ---------------
>>>C <CR>
   ------
Exiting WCS test, WCS last address = 0.

Exiting WCS test, WCS last address = 0.


..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

9.11 ECKAM.EXE MS750 Memory Diagnostic.

NOTE:
First memory array is not tested, must
have 512KB for test to run.

```
DS> RUN ECKAM <CR>
    --------------
.. PROGRAM: ECKAM-REV. 1.0 MS750 MEMORY DIAGNOSTIC, REV 1.0
11 TESTS, AT HH:MM:SS

HIGHEST LONG WORD ADDRESS IS :
MEMORY MAP VALID: 00003FFF (X)
SLOT(0) IS FULLY POPULATED (256KB)
SLOT(1) IS FULLY POPULATED (256KB)
SLOT(3) IS EMPTY
SLOT(4) IS EMPTY
SLOT(5) IS EMPTY
SLOT(6) IS EMPTY
SLOT(7) IS EMPTY
ROM NUMBER: A DEVICE TYPE: DD
ROM NUMBER: B DEVICE TYPE: DM
ROM NUMBER: C DEVICE TYPE: DL
ARRAY(1) SINGLE BIT ERRORS:
     ROW 0  -  0
     ROW 1  -  0
     ROW 2  -  0
     ROW 3  -  0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

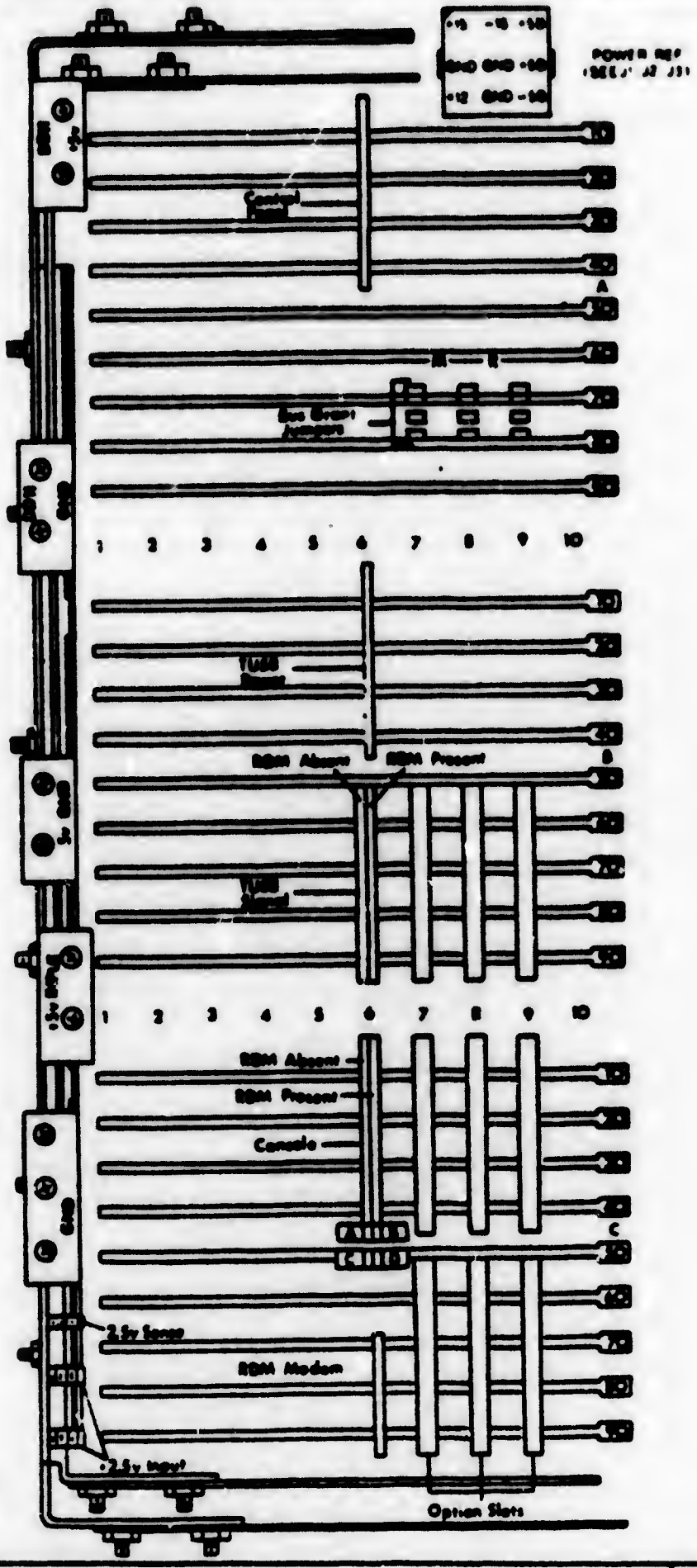


Figure 1 11/751 Backplane

M 081781-A

	SIZE	CODE	NUMBER	REV
	A	SP	MA-V2103-0-0	A

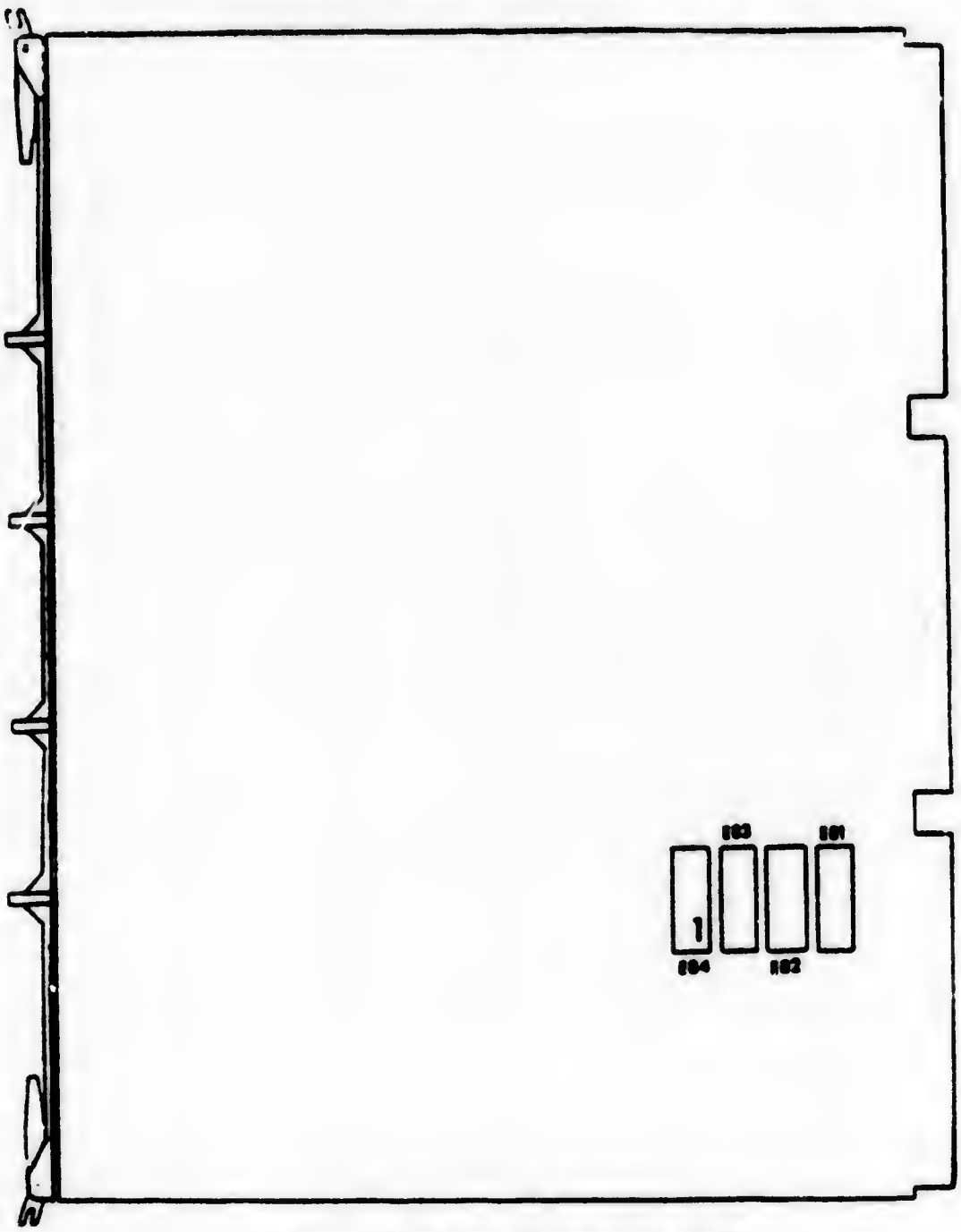


Figure 2 Comet Memory Controller

			Option (L0001 FPA)		
			L0002 DPM		
			L0003 MIC		
			L0004 LBI		
			L0005 (KU750 Option)		
			Option (L0006 RDM)		
			Option		
			Option		
			Option		
			L0011		
			MS750-AA		
			MEM Option		
			MEM Option		
			MEM Option		
			MEM Option		
			MEM Option		
			MEM Option		
	M9202				
	M9202		G727		
			G727		
			G727		
			G727		
			G727		
			G727		
			G727		
			G727		
	M9313		G727		

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28

A B C D E F

Figure 3

11/751 Module Utilization
(Front View)

ALDRICH

M 081781-A

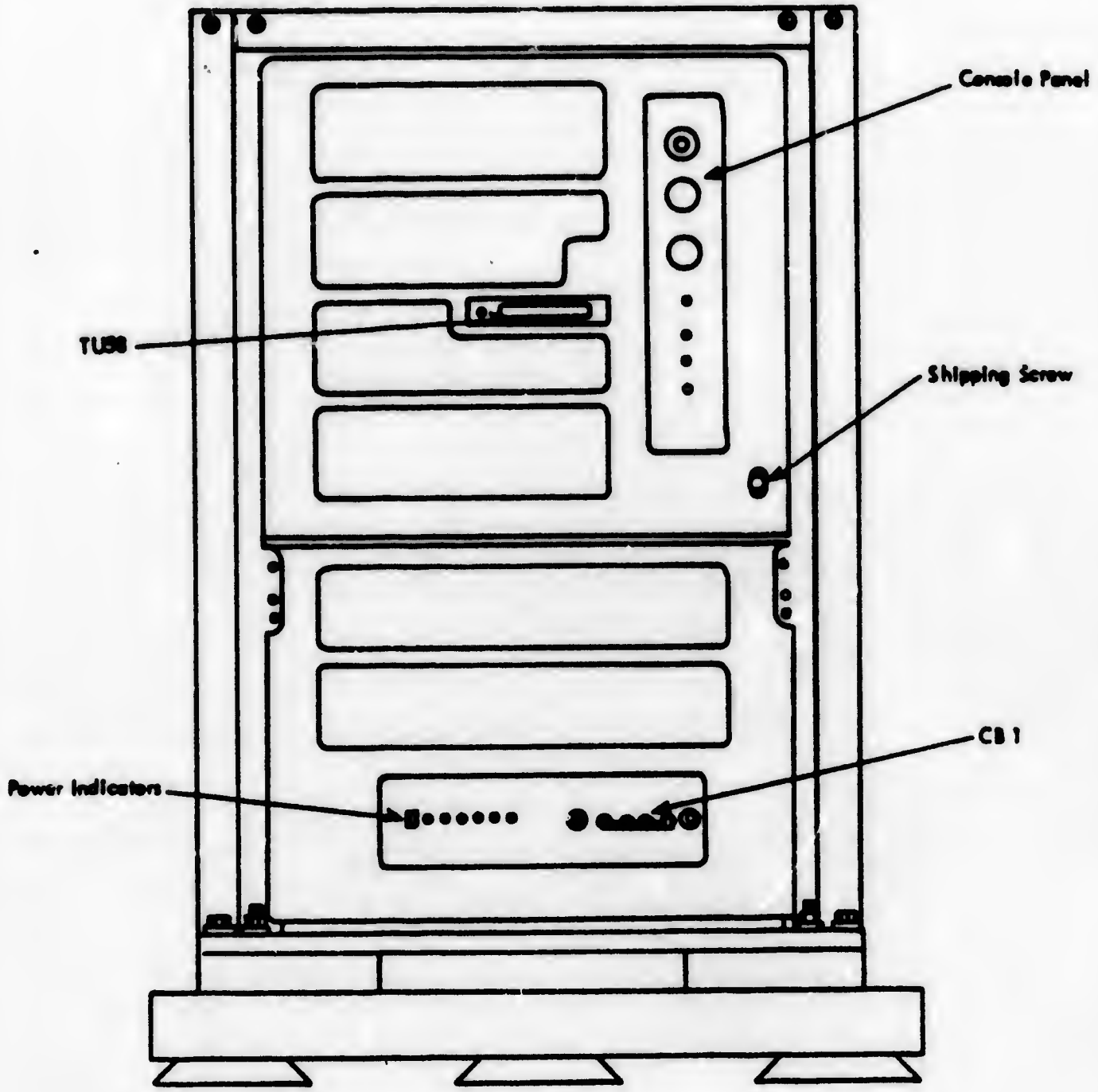


Figure 4 11/751 Front View

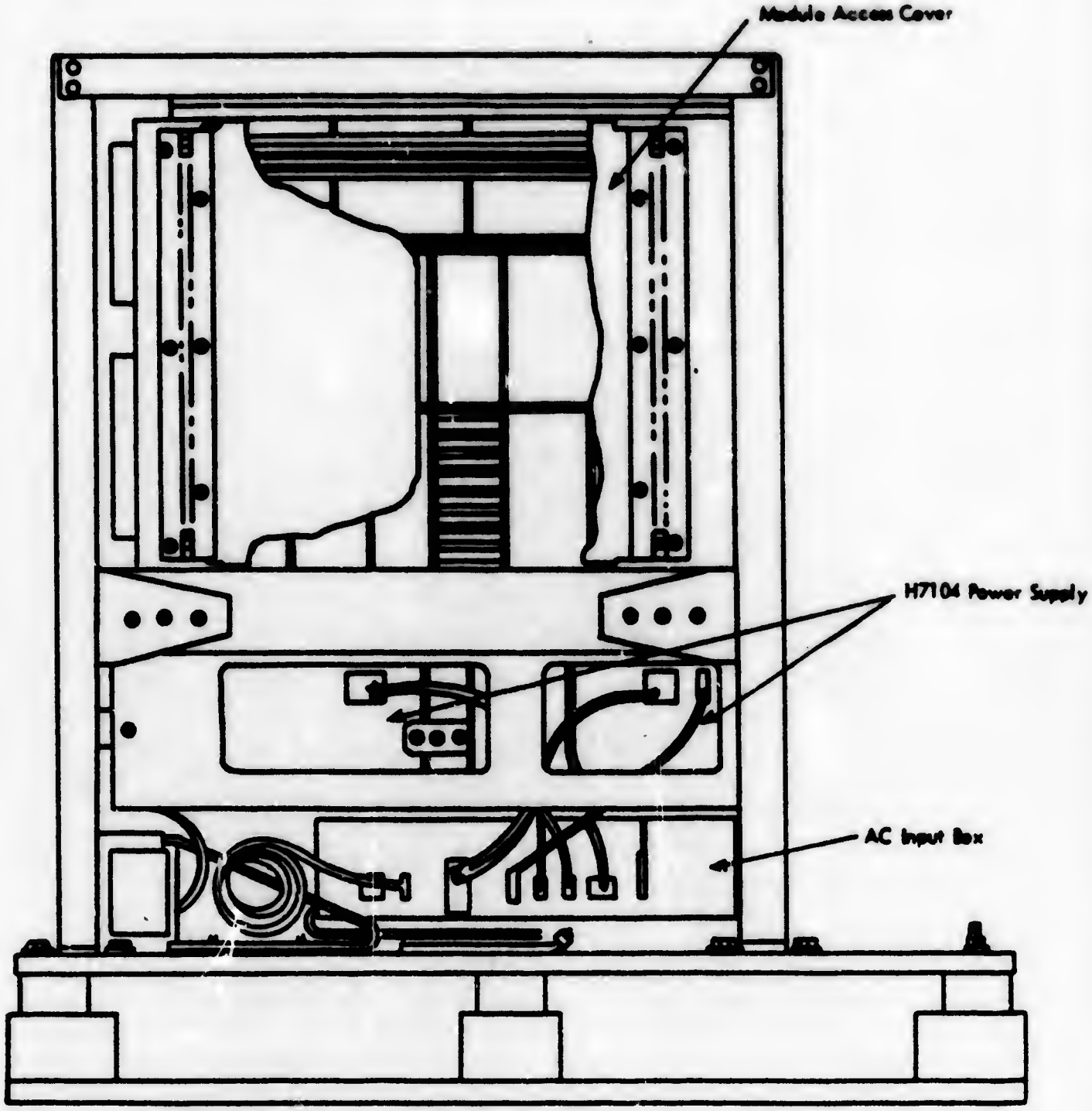


Figure 5 11/751 Side View
(Module Side)

M 081781-A

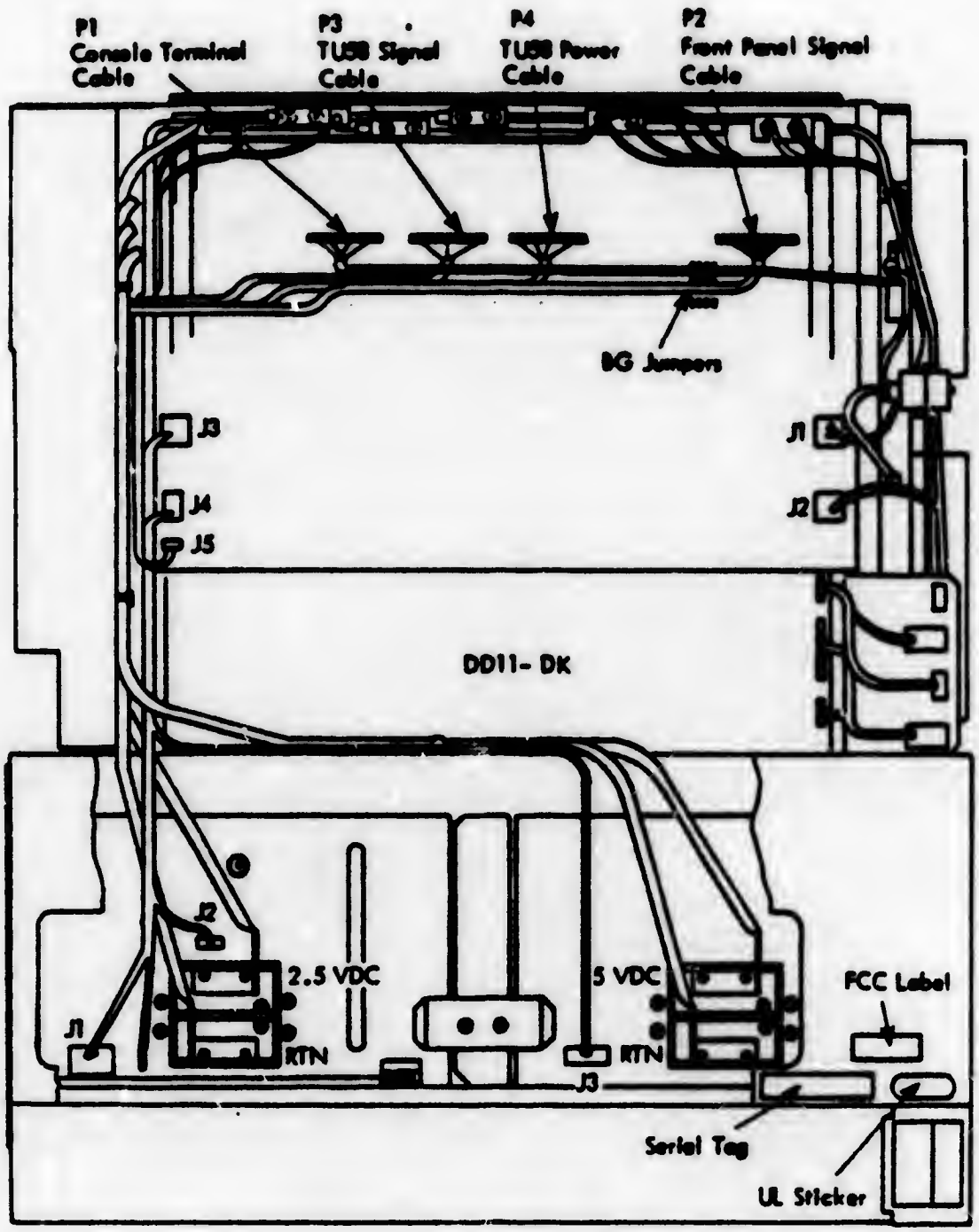


Figure 6 11/751 Side View
(Backplane Side)

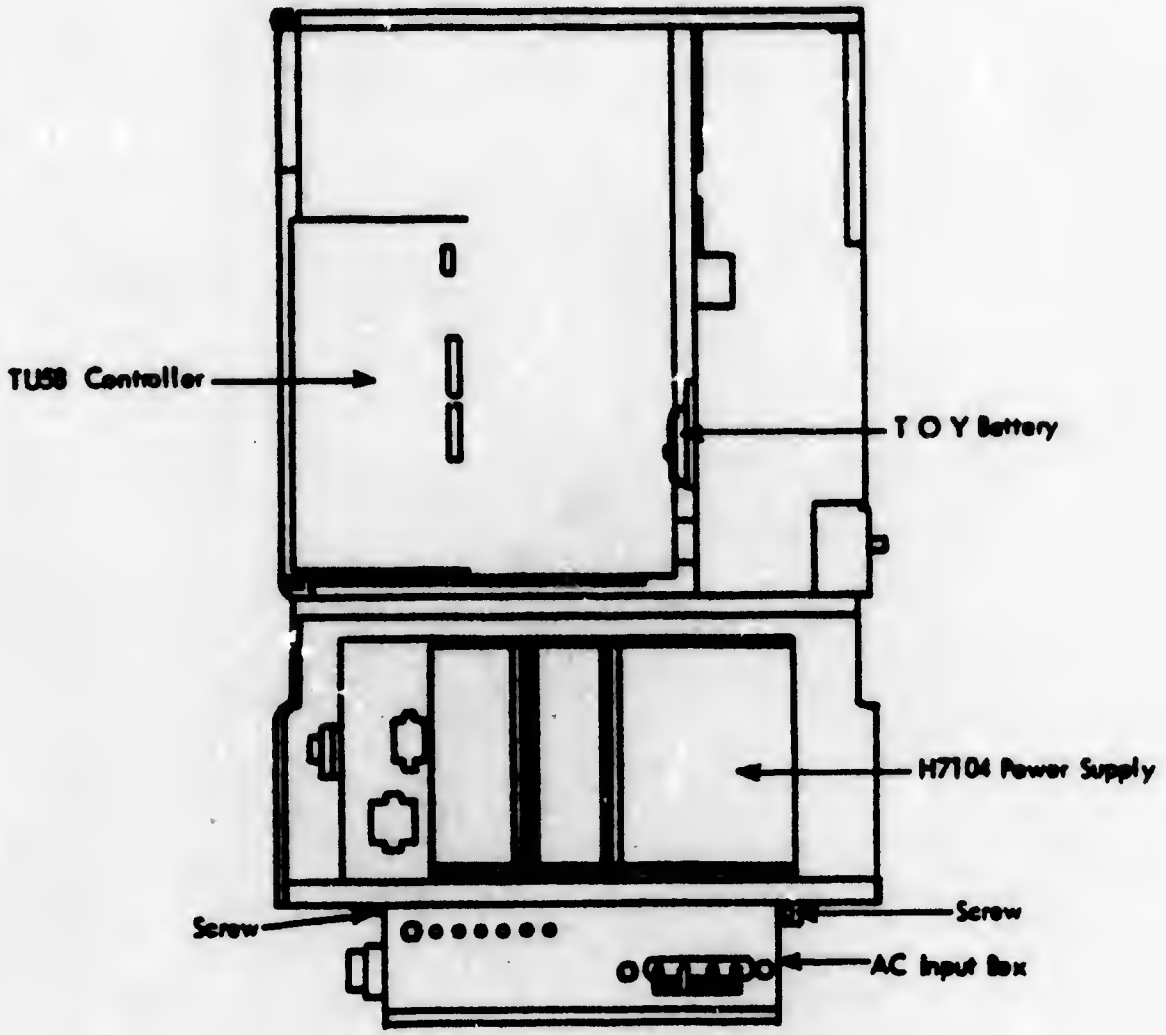


Figure 7 11/751 Front View
(Covers Removed)

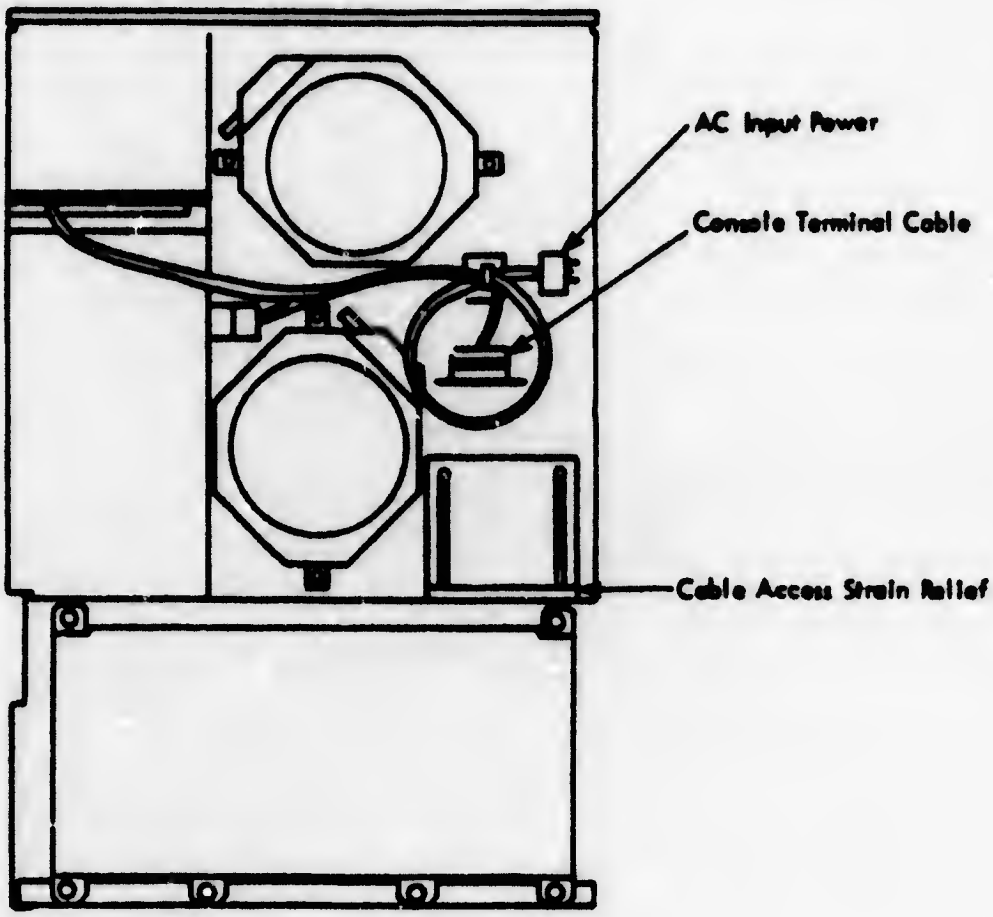


Figure 8 11/751 Rear View
(Covers Removed)

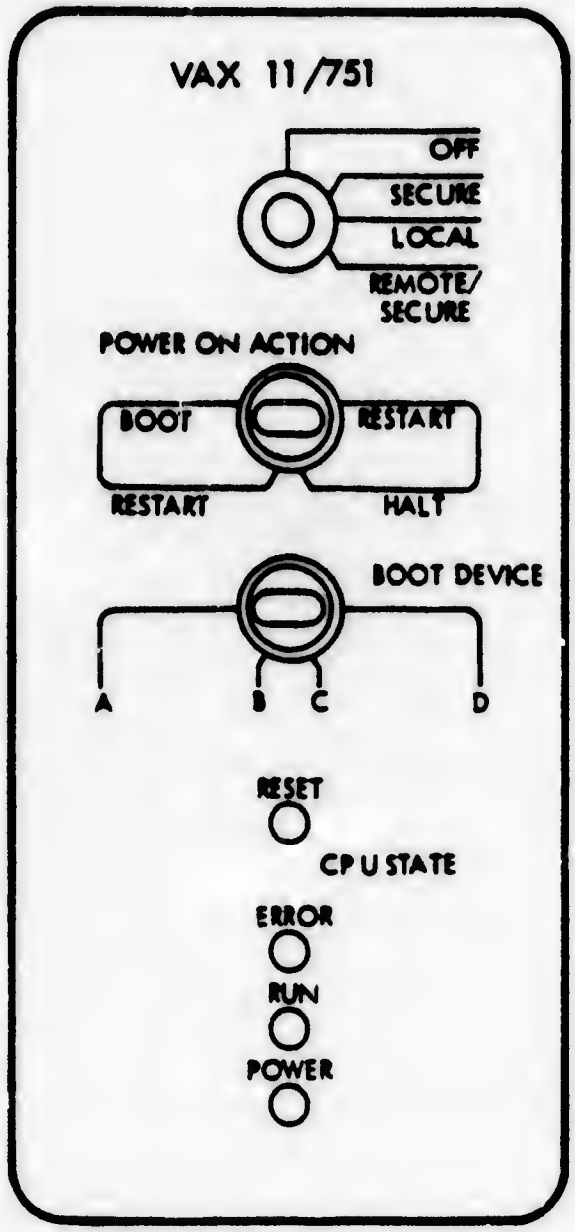


Figure 9 11/751 Console Panel

APPENDIX A Console Routines

Console Commands

The console prompt is the same as the VAX 11/780 ">>>" and appears at the beginning of every line.

"^P" Enter 11/750 Console mode from operating system.

"^P" Enter RDM mode from console mode.
RDM> (with RDM installed)

>>>E Examine command

>>>D Deposit command

>>>I<CR> Init command, invalidates TB, Cache, and does Processor Init and Unibus Init.

>>>T<CP> Test command, runs micro verify microroutine explained later.

>>>S ADR<CR> Start command, The command may have
>>>S <CR> an address argument following, or a carriage return if the PC is used. The start command does an init sequence before going to IRD1 of the macro instruction pointed to by the PC.

>>>C The continue command is the same as the Start command and starts macro execution at the address in the PC.

>>>N Next command is used to single step the macro instruction after the PC is loaded.

>>>B The Boot command in this example will boot the device selected by the front panel DEVICE switch.

>>>X APT load and dump command.

Command switches for examine and deposit commands.

Size Switches

/B sets the data size to byte
/W sets the data size to word
/L sets the data size to long

Function Switches

/G	GPR
/I	IPR
/P	Physcial Memory
/V	Virtual Memory
<SP>P	PSL

Command Switches for Boot Console Command.

>>>B/X<CR>	Boot device selected by front panel DEVICE SELECT switch and inhibit Micro Verify Test.
>>>B/nnnn<CR>	Boot device selected by front panel DEVICE SELECT switch and pass a four digit number as software control flags to VMB.EXE in R5.
>>>B DDCU<CR>	Boot device specified by operator.

Examples:

>>>D/G/L F 1000<CR>	Put 1000 in PC.
>>>D/P 1000 005251D0	Put code in address 1000.
>>>E/I 25<CR>	Examine cache disable register.
>>>I<CR>	Do an Init sequence.
>>>B/10/X DMA0<CR>	Boot Diagnostic Supervisor without micro verify from DMA0.

Console Command Error Codes.

If an illegal console command is attempted or command is aborted because of a microtrap or or some other condition a two digit error code is typed out and the console waits for new input.

Example:

>>>E P<CR>	Examine PSL
>>>E<CR>	Implies examine next location (illegal)
?11	Error Code typed by console.
>>>	Ready for input

Error Codes:

20 = Deposit or examine of memory failed. (access violation, translation not valid, bus error, TB or CS parity error.)
11 = Illegal access of an IPR or PSL.
29 = Binary transfer checksum error.
33 = Attempt to boot from unknown device type.
34 = Boot device not "A", "B", C", or "D".

Console Halt Error Codes

00 = Halt command typed at console.
02 = ^D halt or single macro instruction mode.
04 = Interrupt stack not valid.
06 = Halt instruction executed.
07 = Vector Bits <1:0>=3, Halt at vector
08 = Vector Bits <1:0>=2, *CS disabled or missing
0A = Change Mode Instruction executed on Interrupt Stack.
0B = Change Mode Instruction executed and Vector Bits <1:0> not = 0.
0F = Double Bus Write Error Halt.
11 = Power up and can't find RPB, FPS1 at RESTART/HALT.
12 = Power up warm start flag false FPS1 at RESTART/HALT.
13 = Power up can't find good 64k of memory.
14 = Power up and booting, but bad Boot ROM.
15 = Power up and cold start flag set during boot subroutine.
16 = Power up halt FPS1 at HALT position.
FF = Micro Verify Test failure.

Micro Verify

The Micro Verify Routine is run at power up and during Init sequences to the 11/750. At the beginning of Micro Verify a % will be outputed to the corsole. A successful completion will yield another % . A failure will output one of the following failure codes.

NOTE:
Reference KC750 Microdiagnostics and Technical Manual EK-KC750-TM and the Microdiagnostic listings for detail information on installation and use of KC750 if microdiagnostics are to be run.

TITLE MAST PHASE I BACK-UP VAX 11/751 TEST

Test Number	Test Name	Failure Code
1	R-Bus, W-Bus, D Reg Tests	@
2	M-Bus, Q-Reg Test	C
3	Scratchpad Test	E
4	Explicit Addr.Test Mtemp	F
5	Explicit Addr.Test Rtemp	I
6	Explicit Addr.Test IPRs	J
7	Explicit Addr.Test GPRs	L
8	XB, IR, and OSR Test	O
9	XB, PC, and PC+1size Test	Q
10	RNUM/D-Size Tests	R
11	RNUM/D-Size Tests	T
12	Cache Parity Error Test	X
13	TB Parity Error Test	[
14	Control Store Parity Error Test	]
15	Cache Test	^

EXAMPLE: Micro Verify Failure

```
%F      This indicates a failure of Mtemp Scratchpad
00000XXX FF  PC contains loop count or point at which
>>>          test failed and FF indicates micro
             verify failure.
```


V200

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE 5/1/81

TITLE FLOATING POINT ACCELERATOR

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A B	VAX 11780 Floating Point Accelerator Rewrite.	ML013	Al Gauthier	4/7/81		4/30/81

ENG	APPD	SIZE	CODE	NUMBER	REV
Al Gauthier	Bob Beck	A	SP	MAV2200-0-0	B

EN-01088-16-N6V2-(392)

FP 780 FLOATING POINT ACCELERATOR

1.0 INTRODUCTION

The Floating Point Accelerator (FPA) is an optional high speed VAX 11/780 processor extension. When included in the processor, the FPA executes the addition, subtraction, multiplication, and division instructions that operate on single, and double, precision floating point operands; including the special EMOD and POLY instructions in both single, and double-precision, formats. Additionally, the FPA enhances the performance of 32-bit integer multiply instructions.

NOTE: The FPA does not have to be installed in the 11/780 CPU in order to execute floating point operand instructions. The FPA can be added or removed without changing any existing software.

2.0 REFERENCE DOCUMENTATION

2.1 Manuals:

2.1.1	FP Accelerator Manual	EK-FP780-TD
2.1.2	Power System Overview	EK-PS780-TD
2.1.3	Diagnostic System Manual	EK-DS780-TD

2.2 Reference Listings:

2.2.1	Micro Code Listings	EP-ES0AC
2.2.2	VAX 11/780 Architecture Hndb	EB-07466
2.2.3	VAX Instruction Card	EJ-S2000

2.3 Prints:

2.3.1 FP780 MP00565

2.3.2 11/780 Complete Print Set MP00539

2.3.3 VAX 11780 CPU MAST Back-Up MAV2100-0-0

3.0 REQUIRED TEST EQUIPMENT

3.1 For test equipment, (Refer to section 3.0 in VAX 11/780 CPU MAST Back-Up) MAV2100-0-0.

3.2 Floating Point Accelerator Hardware

3.2.1 M8289 - FCT - FPA Controller

3.2.2 M8288 - FAD - Fraction Adder

3.2.3 M8287 - FML - Fraction Mul Low

3.2.4 M8286 - FMH - Fraction Mul High

3.2.5 M8285 - FNM - Fraction Normalizer

3.2.6 H7100 (A) or (B) Power Supply
(See Option Breakdown below)

FP780-AA = H7100-A (115V 60 HZ) + 5 FPA Modules
FP780-BB = H7100-B (230V 50 HZ) + 5 FPA Modules

3.3 Diagnostic Diskettes

3.3.1 RX1 Floppy Diskette AS-E633?-YE

3.3.2 RX2 Floppy Diskette AS-E158?-DE

3.3.3 RX3 Floppy Diskette AS-E159?-D

3.3.4	RX8 Floppy Diskette	AS-E161?-YE
3.3.5	RX25 Floppy Diskette	AS-F748?-YE

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 FP780 Diagnostics and Monitors:

4.1.1 Level 4 --- The following diagnostics do not require Diagnostic Supervisor.

ESKAH ---- Microdiagnostic Test #1
ESKAJ ---- Microdiagnostic Test #2

4.1. 2 Level 3 --- These Diagnostics run standalone under Diagnostic Supervisor.

NOTE: EVKAA.- This Diagnostic should be run only if operator experiences trouble with Diagnostic Supervisor.

EVKAB ---- Basic Instruction Exerciser
EVKAC ---- Floating Point Instruction Exerciser.

EVKAD ---- Compatability Mode Inst.
EVKAE ---- Privileged Architecture

5.0 SPECIAL INSTRUCTIONS

5.1 CAUTION: No metallic jewelry should be worn while servicing this equipment, due to the high current capabilities of the power supplies.

5.2 Jumper Conversion used is:

I = Jumper IN, O = Jumper OUT, X = Unimportant

Jumper Configurations are explicit or standard configuration is shown by an arrow (--------->).

5.3 In section 8.0, the user's response is underlined.

6.0 INSTALLATION AND TEST SET-UP INSTRUCTION

6.1 Hardware set-up and Configuration

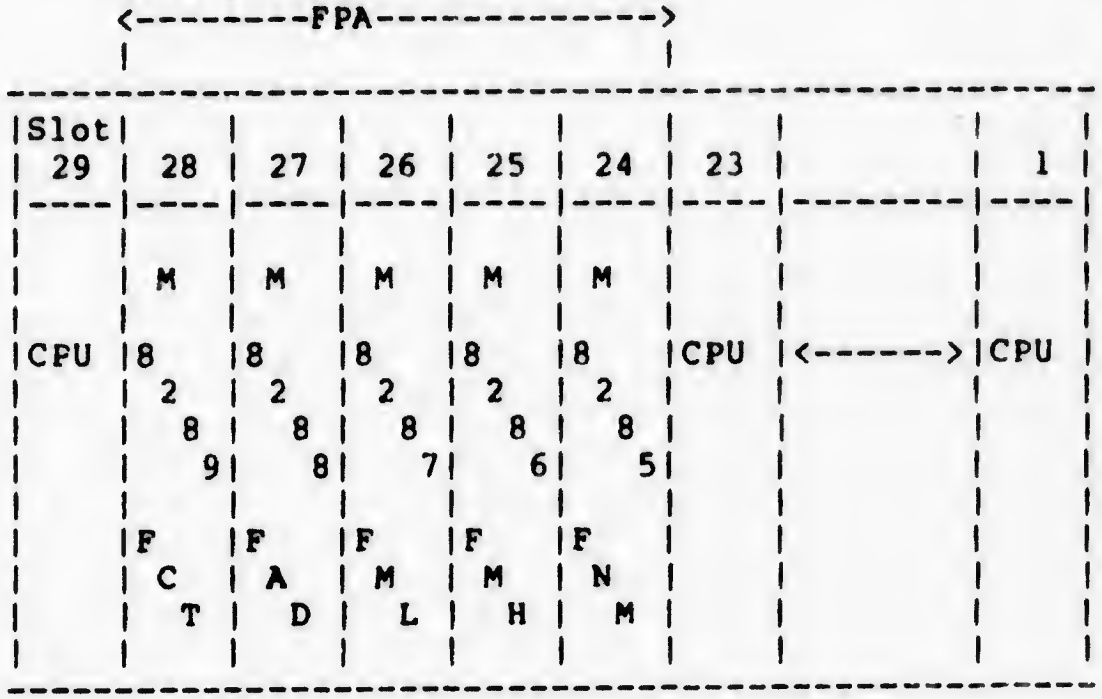
6.1.1 Perform visual inspection for obvious discrepancies, damage or potential power up problems.

CAUTION: All System power must be OFF.

6.1.2 Install Modules in proper slots of CPU. (For physical location. Refer to TABLE A.

TABLE A

Module Utilization of FPA
(viewed from module side)



6.1.3 Install Jumpers W1 to W14 on M8232 Clock Module. Refer to Figure 1.

6.1.4 Update System I.D. Register to proper Rev. level by installing/removing Jumpers on J12 & J13. Refer to Figure 3.

6.2 Installation of FPA Power Supply

CAUTION: ALL SYSTEM POWER OFF.

6.2.1 Remove top screw (front) and move slide clip left in (rear) of Power Supply Blank Cage, #70-14101-0-0.

6.2.2 Remove Power Supply Blank Cage, and insert Power Supply H7100 into #1 slot. Refer to Figure 2.

6.2.3 Move slide clip, (rear), and lock. Position top screw (front) and secure Power Supply in place.

6.2.4 For FPA installation, remove wire from +5C (B) to +5A (D) on acorn pack. Refer to Figure 3.

6.2.5 Wire backpanel (Figure 3) as shown in TABLE B.

TABLE B

FROM	TO
KA780	PS#1
+5A-A	+5V-A
+5A-B	+5V-B
+5A-C	+5V-C
+5A-D	+5V-D
+5A RET-A	+5 RET-A
+5A RET-B	+5 RET-B
+5A RET-C	+5 RET-C
+5A RET-D	+5 RET-D
AC/DC LOW PS1-J3	KA780-J17
OVERTEMP PS2-J4	PS1-J4
Move Cable PS2-J5	PS1-J5

6.3 Diskette Load

6.3.1 Release drive lock and swing out floppy drive assembly.

6.3.2 Insert diskette, RX1 Floppy, (AS-E6337-YE) into RX01 drive assembly.

6.3.3 Close diskette slot cover.

6.4 Power on/Bootstrap

6.4.1 With Main Breaker OFF, plug power cord into proper power outlet.

6.4.2 Turn 869 Power Controller Function Switch to REMOTE position.

6.4.3 With the H7111 (T.O.D.C.) LSI-11 DC, and all H7100 CKT Breakers OFF, apply power to 869 Power Controller.

6.4.4 Middle blower should be ON, with air exiting from center exhaust.

6.4.5 Turn on H7111 Time Of Day Power Supply. Power on indicator should light.

6.4.6 Power on System by Key Switch, and verify operation and air flow direction of the other two blowers.

6.4.7 Power on LSI-11, by placing DC ON/OFF Switch to ON. DC on LED should light. Place HALT/ENABLE Switch to ENABLE.

NOTE: If DC on LED is not lit, check power switch on rear of LSI-11 for ON position.

6.4.8 Set CPU Control Panel AUTO/RESTART Switch to OFF.

6.4.9 Turn on H710J CKT Breakers one at a time observing Power Indicator LED'S. Should get, green power normal indicators.

6.4.10 With Key in LOCAL position, Console program will boot.

6.4.11 Console Terminal will output message. CPU should now be ready to run diagnostics. Message is shown at 8.1.1 of this procedure.

7.0 POWER CHECKS

7.1 Observe indicator on PS#1 for power normal indication. Refer to Figure 2. Check table below for proper voltages regarding FPA on KA780 backpanel.

VOLTAGE/SIGNAL	PIN (loc on KA780 Backpanel)	RANGE
+5A	C26A1	4.9V to 5.2V
AC LOW	J17-1	-8V to -11V
DC LOW	J17-2	-8V to -11V

NOTE: Power supply is not adjustable and must be repaired or replaced if out of spec.

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 Diagnostic Check Out. Run time and pass counts are contained on M.A.S.T. checklists. No errors are allowed unless specified.

8.1.1 Console terminal will display the following message upon completion of boot.

```
CPU HALTED,SOMM CLEAR,STEP=NONE,
CLOCK=NORM
RAD=HEX,ADD=PHYS,DAT=LONG,FILL=00,
REL=00000000
INIT SEQ DONE
HALTED AT 00000000

(RELOADED WCS)
LOAD DONE, 00003200 BYTES LOADED
VER: PCS=01 WCS=0D-12 FPLA=0D
CON=V05-010-L

>>>
```

8.1.2 Remove RX1 Diskette in drive, and insert RX2 Diskette.

T<CR>

```
ZZ-ESKAB V12.0
01,02,03,04,
NO. OF WCS MODULES = 0001
05,06,07,08,09,0A,0B,0C,0D,0E,0F,10,11,12,
13,14,15,16,17,
18,19,1A,1B,1C,1D,1E,1F,20,
SYS ID REG= 01200996
21,22,23,24,25,26,27,28,29,2AA,2B,2C,2D,2E,
2F,30,31,322,33,334,35,36,37,38,39,3A,3B,3C,
3D,
END PASS 0001
MOUNT FLOPPY ZZ-ESZAD & TYPE "DI"

MIC>
```

8.1.3 Remove RX2 Diskette in drive, and insert RX3 Diskette.

DI<CR>

```
3E,
CPU TR=00000010
MS780 16K CHIP AT TR 01
  MAX ADR+1=00100000
DW780 AT TR 03
RH780 AT TR 08
RH780 AT TR 09
3F,40,41,42,43,44,45,46,47,48,49,4A,4B,4C,
4D,4E,
MS780 16K CHIP AT TR 01
  ARRAY *: 00000000
  * SINGLE BIT ERRORS:        00000000
  ARRAY *: 00000001
  * SINGLE BIT ERRORS:        00000000
  ARRAY *: 00000002
  * SINGLE BIT ERRORS:        00000000
  ARRAY *: 00000003
  * SINGLE BIT ERRORS:        00000000
4F,


MS780 16K CHIP AT TR 01
M8213 ROMS OK
50,51,52,
STARTING FPA TESTS
53,54,55,56,57,58,59,5A,5B,5C,5D,5E,5F,
END PASS 0001
        CPU HALTED,SOMM CLEAR,STEP=NONE,
        CLOCK=NORM
        RAD=HEX,ADD=PHYS,DAT=LONG,FILL=00,
        REL=00000000
        INIT SEQ DONE
        HALTED AT 00000000

        (RELOADED WCS)
        LOAD DONE, 00003200 BYTES LOADED
        VER: PCS=01 WCS=0D-12 FPLA=0D
        CON=V05-01-L


>>>
```

8.1.4 Remove RX3 Diskette and mount VAX Instruction Diagnostic #1 RX8.

```
BOOT<CR>

        CPU HALTED
        INIT SEQ DONE
        LOAD DONE, 00014200 BYTES LOADED
DIAGNOSTIC SUPERVISOR.  ZZ-ESSAA-6.1-370
8-AUG-1980 12:25:12
DS> ATT KA780 SBI KAO NO NO 0 1<CR>
DS> SEL ALL<CR>
DS> RUN EVKAB<CR>

..PROGRAM: VAX Basic Instruction Exerciser,
ZZ-EVKAB, REV 2.2, 10 TESTS, AT 12:27:37.14.
TESTING: _KAO

Accelerator type 1 is disabled.
Accelerator type 1 is enabled.
..END OF RUN. 0 ERRORS DETECTED.  PASS
COUNT: 1 TIME: 8-AUG-1980  12:29:34.74
DS>
```

8.1.5 Remove RX8 Diskette and mount Vax Inst. Diag. Diskette #2 RX25.

```
RUN EVKAC<CR>

..PROGRAM: VAX Floating Point Instruction
Exerciser, ZZ-EVKAC, REV 2.0, 3 TESTS AT
12:30:49.49.
TESTING: _KAO

Accelerator type 1 is disabled.
Accelerator type 1 is enabled.
.. END OF RUN. 0 ERRORS DETECTED.  PASS
COUNT: 1 TIME: 8-AUG-1980  12:33:04.18
DS> RUN EVKAD<CR>
```

```
.. PROGRA   VAX Compatibility Mode
Instruction Exerciser, EVKAD, REV 1.2, 4
TESTS, AT 12:33:50.37.
TESTING: _KAO

Accelerator type 1 is disabled.
Accelerator type 1 is enabled.
.. END OF RUN. 0 ERRORS DETECTED.  PASS
COUNT: 1 TIME: 8-AUG-1980  12:34:1).70
DS> RUN EVKAE<CR>

.. PROGRAM: VAX Privileged Architecture
Exerciser, EVKAE, REV 1.2, 9 TESTS, AT
12:36:06.89.
TESTING: _KAO

Accelerator type 1 is disabled.  Accelerator
type 1 is enabled.
.. END OF RUN. 0 ERRORS DETECTED.  PASS
COUNT: 1 TIME: 5-AUG-1980 11:34:55.62
DS>
```

[END OF TEST]

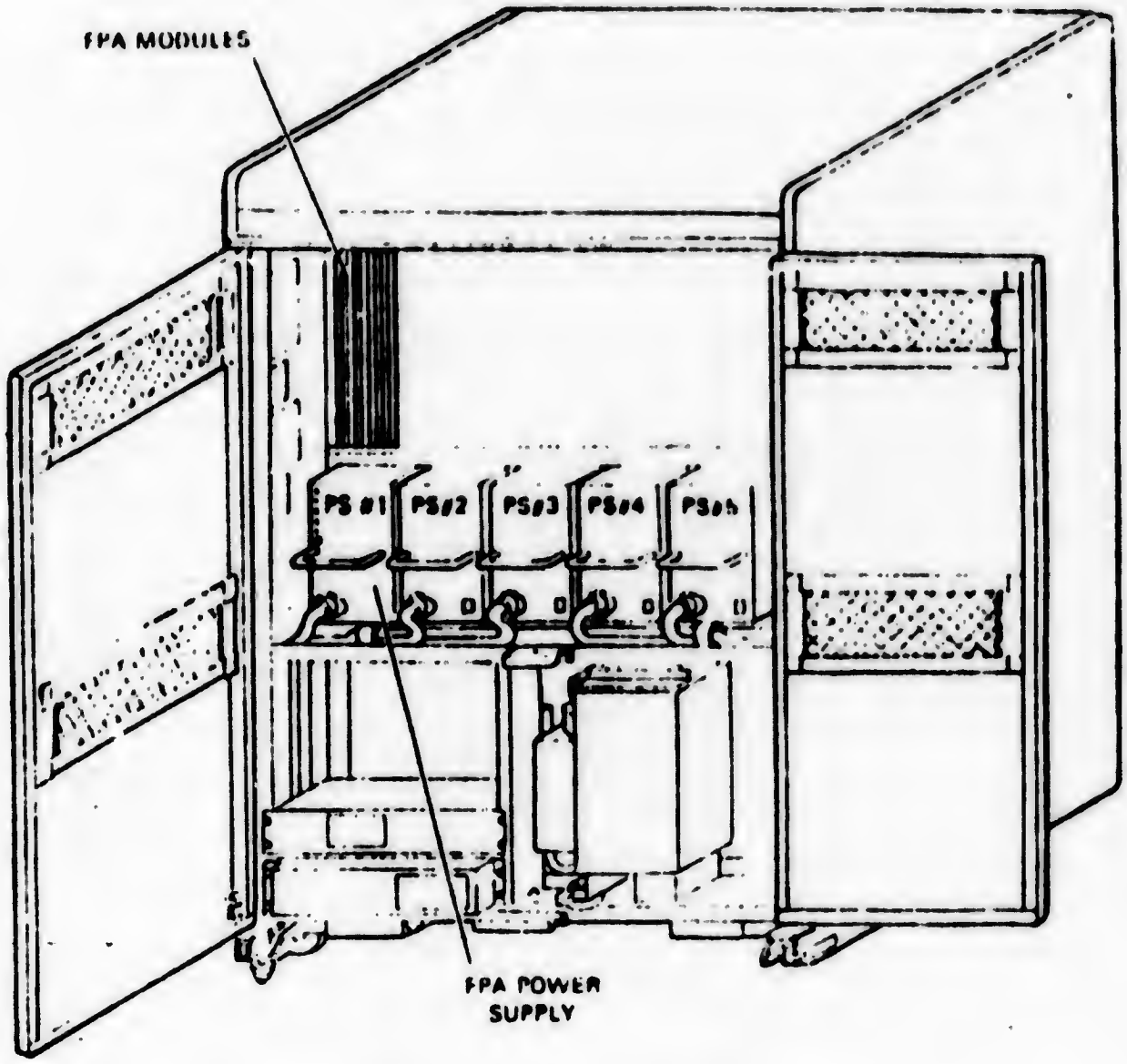


Figure 2 FPA Physical Location

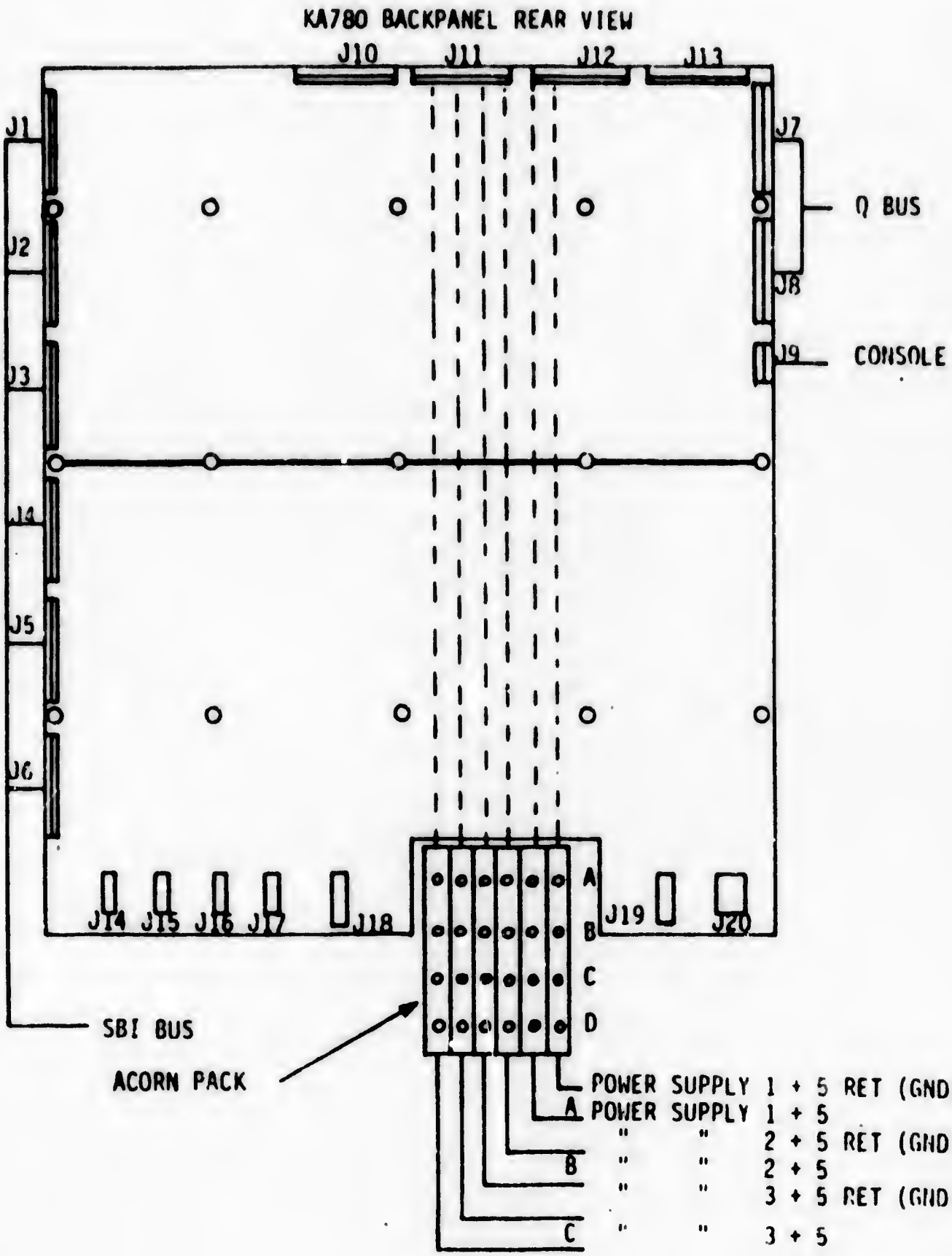


FIGURE 3

* OPTIONAL

SIZE	CODE	NUMBER	REV
A	SP	MAV2200-0-0	B

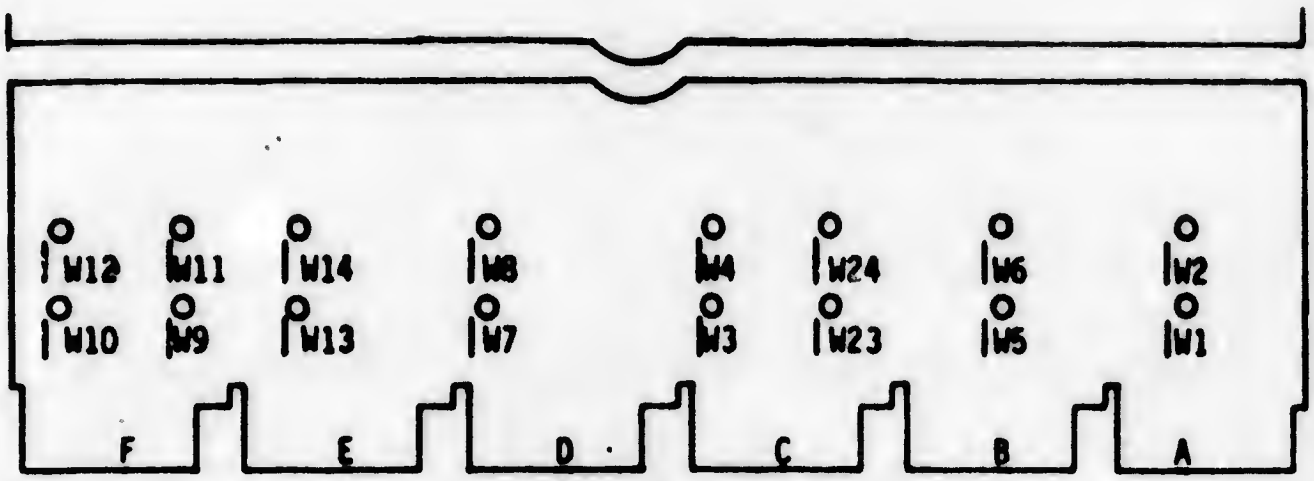


FIGURE 1 M8232

NOTE: W1 through W14=In for FPA
W23 and W24=In for WCS

V2605

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION **DATE** JUNE 11, 1981

TITLE M.A.S.T. MA780

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	New MAST procedure for MA780.	MA-A0000 ML014	D. Ayotte	6/11/81		

ENG	APPD	SIZE	CODE	NUMBER	REV
D. AYOTTE	B. BECK	A	SP	MA-V2605-0-0	A

MA780 MAST BACKUP

1.0 INTRODUCTION

1.1 The MA780 Multiport Memory Subsystem is a four-port dynamic NMOS type whose storage capacity (up to 2 megabytes) is shared by optional configurations of VAX 11780 computer systems. Access to the MA780 memory is controlled by a process of roundrobin priority arbitration. The MA780 can accommodate up to four VAX systems. The Multiport operation is consistent with VAX 11780 architecture, which requires that all cache memories are transparent to the software, and main memories can be locked on controlled boundaries. Implementation of these requirements is provided by multiport hardware that can invalidate caches and arbitrate interlocks among four System Backplane Interconnects (SBI's). The MA780 also has an interrupt mechanism for inter SBI signaling and for notification of all internal error conditions. Refer to Figures 6 and 7.

The basic multiport memory subsystem is comprised of a single array card and no invalidate map. The memory size can be expanded to 2 megabytes by adding up to a maximum of eight cards.

1.2 The following module types are used in the multiport subsystem:

M8258	Multiport Interface (MPI)
M8259	Multiport Controller (MPC)
M8260	Array Timing & Control (MAT)
M8261	Multiport Synchronizer (MPS)
M8210	Memory Array (MAY)
M8212-YA	Data Path/ECC (MDT)

2.0 REFERENCE DOCUMENTATION

2.1 MA780 Documentation

2.1.1 MA780 Technical Description EK-MA780-TD

2.1.2 MA78Ø Maint. Print Set MP88826

2.1.3 Conversion Procedure PØØ-PE-VX-A-NI-CONV

2.1.4 MA78Ø Installation Procedure EK-MA78Ø-IP

2.2 VAX Documentation

2.2.1 VAX 11/78Ø HANDBOOK EB-Ø7466

2.2.2 VAX 11/78Ø HRW HANDBOOK EB-Ø9987

2.2.3 VAX 11/78Ø SFT HANDBOOK EB-ØØ126

2.2.4 VAX 11/78Ø SYS. MAINT. GUIDE EK-1178Ø-PG

2.2.5 DS78Ø DIAG. SUPERVISOR MAN. EK-DS78Ø-UG

3.Ø HARDWARE REQUIRMENTS

3.1 TEST EQUIPMENT

3.1.1 11/78Ø with 256KB of memory

3.1.2 Console terminal

3.1.3 Scope stable at .Ø1 microsecond on X1Ø scale. (Tektronix's 475 or equiv.)

3.1.4 DVM accurate to .1 volts at +15 volts.

4.Ø DIAGNOSTICS REQUIRED

4.1 ESKAN Micro part 3

4.2 ESCCB MA78Ø Multiport Exerciser

NOTE - ESCCB ONLY RUNS WITH MULTI-CPU (2 OR MORE) CONFIGURATIONS.

5.0 SPECIAL INSTRUCTIONS

5.1 In a two (2) CPU MA780 system, one CPU will require a "Left-Hand Conversion". Refer to the Unit Assembly Drawings and the MA780 Installation Procedure for the conversion of one CPU cabinet to a left expandable CPU cabinet. Or refer to the P00-PE-VX-A-NI-CONV-Left hand conversion procedure for the VAX 11780.

6.0 HARDWARE SET UP

6.1 Systems with no SBI expander cabinet.

6.1.1 Remove the SBI far end terminator (M9043) from the CPU's that will be used in the Multiport configuration. Reference figure 1.

6.1.2 Install the interface backplane (E-IA7016512) which is a four (4) slot backplane in the space where the SBI far end terminator was located. This is done for each of the CPU's in the configuration. Reference figure 1.

6.1.3 Install in each of the CPU's an MPI (MultiPort Interface) which is an M8258 module into slot three (3) of the backplane assembly. Reference figure 2.

6.1.4 Install an M9040 (SBI far end terminator) in slot two (2) of the backplane assembly. ONLY IF THE SBI DOES NOT CONTINUE OUT TO AN EXPANDER CAB. Reference figure 2.

6.1.5 Connect six (6) SBI jumper cables from the last device in the CPU cabinet to the interface backplane. Reference figure 1.

6.1.6 Connect two M9045 paddle cards together using four (4) 70-16886-14 flat grey cables - that have the foam padding between them. Reference figure 3.

6.1.7 Insert one paddle card (M9045) into slot fo (4) on the pin side of the interface backpla of one of the CPU's. Insert the other padd card in slot 20 (pin side) of the MA780- memory interconnect. Insert the M8259 into sl 19 of the MA780-AA. Reference figure 4.

6.1.8 Repeat step 6.1.6 in order to make up the cab connection for the second CPU.

6.1.9 Insert one paddle card (M9045) in slot four of the second CPU's interface backplan Insert the other paddle card in slot 20 (p side) of the MA780-AA memory interconnec Insert the M8259 module into slot 17 of t MA780-AA. Figure 4 shows what the configur tion should look like after the two CPU's a connected to the MA780.

6.1.10 Install the MA780-C power cable assembly performing the following steps. NOTE that t installation process differs from CPU cabine and SBI expander cabinets. Refer to Figures 9, 10, and 11 for configuring one to fo ports.

A. Connect J14 of the 70-16884-00 power cab to J14 of the MA780-C backplane.

B. Connect plug J16 of the 70-16885-00 to of the MA780-C backplane.

C. Isolate, from the 70-16885-00 cable, the wires with a lug attached and install them the +5 volt side of the MS780 power supply.

NOTE - On systems where the MA780-C installed in the SBI expander cabinet the wires are installed on the BFT power supply.

D. Isolate, from plugs J14 and J16, the bl wires with a lug attached to the end install them on the ground side of the MS power supply.

NOTE - On systems where the MA780-C is installed in the SBI expander cabinet the black wires are installed on the SFT power supply.

E. Install plug J6 to J15 of the adapter next to the MA780-C assembly on the right.

F. Connect plug J7 to P3 on the CPU -5.2 volt harness.

G. Connect plug J4 to J20 of the MS780 backplane.

H. Connect J3 to J3 of the MS780 power supply.

NOTE - On systems where the MA780-C is installed in the SBI expander cabinet plug J3 is installed on the SFT power supply.

I. Plugs J1, J2, and J3 connect to the SFT backplane. These plugs are used if the MA780-C is the last device and plug into the CPU -5.2 volt harness.

J. Plug J5 is installed in the MA780 cabinet. Run the wires attached to J5 and J5 along the BDI cable tc the MA780.

6.2 System with an SBI expansion cabinet.

6.2.1 Remove the six (6) SBI jumper cables that are between the CPU and expansion cabinets.

6.2.2 Install the interface backplane in the last option slots available in the CPU cabinet.

6.2.3 Install the six (6) SBI jumpers from the last device in CPU cabinet to the interface backplane.

6.2.4 Install the MPI (M8258) module in slot one of the interface backplane.

6.2.5 Using the same procedure as in steps 6.1.7 install the BDI cables between the MA780 and the VAX 11780.

6.2.6 The far end terminator (M9Ø43) will now be located in the last slot of the expander cabinet.

6.2.7 MA78Ø Power Cable Installation - see section 6.1.1Ø.

6.3 Two MA78Ø Configuration

6.3.1 Connect one MA78Ø to one CPU following the steps section 6.1.

6.3.2 Connect the second MA78Ø to the same CPU using the same method as above using the second slot of the interface backplane.

6.4 Starting address selection

6.4.1 The following Table (A) shows the jumper configuration for the starting addresses for an MA78Ø-A. The Jumpers are located on the MA78Ø-A Backplane (J16). See Figure 5.

TABLE A

MEMORY STARTING ADDRESS JUMPERS
(USED ONLY ON POWER UP)

STRAP NAME	PORT Ø		PORT 1		PORT 2		PORT 3	
	SA23	SA22	SA23	SA22	SA23	SA22	SA23	SA22
JUMPER	W19	W2Ø	W15	W16	W11	W12	W7	W8
Ø MB	I	I	I	I	I	I	I	I
* 48 MB	-	-	-	-	-	-	-	-
32 MB	-	I	-	I	-	I	-	I
16 MB	I	-	I	-	I	-	I	-

NOTE

- = NO JUMPER
I = JUMPER INSERTED
* = STANDARD CONFIGURATION
These setting apply to all tables for jumper configurations.

Reference figure 5 for the jumper locations on the memory interconnect and the port interface.

6.5 Multi port numb.. jumpers

6.5.1 The following Table (B) shows the jumper configuration for the multi port number. The jumpers are located on the MA788-A Backplane (J16). See Figure 5.

TABLE B

MULTI PORT NUMBER JUMPER
(NUMBER VISIBLE ON CONTROL PANEL)

	PORT NUMBER	SET MULTI PORT 1 W1	SET MULTI PORT 0 W2
*	0	I	I
	1	-	I
	2	I	-
	3	-	-

* - STANDARD CONFIGURATION

6.6 TR selection

6.6.1 The following Tables (C and D) show the jumper configuration for TR select. The jumpers are located on the MA788-C Backplane (J13). Refer to Figure 5.

TABLE C
STANDARD PORT INTERFACE SLOT 3

	TR LEVEL	JUMPER W17	W18	W19	W20	WIRE WRAP F03H1 TO
	1	-	-	-	-	F03C1
*	2	-	-	-	I	F03D1
	3	-	-	I	-	F03E1
	4	-	-	I	I	F03F2
	5	-	I	-	-	F03H2
	6	-	I	-	I	F03J1
	7	-	I	I	-	F03J2
	8	-	I	I	I	F03M1
	9	I	-	-	-	F03N1
	10	I	-	-	I	F03P1
	11	I	-	I	-	F03P2
	12	I	-	I	I	F03S2
	13	I	I	-	-	F03T2
	14	I	I	-	I	F03U1
	15	I	I	I	-	F03U2

TABLE D
OPTIONAL PORT INTERFACE SLOT 2

	TR LEVEL	JUMPER W4	W3	W2	W1	WIRE WRAP F02H1 TO
	1	-	-	-	-	F02C1
	2	-	-	-	I	F02D1
*	3	-	-	I	-	F02E1
	4	-	-	I	I	F02F2
	5	-	I	-	-	F02H2
	6	-	I	-	I	F02J1
	7	-	I	I	-	F02J2
	8	-	I	I	I	F02M1
	9	I	-	-	-	F02N1
	10	I	-	-	I	F02P1
	11	I	-	I	-	F02P2
	12	I	-	I	I	F02S2
	13	I	I	-	-	F02T2
	14	I	I	-	I	F02U1
	15	I	I	I	-	F02U2

* - STANDARD CONFIGURATION

6.7 Interrupt level jumpers

6.7.1 The following Table (E) will provide the jumper configuration for the interrupt levels for the MA78Ø. The jumpers are located on the MA78Ø-C Backplane (J13). See Figure 5.

TABLE E

INTERRUPT LEVEL JUMPERS

	INTERPORT INTERRUPT LEVEL	ERROR INTERRUPT LEVEL	STANDAPD PORT SLOT 3 W16	OPTIONAL PORT SLOT 2 W5
*	4	5	-	-
	6	7	I	I

* - STANDARD CONFIGURATION

6.8 MA78Ø-D

6.8.1 Install the Invalidate Map module (M821Ø) in the 9th slot of the MA78Ø-A Memory Interconnect.

6.9 Interleaved memory

6.9.1 If MS78Ø memories are on the system and are to be interleaved the second MS78Ø MUST BE AT THE NEXT EVEN TR number past the last MA78Ø TR level.

7.Ø POWER CHECKS

7.1 For the VAX 1178Ø power requirements reference SP-MAV21ØØ-Ø·Ø.

7.2 MA780 power requirements - refer to Figure 8.

VOLTAGE	MEASURED AT	TOLERENCE
+5	PIN 1 OF J3	+/- .25VDC
-5	PIN 1 OF J1	+/- .25VDC
-5.2	PIN 4 of J1	+/- .25VDC
+12	PIN 2 OF J1	+/- 1.25VDC

8.0 DIAGNOSTICS

"For the specific sequence of diagnostics to be run in any situation, or for the current MAST minimum test criteria, e.g. pass-count, etc., refer to the appropriate MAST CHECKLIST. Listed below are the detailed step-by-step instructions for executing each individual diagnostic contained in the CHECKLIST."

All operator responses will be underlined and followed by a <CR>.

No errors allowed.

8.1 ESKAN - MICRO PART III

```
>>>T/C<CR>
ZZ-ESKAB V12.0

MIC>DI/PASS:2<CR>
3E,
CPU TR= 00000010
MS780 16K CHIP AT TR 01
   MAX ADR+1= 00080000
MA780 AT TR 02
   PORT # 00000000
DW780 AT TR 03
DR780 AT TR 0C
DR780 AT TR 0D
3F,40,41,42,43,
MA780 AT TR 02
   PORT # 00000000
  MA780 # 00000000
  MAX ADR+1= 000C0000
  INVALIDATE MAP
44,45,46,47,48,49,4A,4B,4C,4D,4E,4F,50,51,52,53,54,55,
56,57,
MA780 AT TR 02
  ARRAY #: 00000000
   # SINGLE BIT ERRORS·     00000000
  ARRAY #: 00000001
   # SINGLE BIT ERRORS:     00000000
  ARRAY #: 00000002
   # SINGLE BIT ERRORS·     00000000
  INVALIDATE MAP
   # SINGLE BIT ERRORS·     00000000
58,59,5A,5B,5C,5D,5E,5F,60,61,62,63,
MA780 AT TR 02
   SKIPPING PWR FAIL TEST

END PASS 0001

NOTE - NO ERRORS ARE ALLOWED.
```

```
NOTE - ONLY RUN ESCCB IF YOUR SYSTEM HAS TWO OR MORE
CPU'S.

8.2  ESCCB ..... MA780 MULTI-PORT MEMORY EXERCISOR

>>> B<CR>

     CPU HALTED
     INIT SEQ DONE
     LOAD DONE, 00014200 BYTES LOADED
DIAGNOSTIC SUPERVISOR. ZZ-ESSAA-6.1-370 27-MAR-1980
DS> LOAD ESCCB<CR>
DS> ATT MA780<CR>
Device Link? SBI<CR>
Device Name? MA0<CR>
TR? 2<CR>
BR? 4<CR>
MPM? 0<CR>
PORT? 1<CR>
DS> SET ALL<CR>
DS> START<CR>

.  PROGRAM: ZZ-ESCCB MA780 MULTI-PORT MEMORY EXERCISOR
TESTING: _MA0

 SBI BUS CONFIGURATION
   TR     DEVICE
NUMBER     TYPE                 MISCELLANEOUS

     1(D)              MS780     S T A R T I N G
     ADDRESS=00000000(X)
                       ENDING ADDRESS=  000EFFFF(X)
                       MEMORY SIZE= 983040(D) BYTES
     2(D)              MA780     MPM= 0(D) PORT= 1(D)
                       STARTING ADDRESS= 03000000(X)
                       ENDING ADDRESS=   030BFFFF(X)
                       MEMORY SIZE= 786432 (D) BYTES
                       INVALIDATION MAP IS PRESENT
     3(D)              DW780     UBA NUMBER= 0(D)
     4(D)              NO RESPONSE
     5(D)              NO RESPONSE
     6(D)              NO RESPONSE
     7(D)              NO RESPONSE
     8(D)              RH780
     9(D)              NO RESPONSE
     10(D)             NO RESPONSE
```

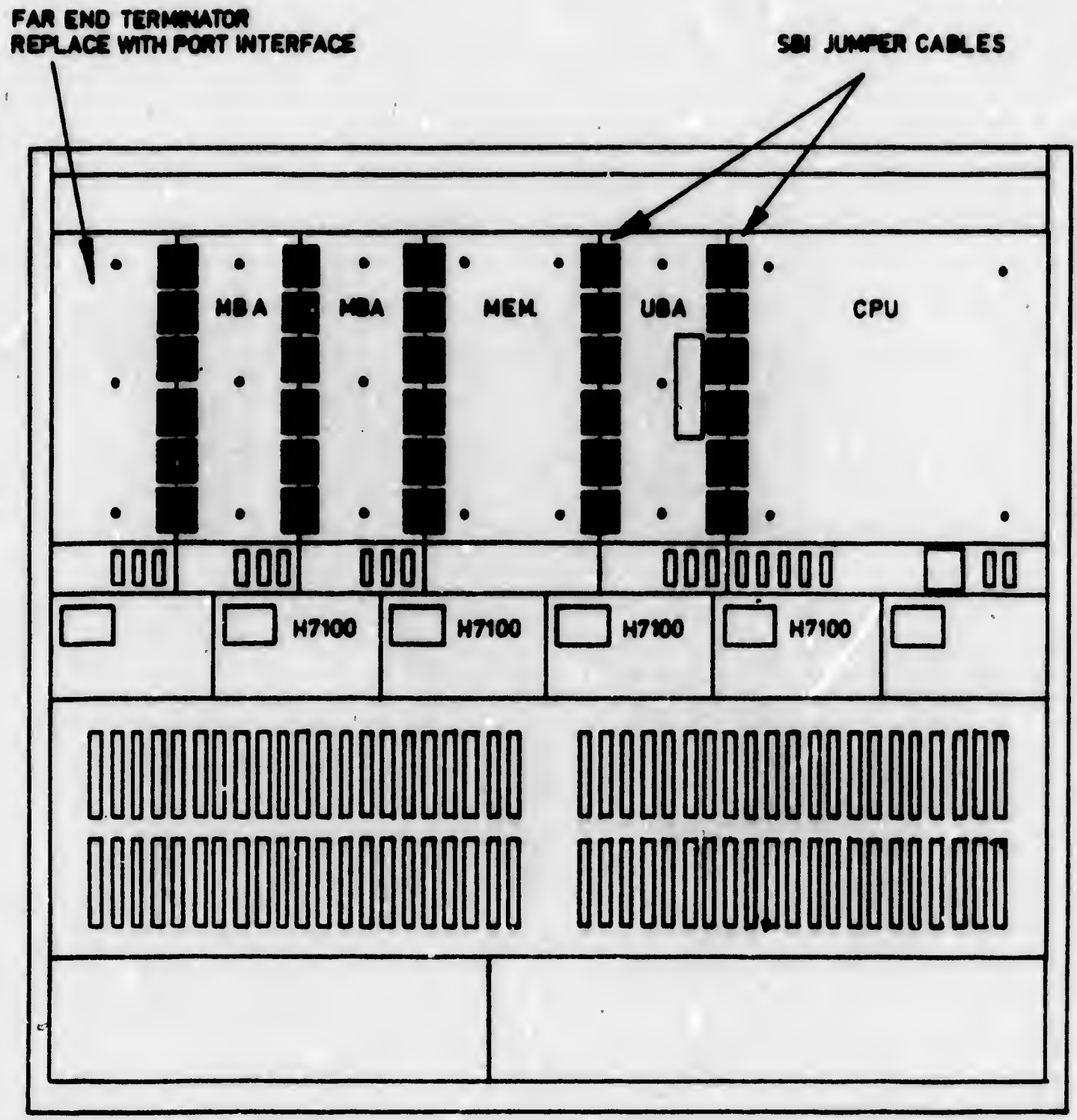
```
        11(D)           NO RESPONSE
        12(D)           NO RESPONSE
        13(D)           DR7##
        14(D)           NO RESPONSE
        15(D)           NO RESPONSE

PROCESSOR  ATTACHED  TO  MPM  #  PORT  1  IS  SLAVED  TO
     PROCESSOR ON PORT #
PROCESSOR  ATTACHED  TO  MPM  #  PORT  1  IS  SLAVED  TO
     PROCESSOR ON PORT #
.. END OF RUN. # ERRORS DETECTED. PASS COUNT: 1


NOTE - # ERRORS ALLOWED.
```

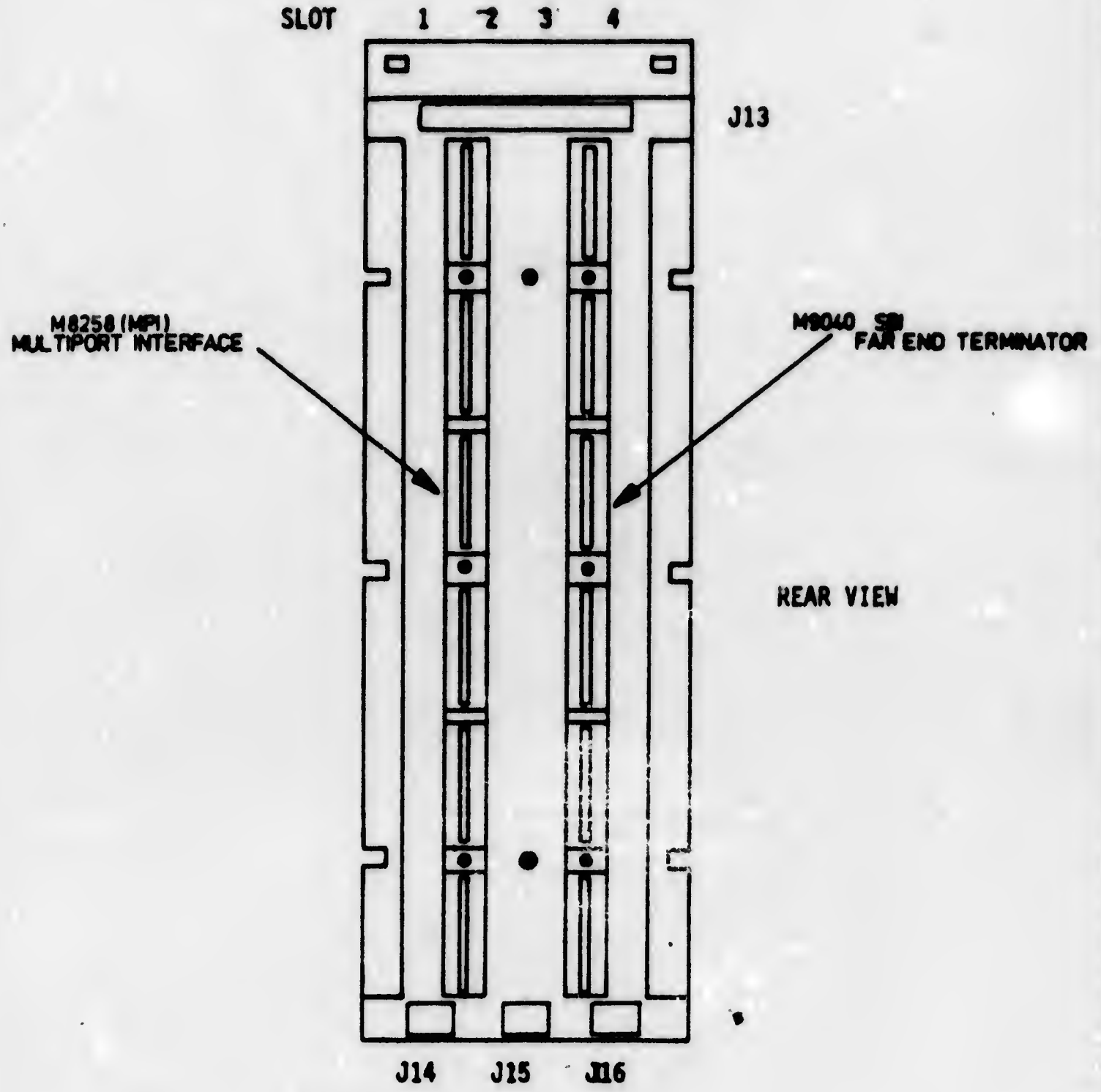
11780 REAR VIEW

FIGURE 1

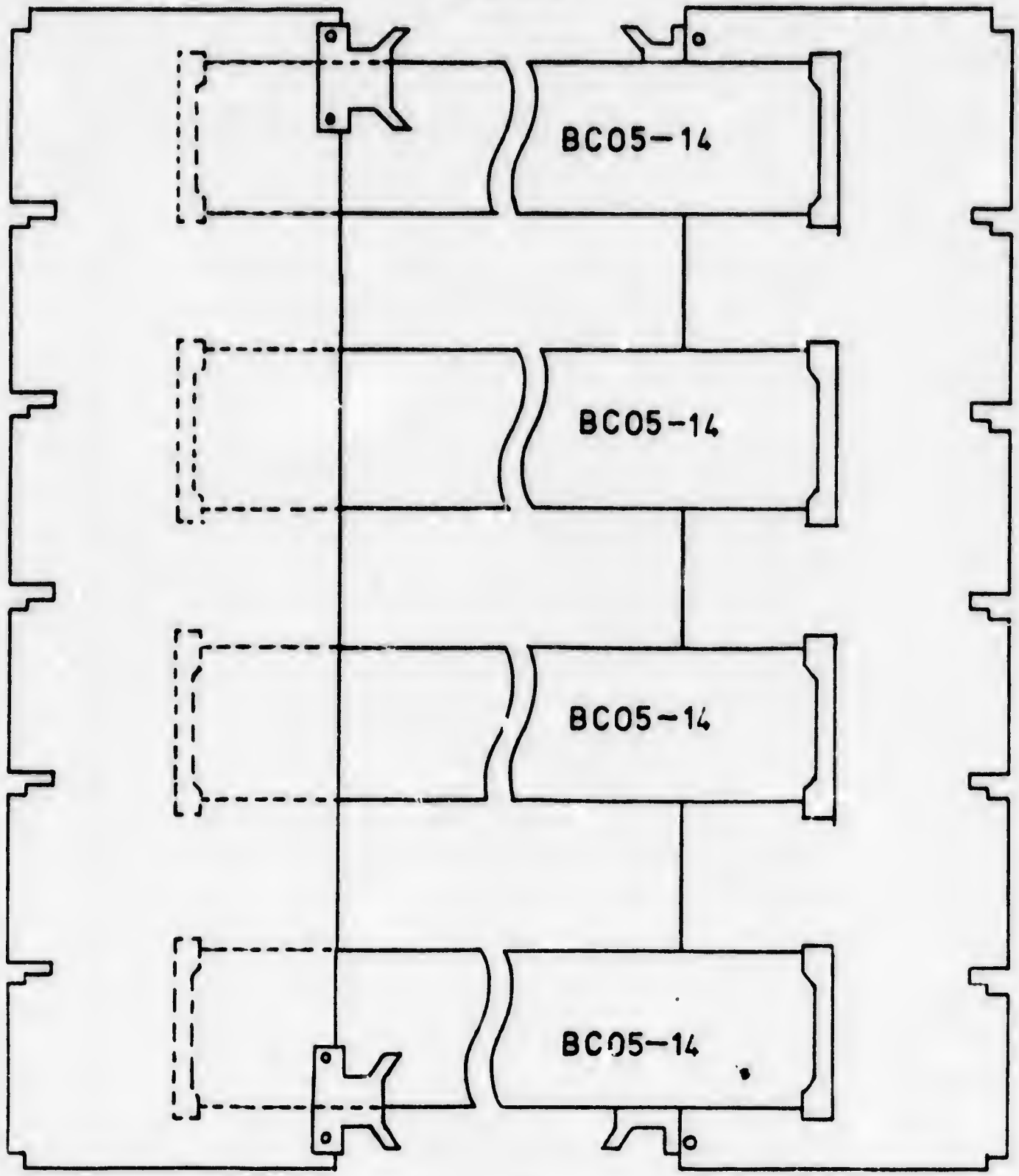


MULTIPORT INTERFACE BACKPLANE

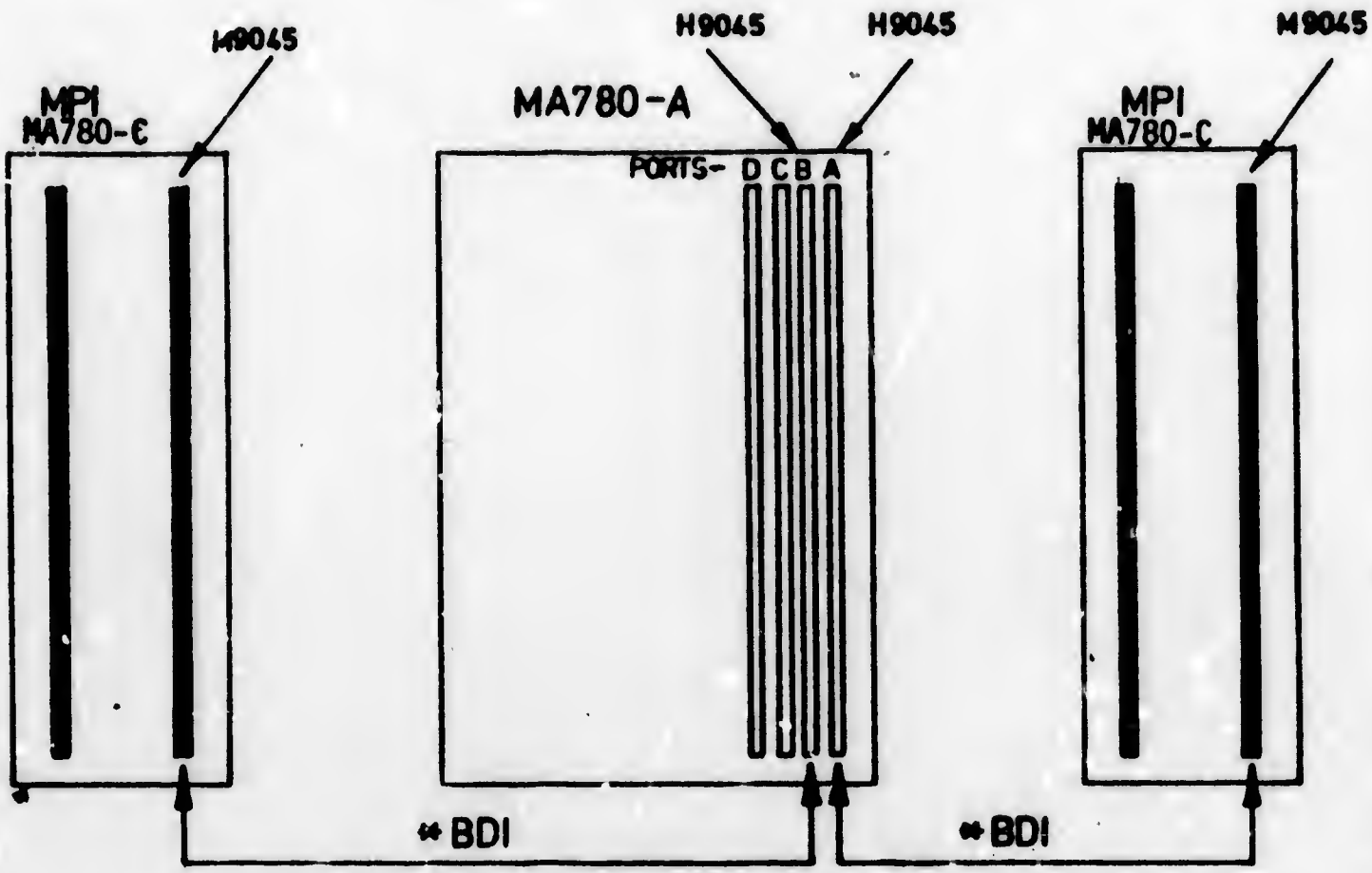
FIGURE 2



CABLE CONNECTIONS
FIGURE 3



MA780 INTERCONNECTIONS
FIGURE 4

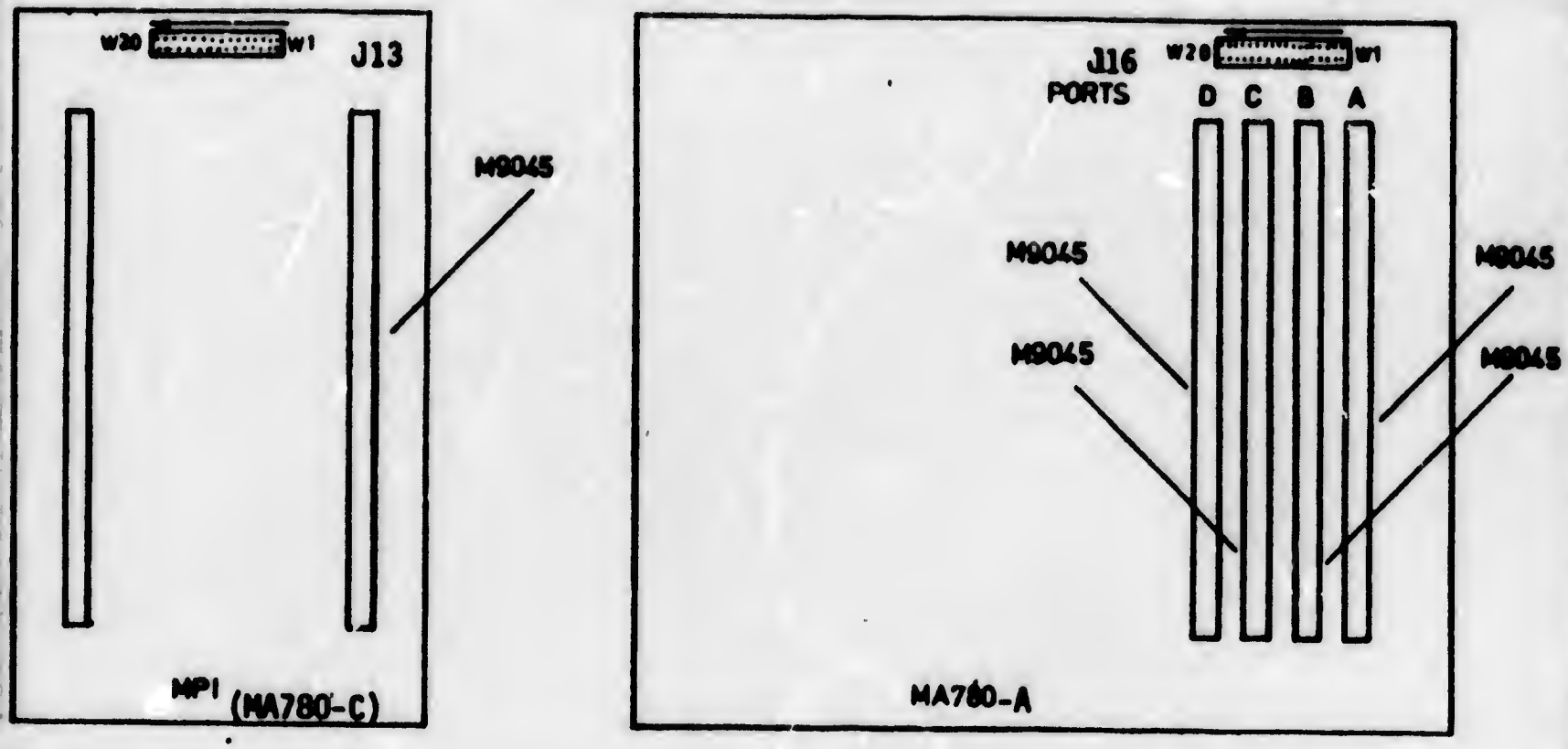


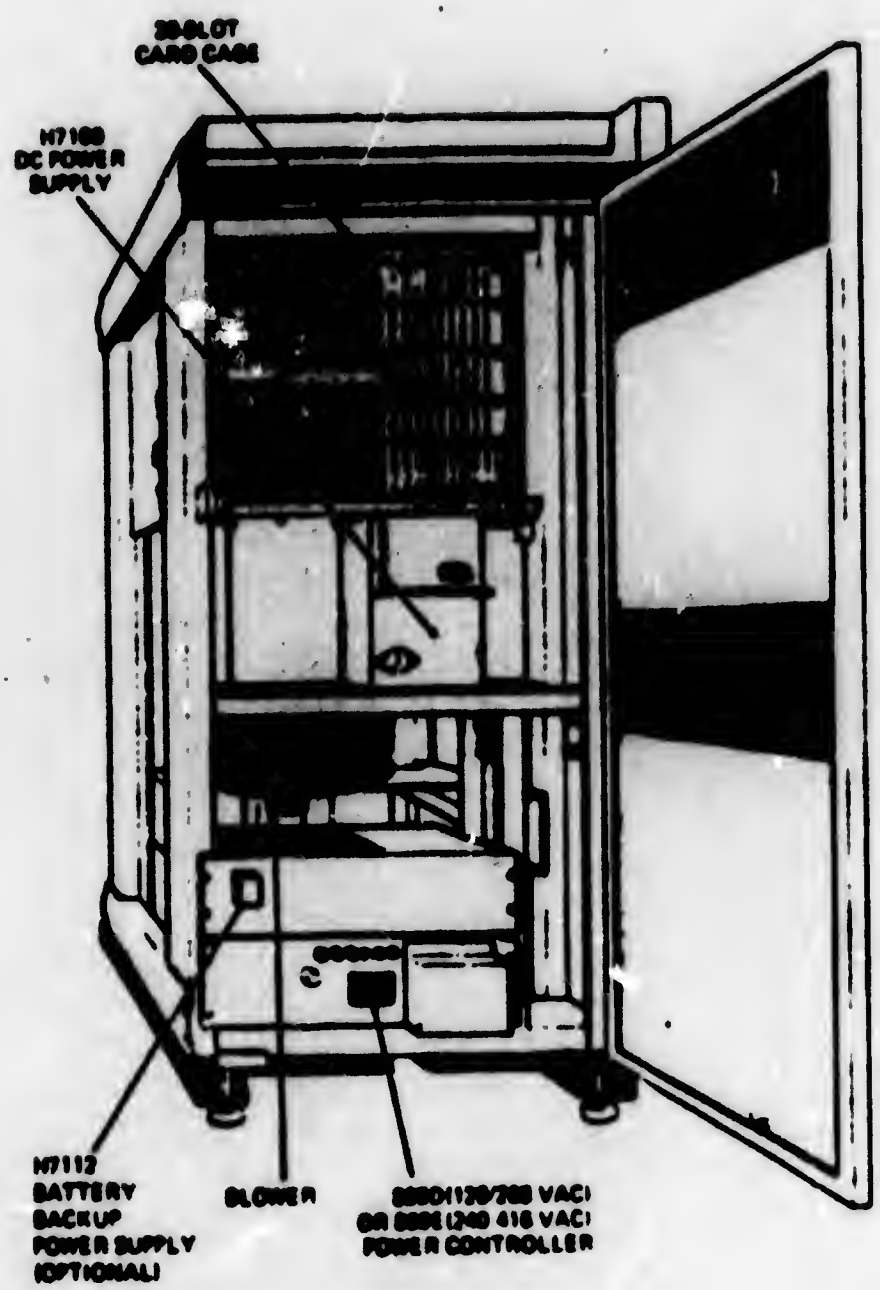
* BDI=BI-DIRECTIONAL INTERCONNECT

JUMPER LOCATIONS

FIGURE 5

REAR VIEW

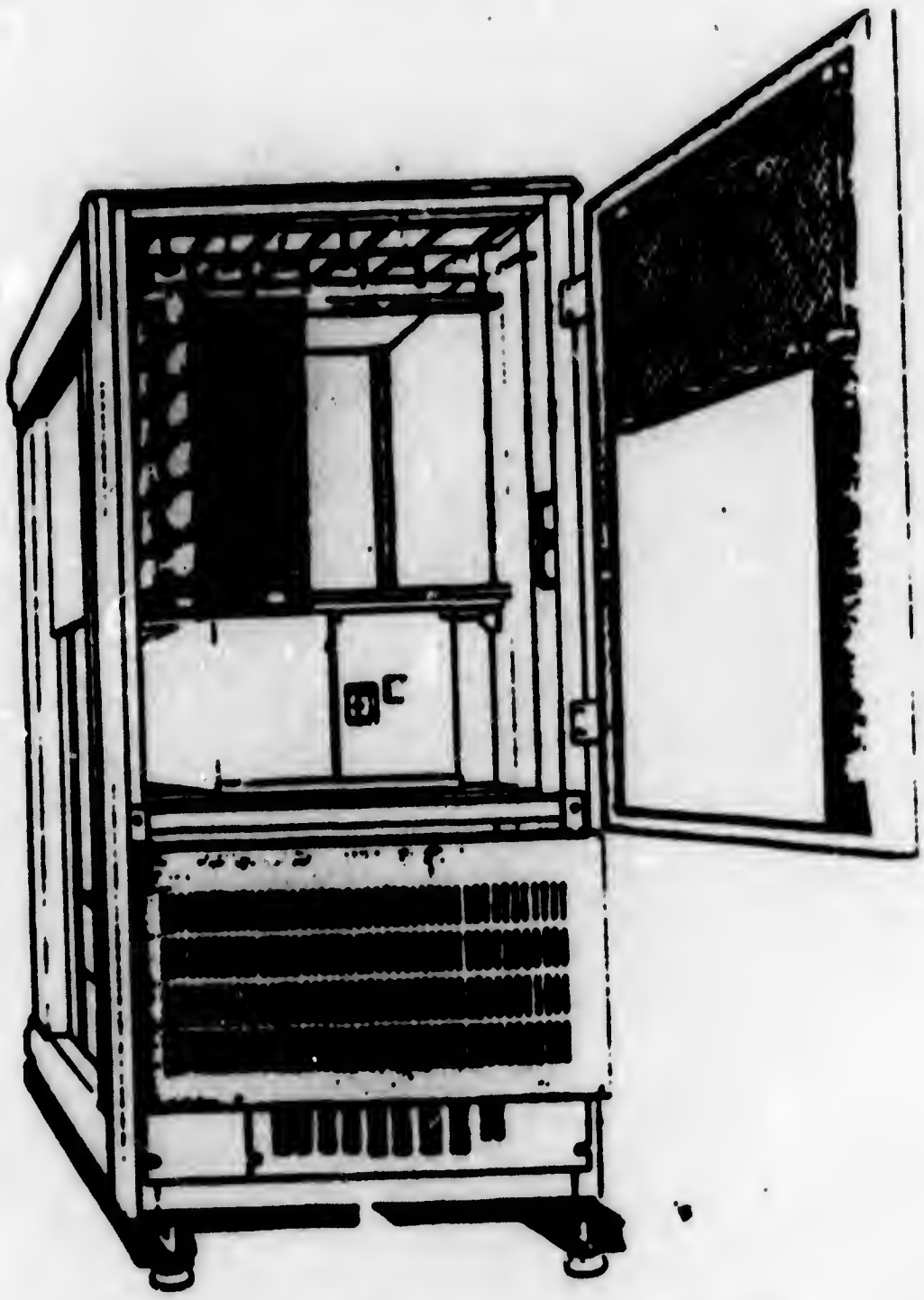




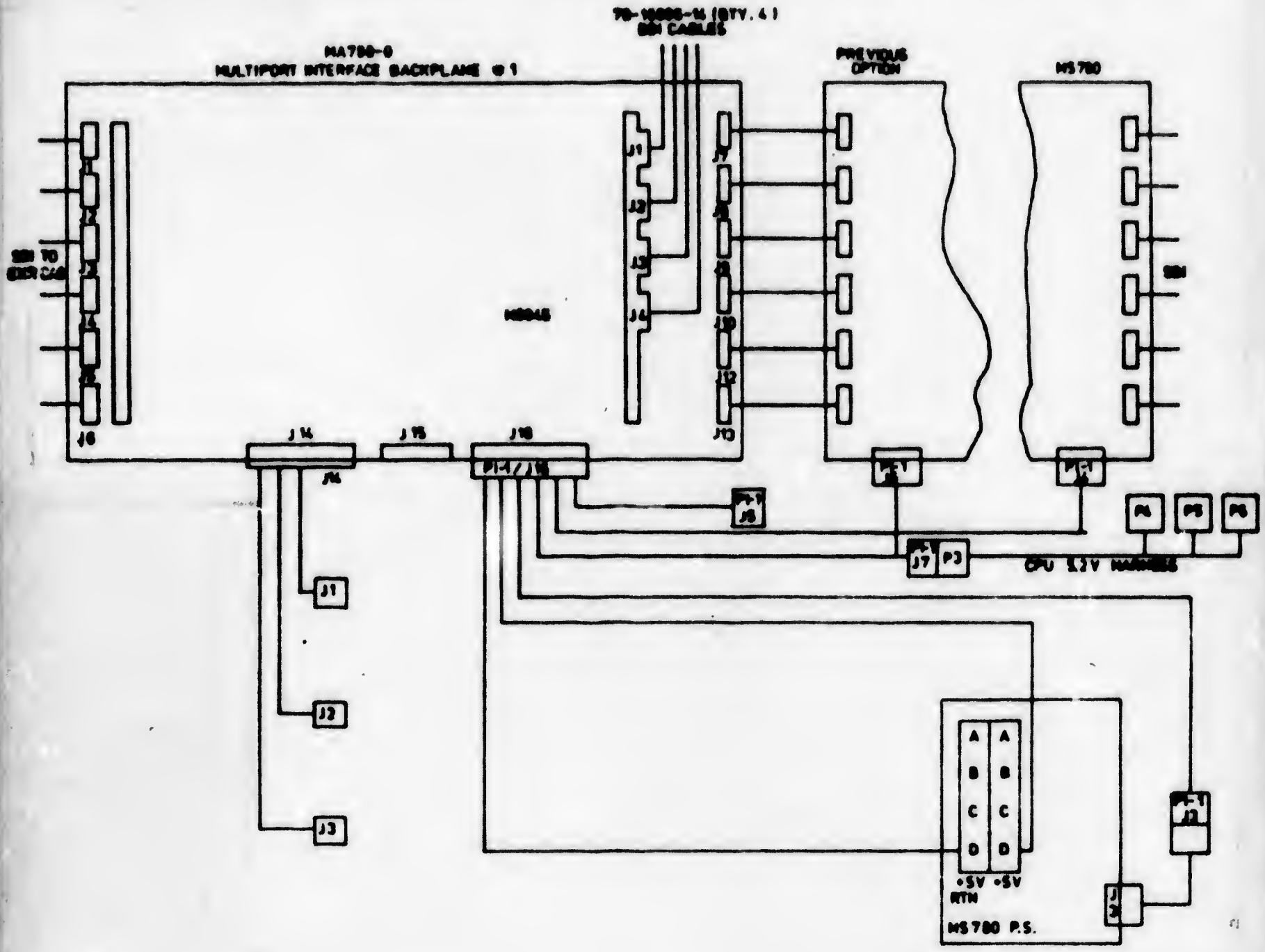
****** FIGURE 6 *******

MA780 MULTIPORT MEMORY (FRONT)

****** FIGURE 7 ******

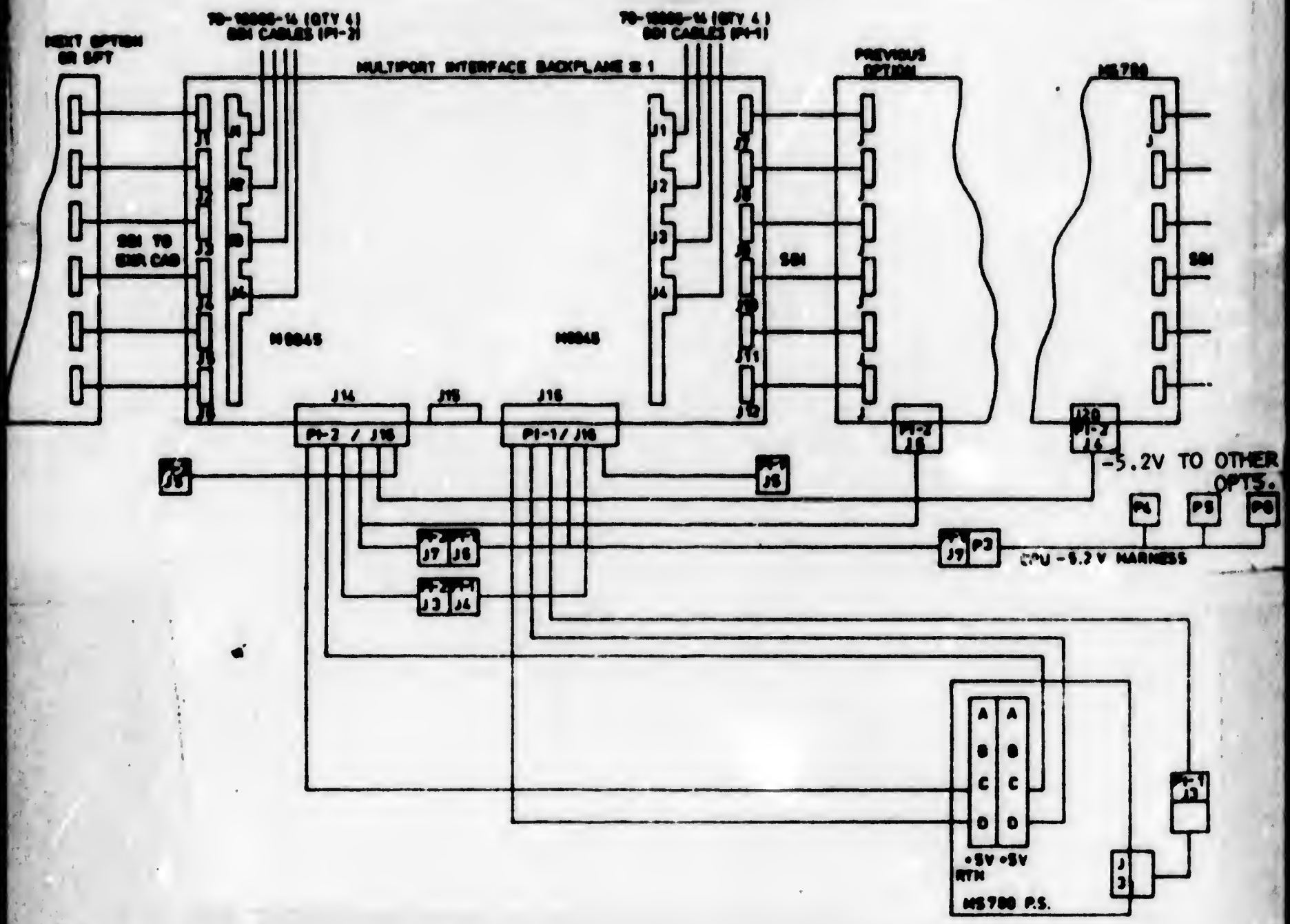


MA780 Multiport Memory Cabinet (Rear View)



***** FIGURE 8 *****

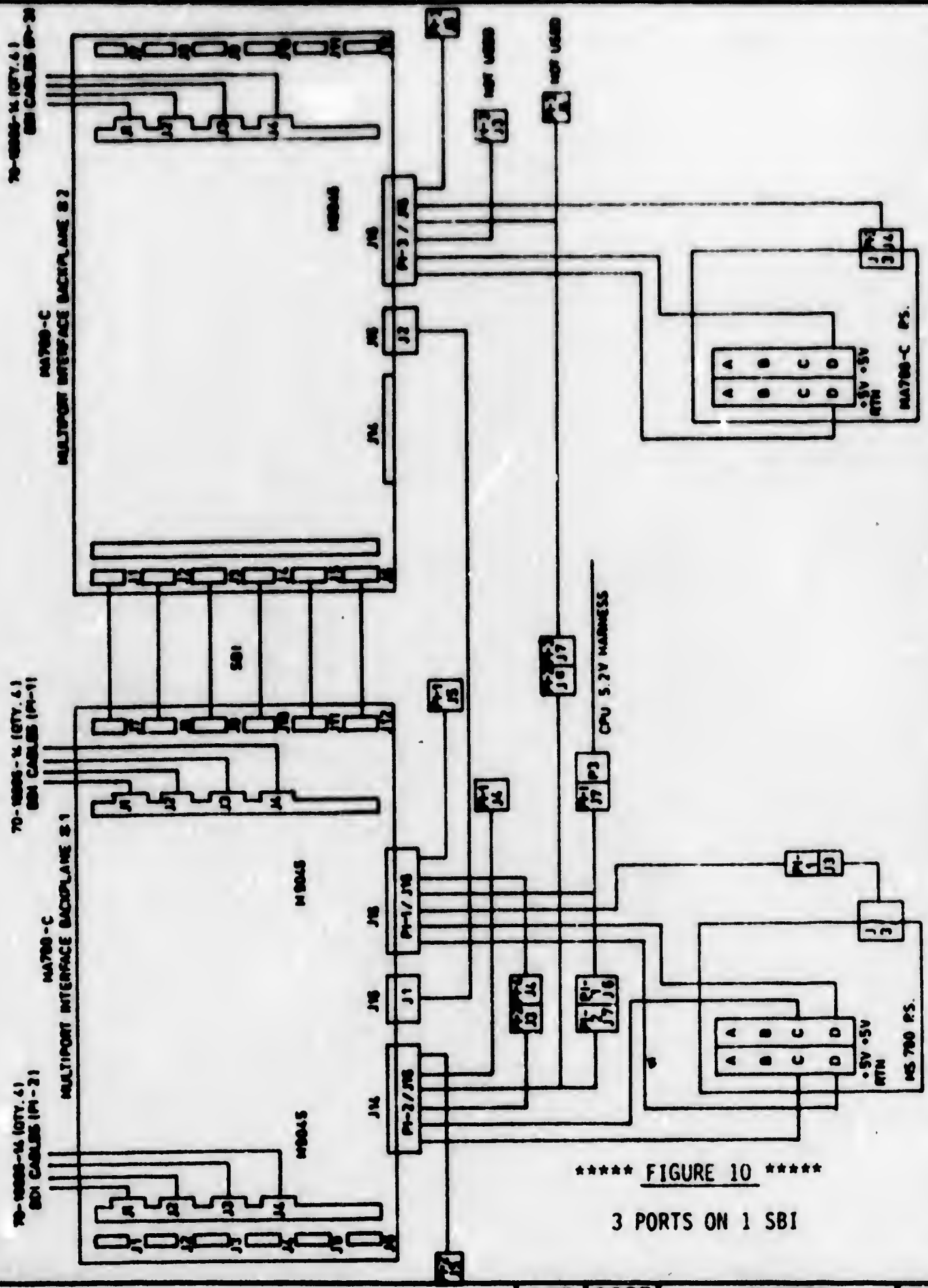
SINGLE PORT INTERFACE

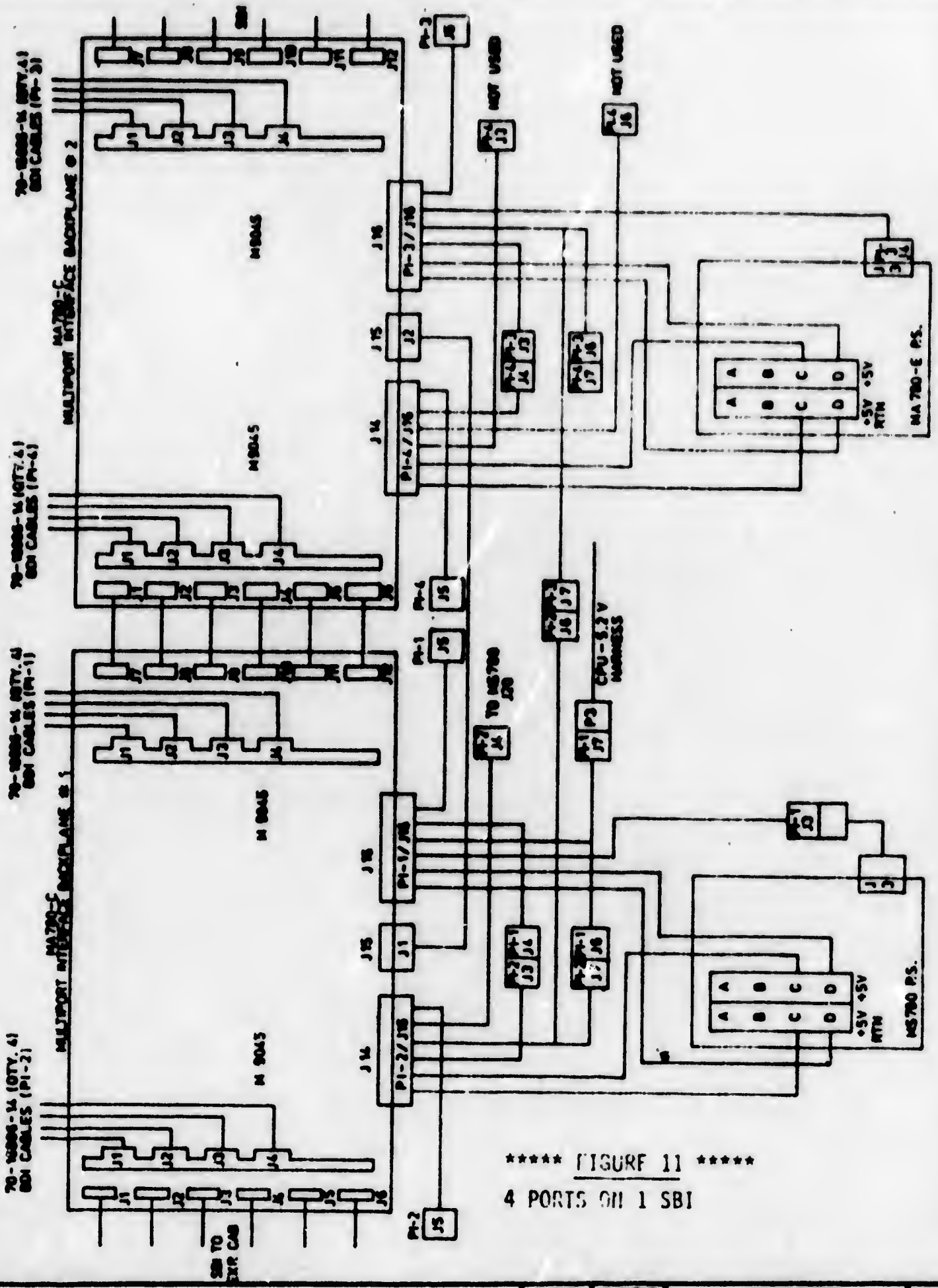


***** FIGURE 9 *****

2 PORTS ON 1 SBI

TITLE MODULAR APPROACH TO SYSTEMS TEST





***** FIGURE 11 *****

4 PORTS ON 1 SBI

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 5/1/81

TITLE MS780 MEMORY

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	VAX 11780 MEMORY CONTROLLER Rewrite	ML013	A.Gauthier	4/11/81	A. B	4/11/81

ENG	APPD	SIZE	CODE	NUMBER	REV
Al Gauthier	Bob Beck	A	SP	MA-V2850-0-0	C

MS780 MEMORY

1.0 INTRODUCTION

The MS780 is comprised of an SBI interface/memory controller and either the M8210 (16K) or M8211 (4K) MOS Array modules.

The MS780 memory controller will buffer one command while it processes another to increase system throughput. Memory controllers can be interleaved to increase the available memory bandwidth. The MS780 also employs error checking and correction (ECC) that corrects all single bit errors and detects all double bit errors.

The MS780 memory array modules are laid out in a 72 bit word, 64 bits data and 8 bits ECC, and come as a 64Kb array (M8211) or a 256Kb array (M8210). This gives an MS780 a max physical memory capacity of 1Mb or 4Mb respectively.

1.1 Memory Option Designations

1.1.1 MS780 - AA (115V) Power Supply, Memory
MS780 - BB (230V) Control, and 128KB
(4K) Memory

1.1.2 MS780 - CA (115V) Power Supply, Memory
MS780 - CB (230V) Control, and 256KB
(16K) Memory

1.1.3 MS780 - BA 128KB (4K) Memory
MS780 - DA 256KB (16K) Memory

1.1.4 H7112-A (115V) Battery Back Up
H7112-B (230V) " " "

2.0 REFERENCE DOCUMENTATION

2.1 Manuals:

2.1.1	Vax Memory System Technical Description	EK-MS780-TD
2.1.2	Diagnostic System Manual	EK-DS780-TD
2.1.3	Power System Overview	EK-PS780-TD
2.1.4	Hardware User Guide	EK-UG780-UG

2.2 Prints

2.2.1	11780 Complete Print Set	M000539
2.2.2	VAX 11780 CPU MAST Back-Up	MAV2100-0 0

2.3 Reference Listings:

2.3.1	Wire list and pin sort	70-13625-0-0
2.3.2	VAX 11780 Architecture Handbook	EB-07466

3.0 REQUIRED TEST EQUIPMENT

3.1 Diagnostic Diskettes:

3.1.1	RX1 Floppy Diskette	AS-E633?-YE
3.1 2	RX3 Floppy Diskette	AS-E159?-DE
3.1.3	RX8 Floppy Diskette	AS-E161?-YE
3.1.4	RX25 Floppy Diskette	AS-F748?-YE

3.2 Hardware

3.2.1 W9025 extender board

3.2.2 Assorted chip clips

3.2.3 Oscilloscope - Tektronix 465 - or equivalent

3.2.4 Voltmeter - Tektrontix DM44 - or equivalent

3.3 Memory Controller

3.3.1 7013625-0-0 Backplane Assembly

3.3.2 M8214 - Memory SBI Board

3.3.3 M8213 - Memory Control Board

3.3.4 M8212 - Memory Data Board

3.3.5 7014103 - Blank Modules

3.4 Memory Array Boards

3.4.1 M8211 - 4K Chip Array

3.4.2 M8210 - 16K chip Array

3.5 Power Supply

3.5.1 70-14957-00 = 115V 60 Hz H7100A with H7102 (+/- 12V Regulator) and H7103 (+/- 5VB Regulator).

OR

(Depending on Configuration)

70-14957-01 = 230V 50 Hz H7100B with H7102 (+/- 12V Regulator). and H7103 (+/- 5VB Regulator)

3.6 Battery Backup (optional)

3.6.1 H7112-A (115V) Battery Charger

or
(Depending on Configuration)

H7112-B (230V) Battery Charger

3.6.2 70-14547-3D Cable for Battery Option

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 MS780 Diagnostics and Monitors

4.1.1 Level 4 - The following diagnostics do not require Diagnostic Supervisor.

ESKAH --- Microdiagnostic Test #1
ESKAJ - - Microdiagnostic Test #2

4.1.2 Level 3 -- These Diagnostics run stand-alone under Diagnostic Supervisor.

NOTE: EVKAA --- This Diagnostic needs to be run only if operator experiences trouble with Diagnostic Supervisor.

EVKAB --- Basic Instruction Exerciser
EVKAC --- Floating Point Instruction Exerciser.
EVKAD --- Compatability Mode Inst.
EVKAE --- Privileged Architecture

5.0 SPECIAL INSTRUCTIONS

5.1 CAUTION: No Metallic Jewelry should be worn while servicing this equipment due to the high current capabilities of the power supplies.

5.2 Jumper conversion used is

I = Jumper In, O = Jumper Out, X = Unimportant

Jumper configurations are explicit, or standard configuration is shown by an arrow (----->).

5.3 WARNING: While inserting or removing modules in the MS780, CONFIRM that THE MEMORY POWER SUPPLY is shut OFF by its CKT Breaker. AC Power to the Memory Power Supply could still be present, or Battery Back-Up Voltages could still be on logic if H7112 is installed.

NOTE: Verify that the Memory Power Supply and the H7112 are plugged into an UNSWITCHED outlet in the 869 Power Controller.

5.4 Before powering up the system a floppy diskette (either RX1 or RX3) which has the console boot program, should be inserted in the RX Drive.

5.5 In section 8.0, the user's response is underlined.

6.0 INSTALLATION SET-UP & TEST INSTRUCTIONS

6.1 Module Utilization Map for MS780

Slot 20	19	18	17		2	1
M8214 MSA	M8213 MCN	M8212 MDT	M8210 (Note #1)	(Note #2)		NOT #3

NOTE#1= Either Module M8210 or M8211 must be inserted in this slot.

NOTE#2= If other M8210's or M8211's, they must be inserted in descending slot openings. Unused slots must contain 7014103 blank Modules.

NOTE#3= Slot #1 is not used for a Memory Array Module. It will have a blank Module or an M9040 Module if there is no S.F.T. on the far end of the S.B.I.

6.2 MS780 Backplane Jumpers and Connections.

6.2.1 Fail Strapping
(Refer to Figure 1, Figure 1A, and to TABLE A below).

TABLE A
Typical Memory Configuration

Memory Controller #	Bus Tr Level	Fail Strap-ping	IRD Strap-ping	SA Strap-ping
1	1	W	0	0
2	2	0	I	4 Mbytes
3	3	0	I	8 Mbytes
4	4	0	I	12 Mbytes

6.2.2 Memory controller with ROM Bootstrap is system critical and will activate fail on power down. Controllers without ROM will use alert.

6.2.3 W = Backplane wire from D20B2 to C20V2 allows the power failing condition

6.2.4 0 = No backplane wire between D20B2 and C20V2. Memory will not activate bus SBI fail L.

6.3 IRD Strapping: (Inhibit ROM Decode)
(Refer to Figure 1 and to table in Section 6.2 of this procedure.

6.3.1 ROM Bootstrap will always be on memory controller #1.

6.3.2 I = Jumper placed across pair of pins. (J21 pin 12). Issues Read Commands to ROM addresses, receive no response, and are not initiated. Refer to Figure 1A.

6.3.3 0 = No Jumper. Issues Read Command to ROM addresses, receives normal confirmation and cycle is initiated.

6.4 TR Level Strapping

Binary Weight	8	4	2	1	BACKPLANE WIRE F20K2 to _____	BUS TR Level
J21 Pin	4	3	2	1		
	0	0	0	0	F20C1	1
	0	0	0	I	F20D1	2
	0	0	I	0	F20E1	3
	0	0	I	I	F20F2	4
	0	I	0	0	F20H2	5
	0	I	0	I	F20J1	6
	0	I	I	0	F20J2	7
	0	I	I	I	F20M1	8
	I	0	0	0	F20N1	9
	I	0	0	I	F20P1	10
	I	0	I	0	F20P2	11
	I	0	I	I	F20S2	12
	0	I	0	0	F20T2	13
	I	I	0	I	F20U1	14
	I	I	I	0	F20U2	15

6.5 Starting Address Strapping. Refer to Figure 1 and to the table below. For this procedure. Starting address strapping is only used by the memory on cold power up so each memory assumes some unique predefined address. The actual operating starting address is loaded into each memory controller. Normal set-up is to have the Memory Controller(s) power up with a starting address of Zero, otherwise Micro #2 will not see the other controller(s). Refer to section 8.2

SA1 J21 Pin #20	SA0 J21 Pin #19	MEMORY CONTROLLER STARTING ADDRESS AFTER COLD POWER UP ONLY
O	O	0 Mega Bytes
O	I	4 Mega Bytes
I	O	8 Mega Bytes
I	I	12 Mega Bytes

6.5.1 Voltage connections and pinning:

Power Supply Voltage Connections:

Volts P.S.	Input Conn. Pin #	Slot 1	Slot 17	Slot 18	Slot 19	Slot 20
-5.2V	J19-1 W5-1 W6-1	EK1	N.C.	N.C.	N.C.	EK1
+5V	J18	AA2,AV1 BA2,BV1 EA2,EV1 FA2,FV1	AA2,AV1 BA2,BV1 EA2,EV1 FA2,FV1	AA2,AV1 BA2,BV1 CA2,CV1 DA2,DV1 EA2,EV1 FA2,FV1	AA2,AV1 BA2,BV1 EA2,EV1 FA2,FV1	AA2,AV1 BA2,BV1 CA2,CV1 DA2,DV1 EA2,EV1 FA2,FV1

NOTE: The Battery voltages listed below are present when the Memory Power Supply is turned on, whether Battery Back-Up is installed or not. These voltages are also present when main AC Power is off and Battery Back-Up is supplying power to Memory, (as in a power fail condition).

Voltage Battery Back-Up	Input Conn. Pin #	Slot 2	Slot 17	Slot 19
+5 Volt Bat.	J14-1,2 J14-3,4	CA2,CV1 DA2,DV1	CA2,CV1 DA2,DV1	CA2,CV1 DA2,DV1
+12 Volt Bat.	J17-2,3	AS1,FD2	AS1,FD2	N.C.
-5.2 V Bat.	J17-1,4 W3-1 W4-1	BL2,EK1	BL2,EK1	N.C.

Ground Connections:

GROUND	J15
	J16-3
	J17-5,6,7
	J17-8,9
	10,11,12
	J19-2
	J20-3

6.5.2 Signal Connections:

Signal	Input Conn. Pin #	Slot 1	Slot 19	Slot 20
MEMORY AC LO	J20-1 W8-1	CR1	N.C.	FE2
MEMORY DC LO	J20-2 W7-1	DE2	FT2	FR2
CLOCKS AC LO	J16-1 W2-1	CR2	N.C.	N.C.
CLOCKS DC LO	J16-2 W1-1	DE1	N.C.	N.C.

6.6 Installation of Memory Controller:

NOTE: Verify that AC Power is OFF before beginning installation.

6.6.1 Installation of a new Memory Controller in the CPU CAB will first involve removal of the existing Memory Controller.

6.6.2 Remove the 4 Mate-N-Lock connectors from the lower edge of the Backplane, along with the (2) +5 Volt, and (2) +5 Volt Return Power Cables.

6.6.3 Remove the SBI Cables on each side of the Backplane. (6) SBI Cables on the right, and (6) SBI Cables on the left.

6.6.4 Remove the (6) screws, (3) on the top rear, and (3) on the front bottom edge of the logic cage.

6.6.5 Remove the Memory Controller from the rear of the CPU Cab,and install the new Controller. Replace all screws and cable connections to their proper locations.

6.7 Installing a Memory Controller in the H9602-H? Cab

6.7.1 Remove the Logic Blanks, (#74-21661-00) from the first and third spaces in the H9602-H? Cab.

6.7.2 The Memory Controller MUST be the first logic in the H9602-H? Cab. Any other Logic occuping the first three spaces must be moved over before installion of the Memory Controller. Only one Memory Controller can be mounted in the H9602-H? Cab.

6.7.3 The Memory Power Supply mounts in Power Supply Slot #1, under the Memory Controller. The AC Power cord for the Memory Power Supply has to be plugged into J14-B of the 869 Power Controller. Backplane Power connections and mounting screws are the same as those used in the installation of the Power Supplies in the main cab.

6.8 Installation and checkout of H7112 Battery Back--Up. (optional)

6.8.1 Mount H7112 above (Time Of Day) power supply using upright holes #18 and #22. (Ref. UA 11780-0-0 Sheet7)

NOTE: For H9602-H? use holes #12 and #16 above 869 Power Controller.

6.8.2 Route AC power cord over 11/03 to 869 outlet J14-B. (Ref IC 11780-0-1 sheet 5 and sheet 6)

NOTE: For H9602-H? route AC Power Cord over rear of 869 to outlet of J17-B.

6.8.3 Route and dress 70-14547-3D (Battery Cable) in left front vertical and center front horizontal to the memory Power Supply J2.

6.8.4 Plug over-temp cable (part # 70-14213-3E) into J11 on back of H7112.

NOTE: The middle pin of the over-temp cable should have about 25 volts Reference to ground when the 869 Power Controller is switched on.

6.8.5 Power up system. Check LED inside H7112 to be ON; indicating that the batteries are charging.

NOTE: For fully charged batteries, the LED should stay on for at least 10 seconds on power up. Normal ON TIME is from a few minutes to a few hours depending on the initial charge state of the batteries.

6.8.6 With Batteries fully charged, load a program into memory.

NOTE #1: If the system has more than 1 memory controller and battery back-up, interleave the memory controllers before loading a program. Refer to section 8.2 After loading a program, halt the system and turn off power by using the key switch first then shut off the breaker on the 869 Power Controller(s) for one minute.

NOTE #2: The Power inverter failure LED on the front of the Memory Power Supply, should come on in approximately 10 to 15 seconds after the main Breaker on the 869 Power Controller is switched OFF.

Turn the 869 main Breaker(s) back ON. Turn on system using the key switch. Restart your program. The program should have been preserved.

6.9 Battery Back-UP Cable Pinning (70-14547-3D) Voltages with cable plugged into P2 of Memory Power Supply.

VOLTAGE/ SIGNAL	COLOR	P2 PIN/S	REALISTIC READINGS PWR.-GND	
			AC PWR ON	AC POWER FAIL COND.
+36 V BAT.	RED	1,2	+30 VOLTS	+36 VOLTS
+36 V RET.	BLACK	7,8	GND	GND
AC LOW -8V,-11V	YELLOW	4	-9 VOLTS	0 VOLTS
RELAY CLOSER +57Volts	GRAY	3,6	+55 VOLTS APPROX.	+36 VOLTS APPROX.

6.10 Detailed test procedure:

6.10.1 Perform visual inspection for obvious discrepancies, damages, or potential power-up problems.

6.10.2 Check to see that modules are in the correct slots. Refer to sec 6.1 of this procedure.

6.10.3 Verify proper hardware set up. Refer to sec 6 for configuration jumper tables.

6.10.4 Take resistance readings of the power supply outputs, to verify that there are no power to ground shorts.

NOTE: Readings will vary depending on the number of Array Modules installed.

6.10.5 Turn on memory power supply breaker and observe indicators for normal power indications.

7.0 POWER CHECKS

7.1 Check Memory Voltages:

VOLTAGE/ SIGNALS	COLOR	PIN		VALUE
+5 volt	Red	J18		+4.9 to +5.2 Volts
-5 volt	Blue	J19	Pin 1	-5.0 to -5.3 Volts
+12 volt	Orange	J17	Pins 2,3	+11.66 to +12.24 volts
+5 Batt.	Red	J14	Pins 1,2, Pins 3,4	+4.75 to +5.25 volts " " " "
AC Low	Yellow	J20	Pin 1	-8 to-11 volts
DC Low	Violet	J20	Pin 2	-8 to-11 volts
-5 Batt.	Blue	J17	Pins 1,4	-4.75 to -5.25 volts

NOTE: Power Supply is not adjustable and must be replaced if out of range.

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimun test criteria, e.g.: pass counts, etc., refer to the appropriate MAST CHECKLIST.

8.1.1 Insert RX3 Diskette in RX drive, and boot system.

```
>>>
      T<CR>
ZZ-ESKAB   V12.0
3E,
CPU TR= 00000010
```

```
MS780 16K CHIP AT TR 01
MAX ADR+1= 00100000
DW780 AT TR 03
RH780 AT TR 08
RH780 AT TR 09
3F,40,41,42,43,44,45,46,47,48,49,4A,4B,4C,

4D,4E,

MS780 16K CHIP AT TR 01
  ARRAY #: 00000000
  # SINGLE BIT ERRORS:    00000000
  ARRAY #: 00000001
  # SINGLE BIT ERRORS:    00000000
  ARRAY #: 00000002
  # SINGLE BIT ERRORS:    00000000
  ARRAY #: 00000003
  # SINGLE BIT ERRORS:    00000000
4F,
MS780 16K CHIP AT TR 01
M8213 ROMS OK
50,51,52,
NO FPA

END PASS 0001

        CPU HALTED,SOMM CLEAR,STEP=NONE,
        CLOCK=NORM
        RAD=HEX,ADD=PHYS,DAT=LONG,FILL=00,
        REL=00000000
        INIT SEQ DONE
        HALTED AT 00000000

        (RELOADING WCS)
        LOAD DONE, 00003200 BYTES LOADED
        VER: PCS=01 WCS=0D-12 FPLA=0D CON=
        V05-01-L
```

8.2 Interleaving Memory Controllers.
(This is for systems having more than one memory MS780).

8.2.1 Interleaved memory controllers must be contiguous with the bus TR levels.

8.2.2 Have t..e same starting address.

8.2.3 Have same array size.

8.2.4 Be at least two way interleaving.
Example: With 4 controllers,
Controller 1 & 2 interleaved and
3 & 4 interleaved.

8.2.5 When interleaving memory you must first deposit the following into the Memory Controller Configuration registers:

Controller #1

```
>>>
   D 20002000  101<CR>        (2 way Interleaved)

>>>
   D 20002004  4000<CR>       (starting Add.=0)
```

Controller #2

```
>>>
   D 20004000  101<CR>        (2 way Interleaved)

>>>
   D 20004004  4000<CR>       (starting Add.=0)
```

NOTE: Anytime Micro #2 is run the Memory Controllers have to be Interleaved again before running other Diagnostics or software.

8.2.6 Remove RX3 Diskette and mount VAX Instruction Diagnostic #1 RX8.

```
>>>
   BOOT<CR>
```

```
                CPU HALTED
                INIT SEQ DONE
                LOAD DONE, 00014200 BYTES LOADED
DIAGNOSTIC SUPERVISOR, ZZ-ESSAA-6.1-370 6-AUG-
1980 07:23:00
DS>ATT KA780 SBI KA0 NO NO 0 0<CR>
DS>SEL ALL<CR>
DS>SET HALT<CR>
DS>RUN EVKAB<CR>

..PROGRAM: VAX Basic Instructions Exerciser,
ZZ-EVKAB, REV 2.2 10 TESTS, AT 08:21:37.53
TESTING: _KA0

.. END OF RUN. 0 ERRORS DETECTED. PASS COUNT: 1,
TIME: 6-AUG-1980 08:22:36.64
```

8.2.7 Remove RX8 Diskette and mount VAX INSTRUCTIONS DIAGNOSTIC #2 RX25 in the drive.

```
DS>RUN EVKAC<CR>

.. PROGRAM: VAX Floating Point Instructions
Exerciser, ZZ -EVKAC, REV 2.0, 3 TESTS, AT
08:23:37.99.
TESTING: _KA0

..END OF RUN, 0 ERRORS DETECTED.  PASS COUNT: 1,
TIME: 6-AUG-1980 08:24:45.92
DS>RUN EVKAD<CR>

.. PROGRAM: VAX Compatibility Mode Instructions
Exerciser, EVKAD, REV 1.2, 4 TESTS, AT
08:25:26.42
TESTING: _KA0

..END OF RUN, 0 ERRORS DETECTED.  PASS COUNT: 1,
TIME: 6-AUG-1980 08:25:37.42
DS>RUN EVKAE<CR>

.. PROGRAM: VAX Privileged Architecture
```

```
Exerciser, EVKAE, REV 1.2, 9 TESTS, AT
08:26:22.54
TESTING: _KA0

..END OF RUN, 0 ERRORS DETECTED. PASS COUNT: 1,
TIME: 5-AUG-1980 11:34:555.62
DS>
```

[END OF TEST]

TITLE

MODULAR APPROACH TO SYSTEMS TEST

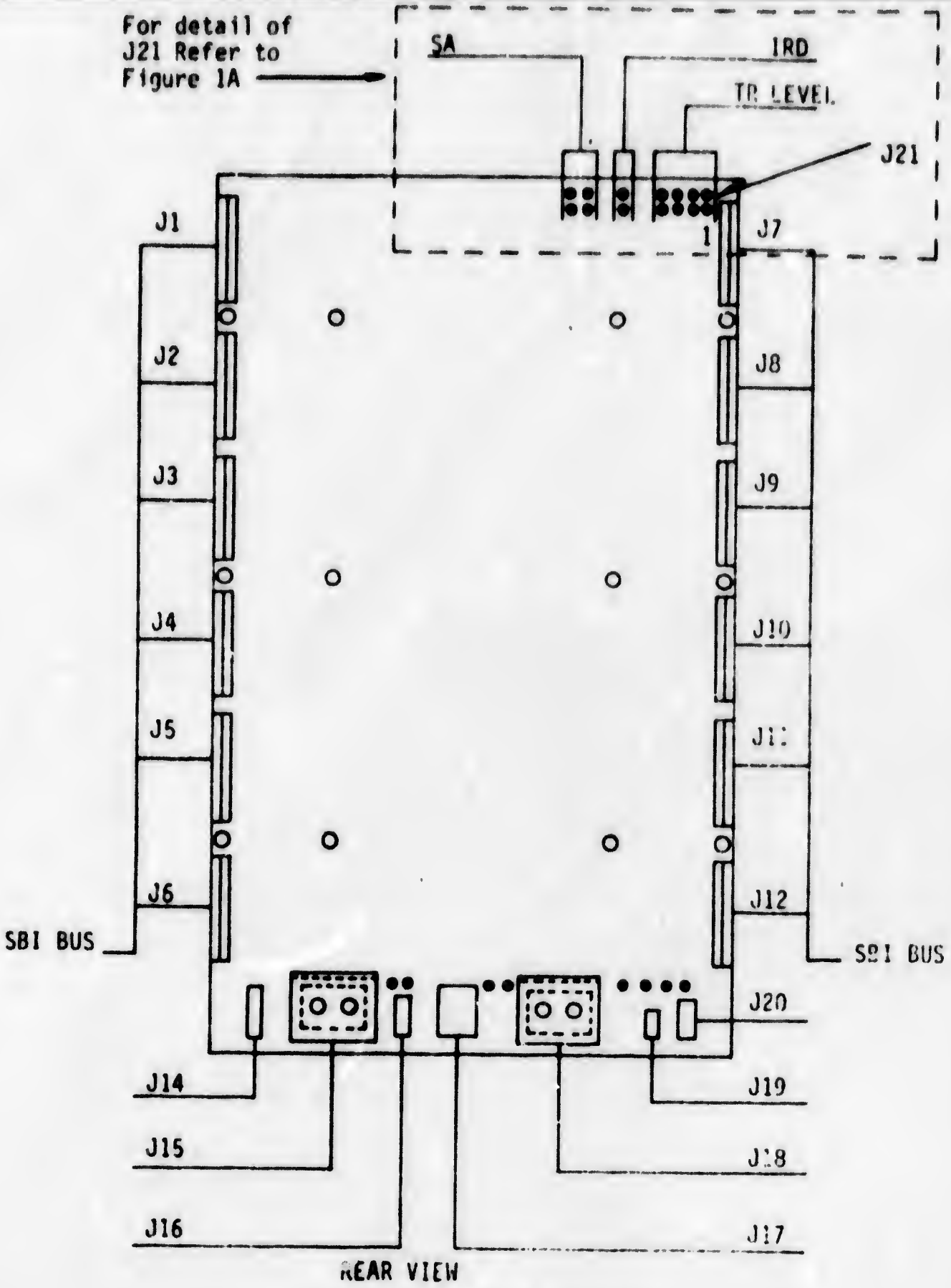


FIGURE 1 MS780 BACKPANEL

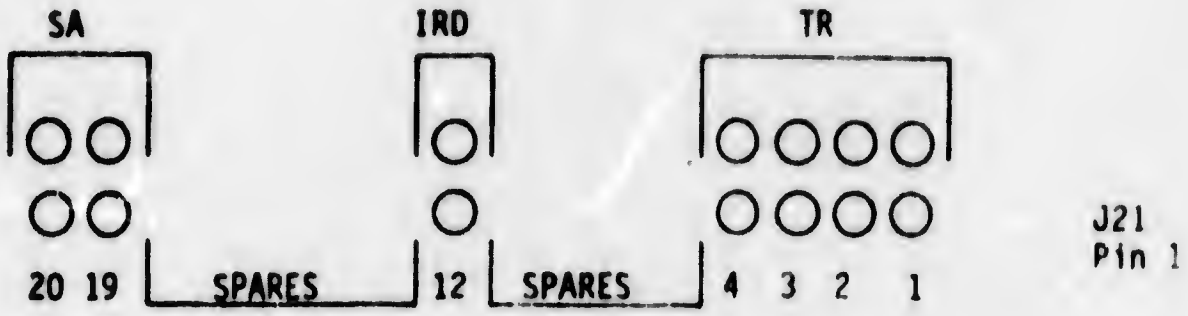


FIGURE 1A Locating the pinning on the J21 section of the MS780 BACKPANEL.


V2.9.10

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. **DATE** 6/5/81

TITLE RH780 MASSBUS ADAPTOR

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
B	Re-write Back-Up of VAX RH780	ML013	Al Gauthier	4/25/81		

ENG	APPD	SIZE	CODE	NUMBER	REV
Al Gauthier	Bob Beck	A	SP	MM-V2910-0-0	B

RH780- MASSBUS ADAPTOR

1.0 INTRODUCTION

The RH780 MASSBUS ADAPTOR (MBA) is the interface between the Massbus and the SBI (SYNCHRONOUS BACKPLANE INTERCONNECT). It performs all control, arbitration, address mapping, and buffering functions. Up to four MBA's may be placed on the VAX 11/780.

The MBA uses a 32-byte silo for data buffering. Data transfers on the SBI are quad-word (64-bit), therefore making efficient use of the SBI bandwidth. On memory to MBA data transfers, the MBA anticipates upcoming Massbus data transfers by pre-fetching the next quad-word of data from memory.

2.0 REFERENCE DOCUMENTS

2.1 Manuals:

2.1.1	VAX-11 RH780 Massbus Adaptor Technical Description	EK-RH780-TD
2.1.2	Power System Overview	EK-PS780-TD
2.1.3	Diagnostic System Manual	EK-DS780-TD

2.2 Prints:

2.2.1	VAX 11780 CPU MAST Back-UP	MAV2100-0-0

2.3 Reference Listings:

2.3.1	Wire lists and pin sort	70-13627-0-0
2.3.2	VAX 11780 Architecture Handbook	EB-07466

3.0 REQUIRED TEST EQUIPMENT

3.1 Test Equipment:

3.1.1 Voltmeter-Tektronix DM44 or equivalent

3.2 Massbus Adaptor Hardware:

3.2.1 7013627-0-0 Backplane Assembly

3.2.2 7013712-0-0 Card Cage

3.3 Modules:

3.3.1 M8275 - MSI ..... (MBA/SBI INTERFACE)

3.3.2 M8276 - MIP ..... (MBA/INTERNAL REGISTER)

3.3.3 M8277 - MDP ..... (MASBUS DATA PATH)

3.3.4 M8278 - MCP ..... (MASSBUS CONTROL PATH)

3.3.5 M9041 - Massbus Paddle Card

3.3.6 (2) 7014103 - Blank Modules

3.4 Cables:

3.4.1 (3) BC06R-10 Cables, to rear I/O panel or depending on Configuration, to side Expander I/O panel.

3.4.2 (6) S.B.I. Cables Part# 1700087-00

3.4.3 (1) Overtemp Cable Part# 70-14213-0K

3.4.4 (1) AC/DC Low Cable * Part# 70-14212-0M

* NOTE: The AC/DC Low Cable is connected between J3 on the H7100 Power Supply and J13 on the RH780 Backplane. When a second RH780 is connected to the same H7100 Power Supply, the AC/DC Low Cable is connected between J14 on the first RH780 Backplane, and J13 on the second RH780 Backplane.

3.5 MBA Option Designations:

3.5.1 RH780-00 Massbus Adaptor only

3.5.2 RH780-AA (115V) Adaptor + Power Supply
or
RH780-AB (230V) Adaptor + Power Supply

3.6 Diagnostic Diskettes:

3.6.1 RX1 Floppy Diskette AS-E633?-YE

3.6.2 RX2 Floppy Diskette AS-E158?-DE

3.6.3 RX3 Floppy Diskette AS-E159?-DE

3.6.4 RX7 Floppy Diskette AS-E160?-YE

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 LEVEL 4 -- The following Diagnostics do not require Diagnostic Supervisor.

ESSAA ---- Supervisor Diagnostic

ESKAH ---- Microdiagnostic Test #1
ESKAJ ---- Microdiagnostic Test #2

4.2 LEVEL 3 -- These Diagnostics run standalone under Diagnostic Supervisor.

ESCAA ---- Vax Channel Diagnostic

NOTE: ESCAA is the only Diagnostic that checks for MASSBUS FAIL. A Massbus or Terminator must be connected to the RH780 while running this Diagnostic. For complete functional testing of the RH780, the dagnostic for the Massbus Device connected to the RH780 under test should be run.

5.0 SPECIAL INSTRUCTIONS

5.1 CAUTION: No metallic jewelry should be worn while servicing this equipment due to the high current capabilities of the power supplies.

5.2 Jumper convention used is:

I = Jumper In, O = Jumper Out, X = Unimportant

Jumper Configurations are explicit, or standard configuration is shown by an arrow, (----->).

6.0 INSTALLATION & TEST SET-UP INSTRUCTION

6.1 Module Utilization Map for RH780

UTILIZATION MAP

6	5	4	3	2	1
BLANK	BLANK	M8272-7K	M8272-7K	M8272-7K	M8272-7K
MODULE	MODULE	MCP8	MDP7	MIR6	MSI5

6.2 MBA Interrupt Level Selection.

For location of (W) jumpers, refer to TABLE 1 and Figure 1.

TABLE 1
Interrupt Selection

ISR #	W5	W6
4	-	-
5 *	-	I
6	I	-
7	I	I

* = ALL

6.3 TR Arbitration level Selection. For location of (W) jumpers, refer to Figure 1 and TABLE 2.

TABLE 2
Arbitration Selection

BUS TR#	SEL D	SEL C	SEL B	SEL A	WIRE WRAP TABLE All Wraps From F02F1 To -----
	W1	W2	W3	W4	
0	I	I	I	I	F02B1
1	O	O	O	O	F02C1
2	O	O	O	I	F02D1
3	O	O	I	O	F02E1
4	O	O	I	I	F02F2
5	O	I	O	O	F02H2
6	O	I	O	I	F02J1
7	O	I	I	O	F02J2
8*	O	I	I	I	F02M1
9**	I	O	O	O	F02N1
10	I	O	O	I	F02P1
11	I	O	I	O	F02P2
12	I	O	I	I	F02S2
13	I	I	O	O	F02T2
14	I	I	O	I	F02U1
15	I	I	I	O	F02U2

* = Normal RH0
** = Normal RH1

6.4 Mate-N-Lock Connections. Refer to TABLE 3.

TABLE 3
M-N-L Connection

	SIGNAL NAME			
CONNECTOR	PS. AC. LO. L	PS. DC. LO. L	-5V	GND
J15	N/C	N/C	1	2
J14	1	2	N/C	3
J13	1	2	N/C	3

6.5 Installing the RH780:

6.5.1 Normal Configuration for RH780 Backplanes in the CPU Cab is to have TR 9 mounted next to the Memory Backplane and TR 8 next to TR 9. This will allow for proper cabling to the I/O panels, (TR 9 to the side exp. I/O panel and TR 8 to the rear I/O Panel).

6.5.2 Whenever an S.B.I. Device is cabled to the side I/O Panel in the CPU Cab or the H9602-H? Cab, that Device is mounted FIRST. Rear I/O Panel Devices are mounted next.

NOTE 1: If both RH780's are cabled to rear I/O Panel, TR 8 goes to J3 and TR 9 goes to J4. Refer to Figure 2.

NOTE 2: If using only the rear I/O Panel for the H9602-H? cab, J3 is to be cabled to the lowest RH780 TR Level in that cab. J4 is then cabled to the next higher TR Level etc. Refer to Figure 3.

6.5.3 The Massbus Cable Transition Block comes installed in J3 of the rear I/O Panel for the CPU and the H9602-H? cab. If J4, J5, J6, are to be used, another Transition Block must be installed in each J number used.

6.5.4 After Cables from the M9041 to the rear and/or side I/O Panels are installed, any excess cable is folded flat and tie-wrapped into the center rear horizontal channel.

6.5.5 The H7100 Power Supply is mounted in Power Supply Slot #5 for CPU installation.

6.5.6 For the H9602-H? Cab, the H7100 Power Supply could be in slot #1 or slot #2, depending on System Configuration.

NOTE: If slot #1 is used, the AC Power cord plugs into the 869 Power Controller J15-B. For slot #2, the AC Power cord plugs into J18-B.

6.5.7 For CPU Power Supply slot #5 and H9602-H?, slot #2, remove the power supply blank, Part # 70-14101-00.

NOTE: 2 RH780 MASSBUS adaptors can be connected to one H7100 Power Supply.

6.6 Cabling to side Expander I/O Panel. Refer to TABLE 4.

TABLE 4
Side Cabling I/O Panel

CABLE	FROM	TO
1. BC06R-10	M9041-C	Exp. I/O Conn J4
2. BC06R-10	M9041-B	Exp. I/O Conn J5
3. BC06R-10	M9041-A	Exp. I/O Conn J6

NOTE: Cables at M9041 are ribbed side up, with stripe to backplane.

6.7 Cabling to rear I/O Panel. Refer to TABLE 5.

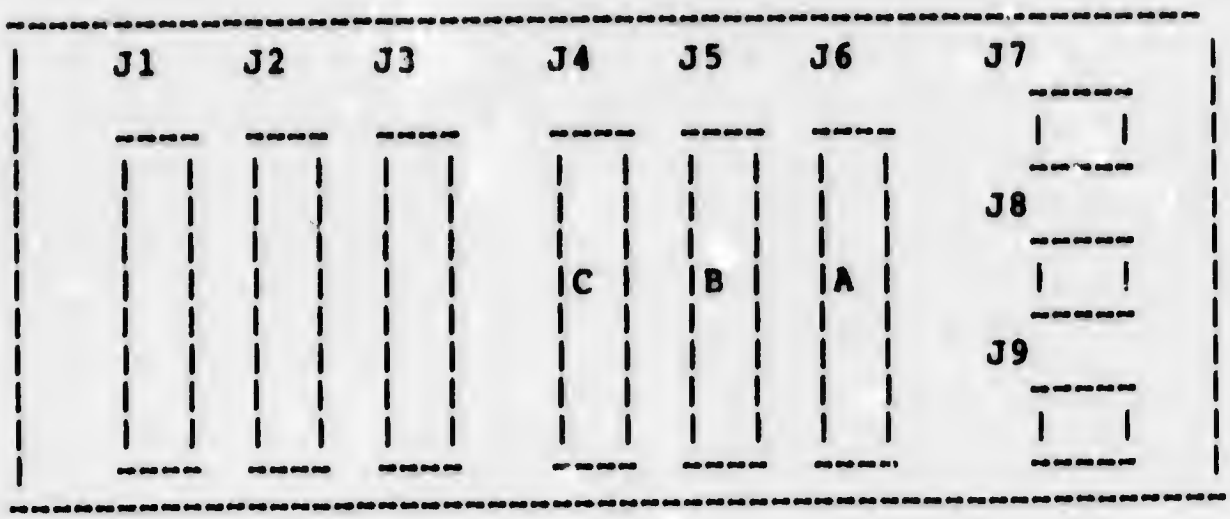
TABLE 5
Rear Cabling to I/O Panel

CABLE	FROM	TO
1. BC06R-10	M9041-C	I/O Conn. J3 Slot C
2. BC06R-10	M9041-B	I/O Conn. J3 Slot B
3. BC06R-10	M9041-A	I/O Conn. J3 Slot A

NOTE: Cables at M9041 are ribbed side up, with stripe to backplane.

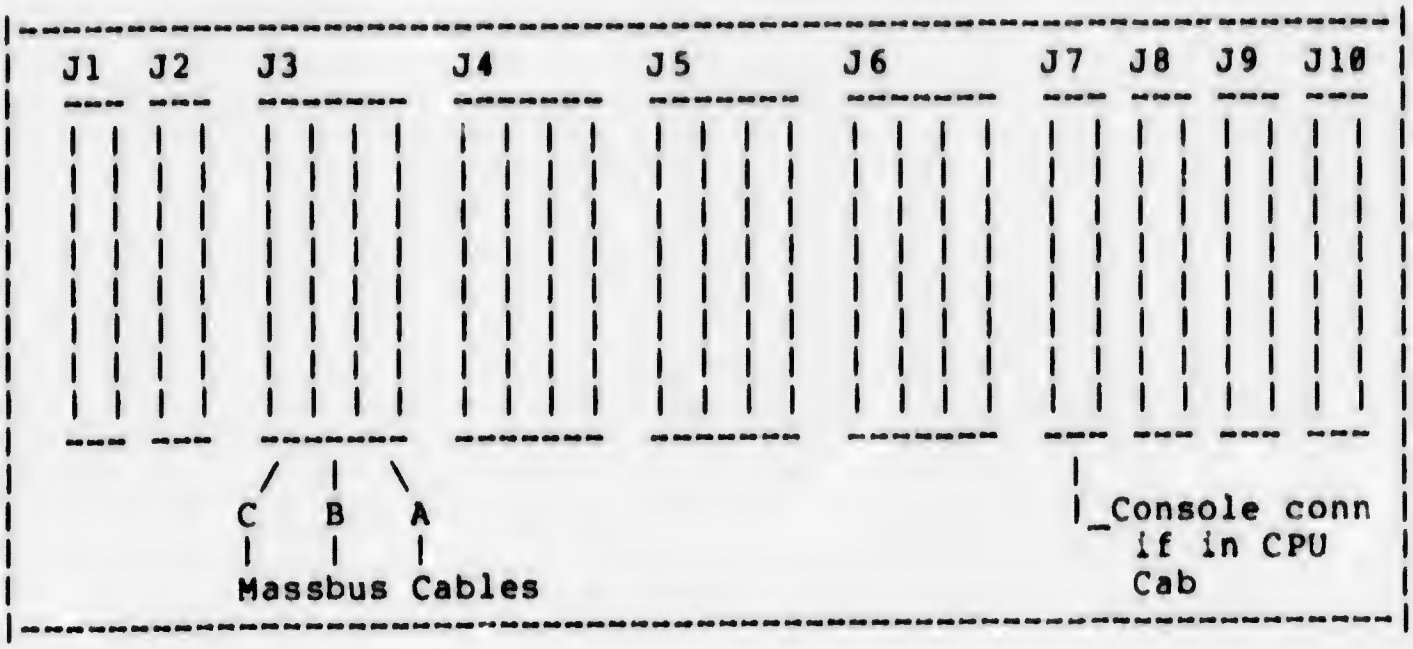
6.8 Side expander I/O connector panel viewed from inside cabinet. Massbus cables at J4, J5, & J6 are ribbed side to front and stripe down. Refer to Figure 4.

FIGURE 4
I/O Expander Connector Panel



6.9 I/O connector panel viewed from inside of cabinet. Refer to Figure 5. Massbus cables are ribbed side toward J1 and stripe up.

FIGURE 5.
I/O Connector Panel



7.0 POWER CHECKS

7.1 Power up H7100 (for RH780). Observe (POWER NORMAL) indicators. Check the following voltage/signals for correct readings. Refer to TABLE 5.

TABLE 5
Voltage Readings

VOLTAGE/SIGNAL	PIN	TOLERANCE
+5 Volts	C01A2	+4.9V to +5.2V
-5 Volts	J15 Pin 1	-5.0V to -5.3V
AC LOW	J14 Pin 1	-8.0V to -11.0V
	J13 Pin 1	-8.0V to -11.0V
DC LOW	J14 Pin 2	-8.0V to -11.0V
	J13 Pin 2	-8.0V to -11.0V

NOTE: Power Supply is not adjustable and must be repaired or replaced if out of range.

8.0 DIAGNOSTIC TEST PROCEDURE

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria, e.g.: pass counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the checklist.

8.1 Console terminal will display the following messages upon completion of boot.

8.1.1
```
CPU HALTED, SOMM CLEAR,STEP=NONE,CLOCK=NORM,
RAD=HEX,ADD=PHYS,DAT=LONG,FILL=00,
REL=000000
INIT SEQ DONE
HALTED AT 0000J000

(RELOADING WCS)
LOAD DONE, 00003200 BYTES LOADED
VER: PCS=01 WCS=0D-12 FPLA=0D CON=V05-01-L
>>>
```

8.1.2 Remove RX1 Diskette in drive, and insert RX2 Diskette.

```
T<CR>

ZZ-ESKAB V12.0
01,02,03,04,
NO. OF WCS MODULES = 0001
05,06,07,08,09,0A,0B,0C,0D,0E,0F,10,11,12,13,
14,15,16,17,18,19,1A,1B,1C,1D,1E,1F,20,
SYS ID REG= 81200996
21,22,23,24,25,26,27,28,29,2A,2B,2C,2D,2E,2F,
30,31,32,33,34,35,36,37,38,39,3A,3B,3C,3D,
END PASS 0001

MOUNT FLOPPY ZZ-ESZAD & TYPE "DI"

MIC>
```

8.1.3 Remove RX2 Diskette in drive, and insert RX3 Diskette.

```
DI<CR>

3E,
CPU TR= 00000010
MS780 16K CHIP AT TR 01
  MAX ADR+1= 00100000
DW780 AT TR 03
RH780 AT TR 08
RH780 AT TR 09
3F,40,41,42,43,44,45,46,47,48,49,4A,4B,4C,4D,
4E,
MS780 16K CHIP AT TR 01
  ARRAY #: 00000000
  # SINGLE BIT ERRORS:                    00000000
  ARRAY #: 00000001
  # SINGLE BIT ERRORS:                    00000000
  ARRAY #: 00000002
  # SINGLE BIT ERRORS:                    00000000
  ARRAY #: 00000003
```

```
  # SINGLE BIT ERRORS:                    00000000
4F,
MS780 16K CHIP AT TR 01
  M8213 ROMS OK
50,51,52
MP FPA

END PASS 0001

    CPU HALTED,SOMM CLEAR,STEP=NONE,CLOCK=
    NORM
    RAD=HEX,ADD=PHYS,DAT=LONG,FILL=00,
    REL=00000000
    INIT SEQ DONE
    HALTED AT 00000000

    (RELOADING WCS)
    LOAD DONE, 00003200 BYTES LOADED
    VER: PCS=01 WCS=0D-12 FPLA=0D
    CON=V05-01-L

    >>>
```

8.1.4 Remove RX3 Diskette and mount VAX CHANNEL DIAG. RX7.

```
    BOOT<CR>

    CPU HALTED
    INIT SEQ DONE
    LOAD DONE, 00014200 BYTES LOADED
DIAGNOSTIC SUPERVISOR,ZZ-ESSAA-6.1-370
7-AUG-1980 04:57:54


DS>
```

```
     ATT RH780 SBI RH0 8 5 <CR>
DS> ATT RH780 SBI RH1 9 5 <CR>
DS> SEL RH0 <CR>
DS> SEL RH1 <CR>
DS> RUN ESCAA <CR>

.. PROGRAM: ESCAA-REV,6.2 RH780 DIAGNOSTIC,
REV 6.2 20 TESTS, AT 11:40:37.22.
TESTING: -RH0 -RH1

RH0 BASE ADDRESS IS 20010000
DRIVE [0] RESPONDED
******* NO MBE PRESENT ON MASSBUS *******
RH1 BASE ADDRESS IS: 20012000
DRIVE [0] RESPONDED
******* NO MBE PRESENT ON MASSBUS *******
..END OF RUN. 0 ERRORS DETECTED. PASS COUNT:1
TIME: 5-AUG-1980 11:42:02.54

DS>
```

[END OF TEST]

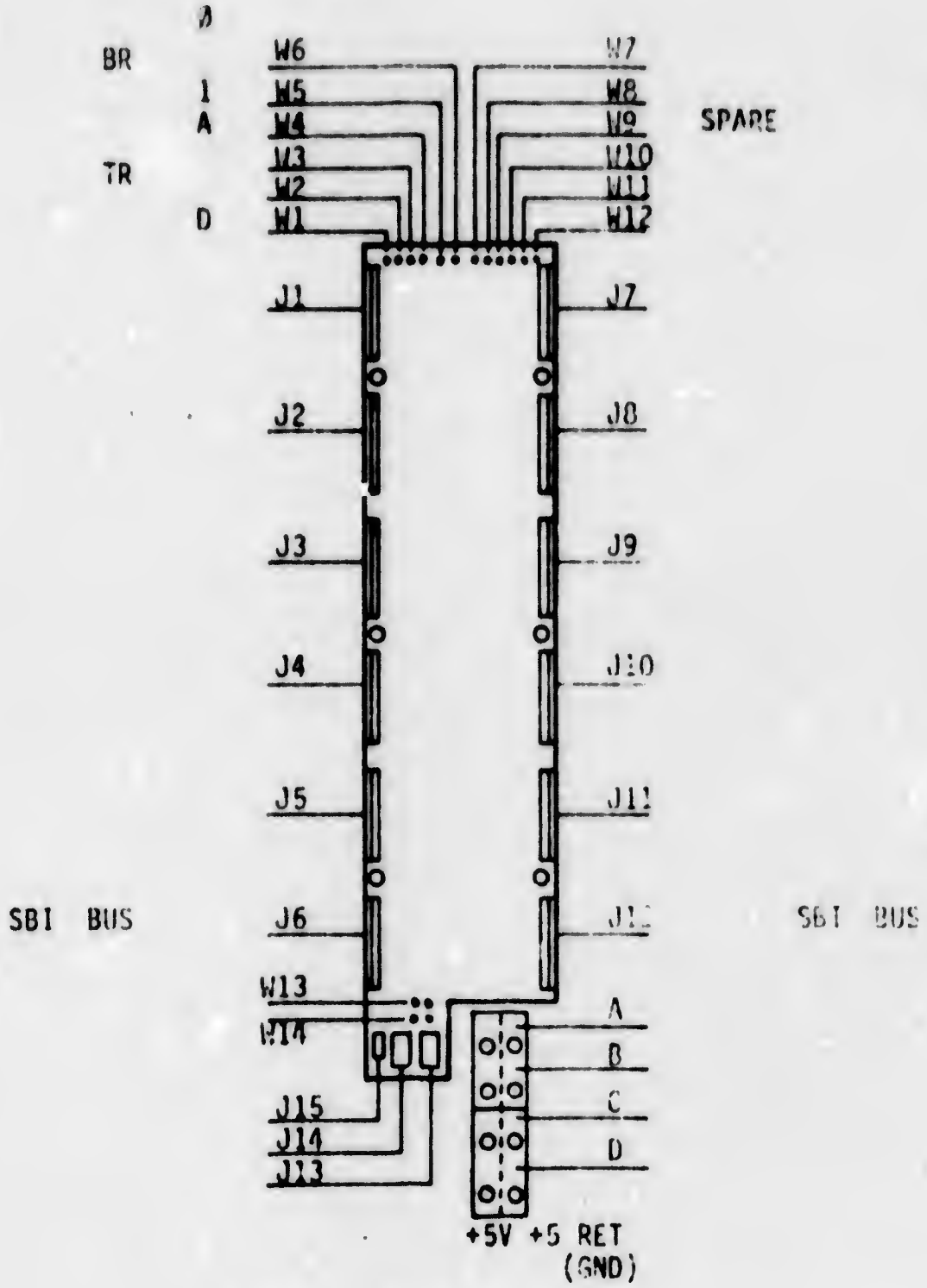
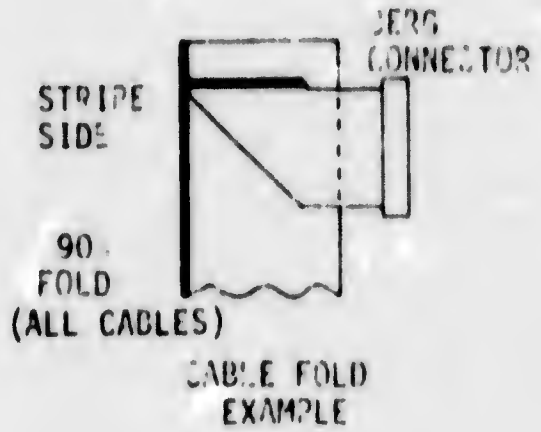


FIGURE 1 RH780 BACKPLANE
(Rear View)



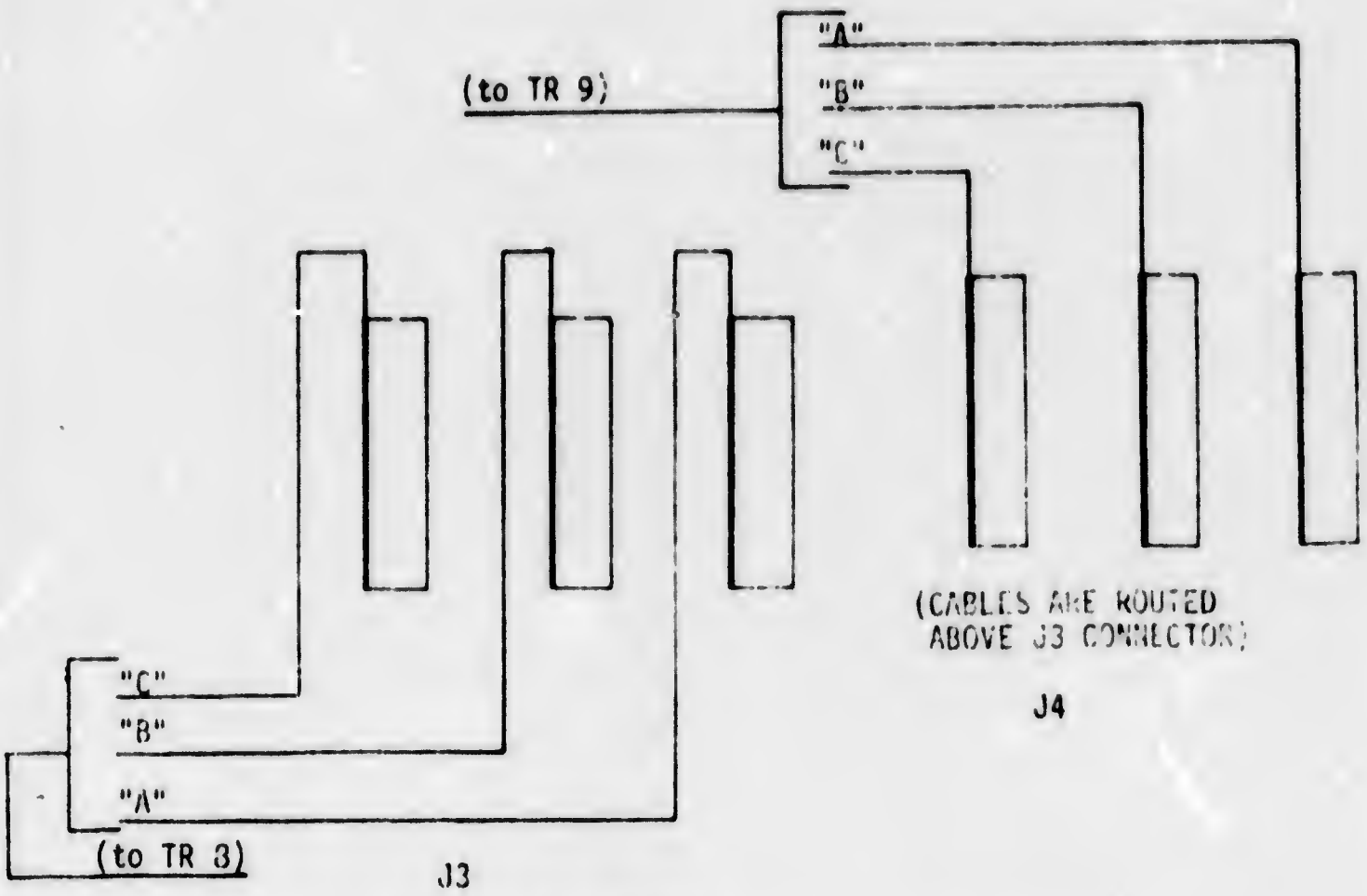


FIGURE 2 CABLING

(Cabling To Rear I/O Panel Of CPU Can).
(as viewed from inside of cab).

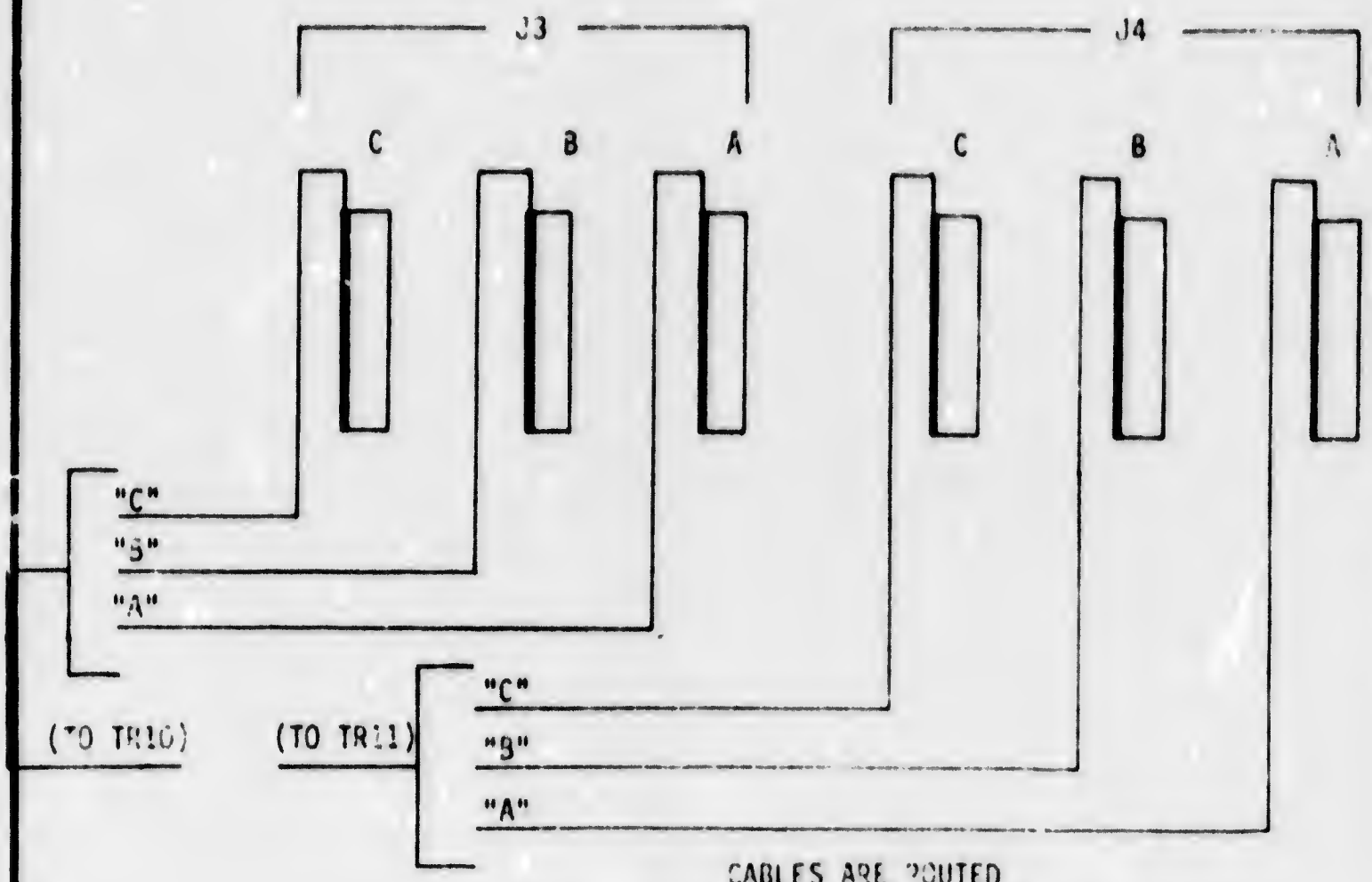


FIGURE 3 CABLING H9602-H ? EXPANDER CABINET

(Cabling To Rear I/O Expander Cab).
(as viewed from inside of cab).


V29

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 4/8/81

TITLE RH750 MAST BACKUP

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	NEW RELEASE	ML013	D. MONACO			6/3/81

D L Monaco

ENG	APPD	SIZE	CODE	NUMBER	REV
D. MONACO	Bob Beck	A	SP	MA-V2912-0-0	A

1.0 Introduction.

The RH750 or MASSBUS Adapter (MBA) is a general purpose interface between the Comet Memory Interconnect (CMI) and high speed massbus drives. It is a single extended hex module that is installed in one of three VAX KA750 CPU option slots. The extensive use of Gate Arrays allows this compact packaging. A single MBA can control up to eight different devices on the massbus. A maximum of three RH750's may be installed in the KA750. The MBA can handle data transfer rates up to 2 MB/sec.

2.0 Reference Documentation

2.1 Manuals

1.	750 Diagnostic System Overview	EK-VXD75-UG
2.	Hardware Handbook	EB-17281-20
3.	VAX11 Architecture Handbook	EB-17500-18
4.	VAX11 Software Handbook	EB-18057-20
5.	VAX Instruction Card	AV-D827A-TE
6.	750 Install. & Accept. Manual	EK-SI750-IN
7.	KC750 Microdiagnostics Tech. Manual	EK-KC750-TM
8.	Remote Diagnostics Users Guide	EK-KC750-UG
9.	RH750 Technical Discription	EK-RH750-TD

2.2 Prints

1.	11750 Field Maintenance Print Set	MP-00838
2.	KA750 Field Maintenance Print Set	MP-01024
3.	RH750 Field Maintenance Print Set	MP-01045

3.0 Required Test Equipment

1. VAX 11/750 CPU with 512KB Memory
2. EIA Console Terminal (ie. LA36,LA120)
3. Appropiate Load Media.

3.1 Optional Test Equipment

1. Oscilloscope Tektronix 465 or equivalent
2. D.V.M. accurate to .1 Vdc at 15 Vdc.
3. KC750 (RDM)
4. L9101 Comet Extender Module
5. Massbus Exerciser

4.0 Required Diagnostics

1.	Diagnostic Supervisor	ECSAA.EXE
2.	RH750 Diagnostic	ECCAA.EXE

5.0 Special Instructions

5.1 Throughout this procedure, it is assumed that the user is familier with DEC hardware, and the VAX 11/750.

5.2 The RH750 may be verified without the use of a drive or MRE through the use of its wrap-around mode.

6.0 Installation and Test Set-up Instructions

6.1 Unpacking instructions as received from High-Volume.

6.6.1 Unpack and save all boxes and packing material if it is needed to re-package the RH750 for shipment.

6.2 Visual Checks

6.2.1 With RH750 unboxed check for problems as per DEC standard 116 (broken parts , etc.).

6.3 Hardware Configuration

6.3.1 Install L0007 into KA750 (slots 7 - 9) as per system configuration sheet, reference figure 1.

6.3.2 Remove L0011 Comet Memory Controller from CPU, slot 10 reference module utilization section 6.4.

6.3.3 Install Massbus Boot Rom 23908A9 into E84 of the L0011 Comet Memory Controller, reference figure 2.

6.3.4 Reinstall L0011 into CPU slot 10.

CAUTION:

When installing Backplane Housing Connectors make sure that pins are engaged in the guide at each end of the housing and keyway is to the left as viewed from the rear of backplane. DO NOT USE EXCESS FORCE as connector will rest on the tops of the pins in the guide holes.

6.3.5 Install Backplane Housing Connectors onto KA750 Backplane in slot designated by system configuration sheet reference figure 3.

6.3.6 Remove BG Jumpers A67 - A68, A69 - A70, A73 - A74 and A77 - A78 from backplane slot RH is being installed into reference figure 3 and section 6.4 pin numbering.

6.3.7 Install device select and arbitration level jumpers as per system configuration sheet and figure 3 .

6.3.8 For normal Silo fill rate install Silo Fill Rate Jumper into A43 - A45.

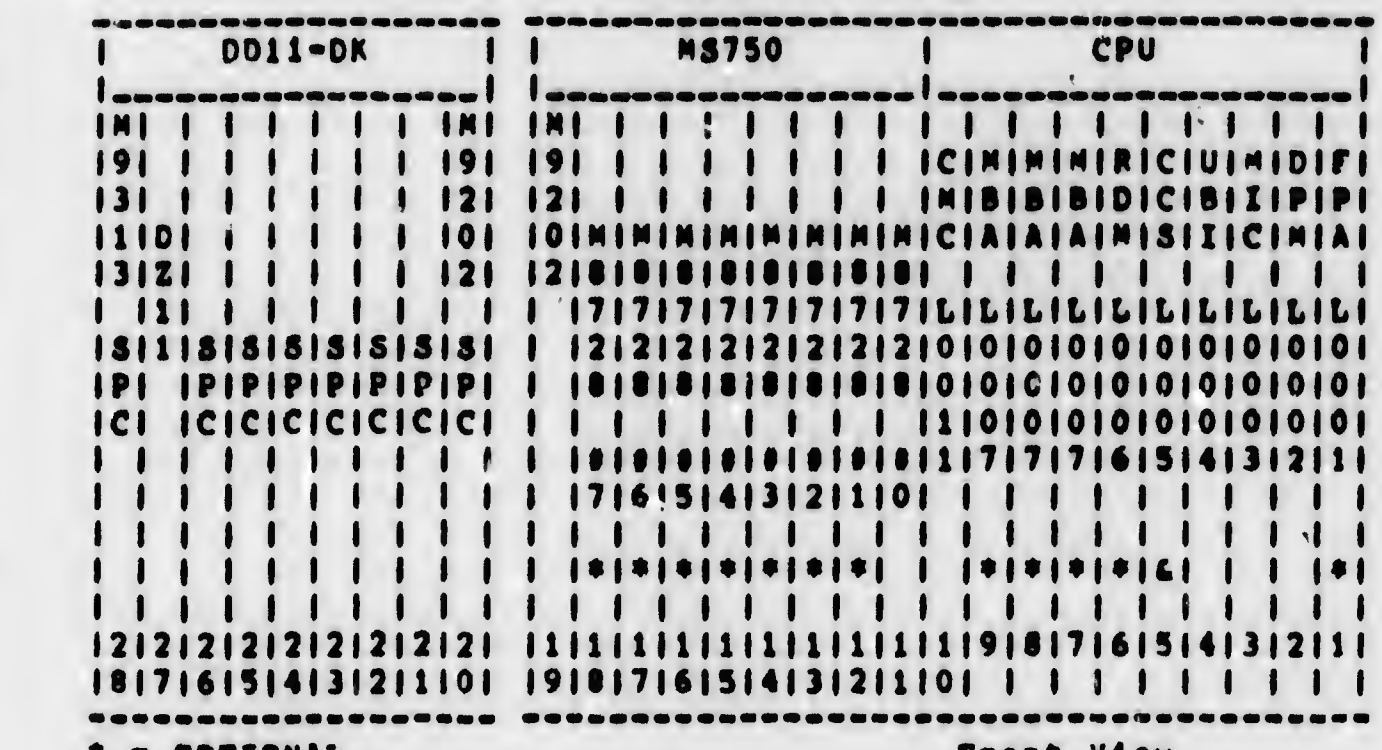
6.3.9 Remove appropriate blank panel cover from I/O panel, reference figure 4.

6.3.10 Install one end of the Massbus cable assembly 7018509-00 onto the Backplane Housing Connectors. Route cables up over cable cage and insert the other end through the I/O Panel and into the MASSBUS Receptacle Housing Assy. reference figures 4 and 5.

6.3.11 Install MASSBUS Receptacle Housing Assy. in I/O Panel assembly on the rear of the 11/750 reference figure 6.

6.4 Module Utilization

11/750 MODULE UTILIZATION



NOTE: There are three methods of pin numbering used in 11/750 CPU's.

PIN NUMBERING AND PLACEMENT EXAMPLES:

DD11-DK	MS750	11/750
A01A1 . . A01A2	A01A1 . . A01A2	A0101 . . A0102
A01B1 . . A01B2	A01B1 . . A01B2	A0103 . . A0104
A01C1 . . A01C2	A01C1 . . A01C2	A0105 . . A0106
A01D1 . . A01D2	A01D1 . . A01D2	A0107 . . A0108
A01V1 . . A01V2	A01V1 . . A01V2	A0193 . . A0194

7.0 Power Checks

7.1 Power requirements for RH750.

+ 5.0 volts
- 5.0 volts
+ 2.5 volts

NOTE: Voltages are provided by CPU power supply and are non adjustable with no checking necessary.

8.0 Diagnostic Test Procedures:

For the specific sequence of diagnostics to be run in any situation, or for the current MAST minimum test criteria, e.g.: pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are the detailed step-by-step instructions for executing individual diagnostics contained in the CHECKLIST.

NO ERRORS allowed on diagnostics.

8.1 Cassette Load of Diagnostic Supervisor

8.1.1 Insert cassette containing ECSAA.EXE Diagnostic Supervisor, into the TU58.

8.1.2 Set the Console Power on Action Switch to the Boot position.

8.1.3 Set the Device Select Switch to A.

8.1.4 Press the Reset Button located on the console panel.

When boot is complete console will respond with the following.

```
DIAGNOSTIC SUPERVISOR, ZZ-ECSAA-5.4-121  DD-MMM-YYY
DS>
```

8.2 System Disk Load of Diagnostic Supervisor

8.2.1 Place correct media in system disk and power up.

8.2.2 Set the Front Panel Power on Action Switch to the Halt position.

8.2.3 Set the Device Select to B, C or D. whatever your media is mounted on.

8.2.4 Depress the Console Reset Button, and wait for the console prompt.

8.2.5 Now type B/10 (drive type,controller,unit) <CR>

Example:

```
>>>B/10 DBA0 <CR>
   ---------------
```

When boot is complete console will print the following message.

```
DIAGNOSTIC SUPERVISOR, ZZ-ECSAA-6.1-175 DD-MMM-YYYY
DS>
```

8.3 Configuring The Diagnostic Supervisor

8.3.1 Before running RH750 diagnostic the Diagnostic Supervisor must be configured. Following is an example.

```
DS> ATTACH RH750 CMI RH0 5 <CR>
    ---------------------------

DS> SEL ALL <CR>
    -----------
```

NOTE:

It is assumed that the proper diagnostics are located on the load media being used. The following format will be used to illustrate running diagnostics under the Diagnostic Supervisor.

8.X Diagnostic name

```
DS> RUN XXXXX <CR>          (how to start diagnostic)
    --------------          (operator input indicator)
XXXXXXXXXXX                 (beginning of run print out)
XXXXXXXXXXX                 (special instructions)
XXXXXXXXXXX                 (end of run print out)
```

8.4 DS> RUN ECCAA <CR>

(Example of running wrap-around mode)

```
PROGRAM: ECCAA-REV. 1.0 RH750 DIAGNOSTIC, REV 1.0, 20 TEST
TESTING: _RH0

RH0 BASE ADDRESS IS: 40F28000
NO DRIVE RESPONDED.
*******  NO MBE PRESENT ON MASSBUS  *******
.. END OF RUN.  0 ERRORS DETECTED.  PASS COUNT: 1.
```

(Example of running with drive connected)

```
PROGRAM: ECCAA-REV. 1.0 RH750 DIAGNOSTIC, REV 1.0, 20 TEST
TESTING: _RH0

RH0 BASE ADDRESS IS: 40F28000
DRIVE 0 RESPONDED.
*******  NO MBE PRESENT ON MASSBUS  *******
.. END OF RUN.  0 ERRORS DETECTED.  PASS COUNT: 1.
```

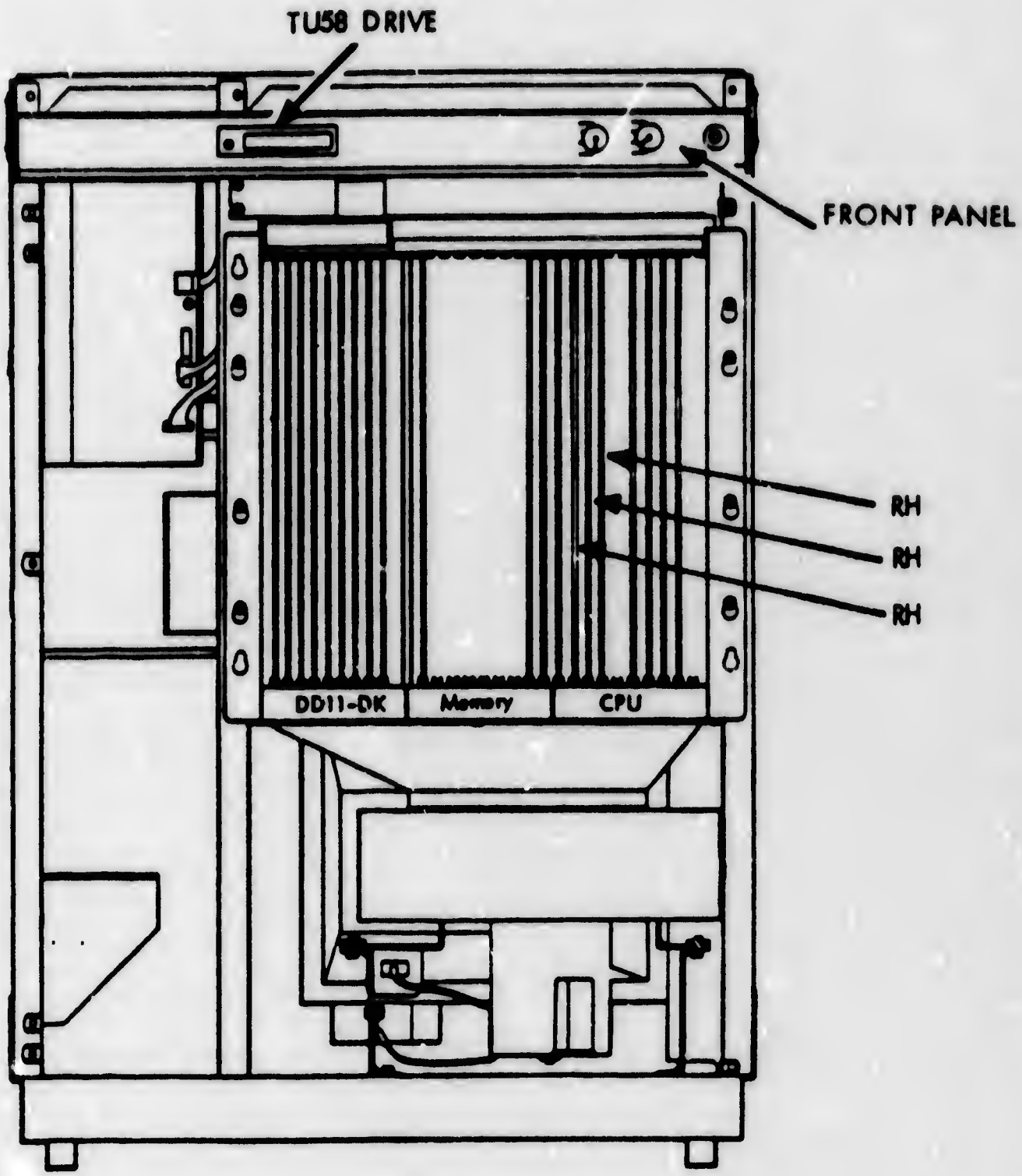


FIGURE 1
RH750 MODULE
INSTALLATION

L0011 C.M.C.

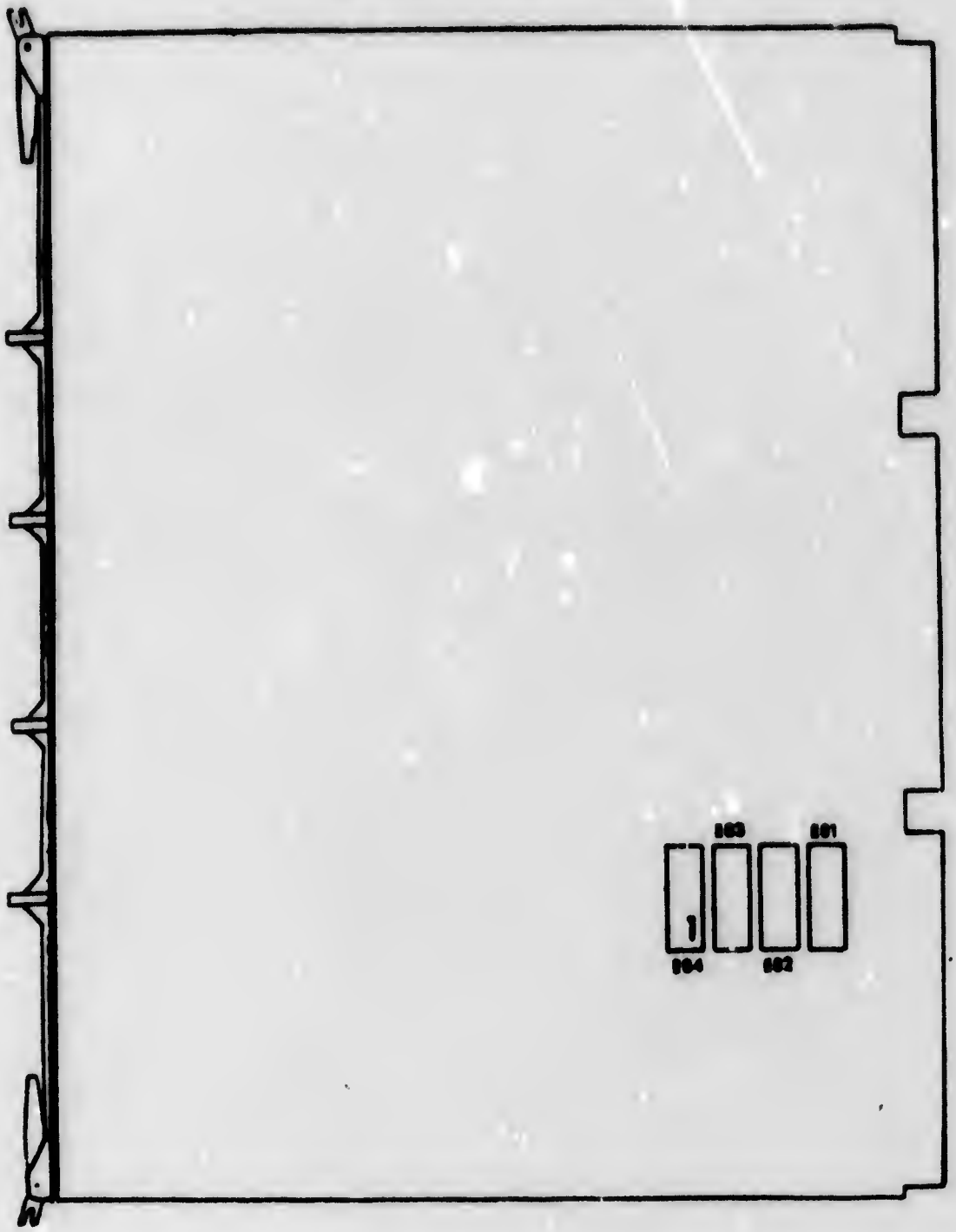


FIGURE 2
Comet Memory
Controller

RH750 CONFIGURATION JUMPERS		
RH SELECT	BASE ADDRESS	JUMPERS
0	F28000	A51-A53 A52-A54
1	F2A000	A51-A53
2	F2C000	A52-A54
ARBITRATION LEVEL		JUMPERS
3		A62-A64
2		A60-A62 A63-A64
1		A60-A62 A64-A66 A61-A63
SILO FILL RATE		JUMPERS
NORMAL		A43-A45

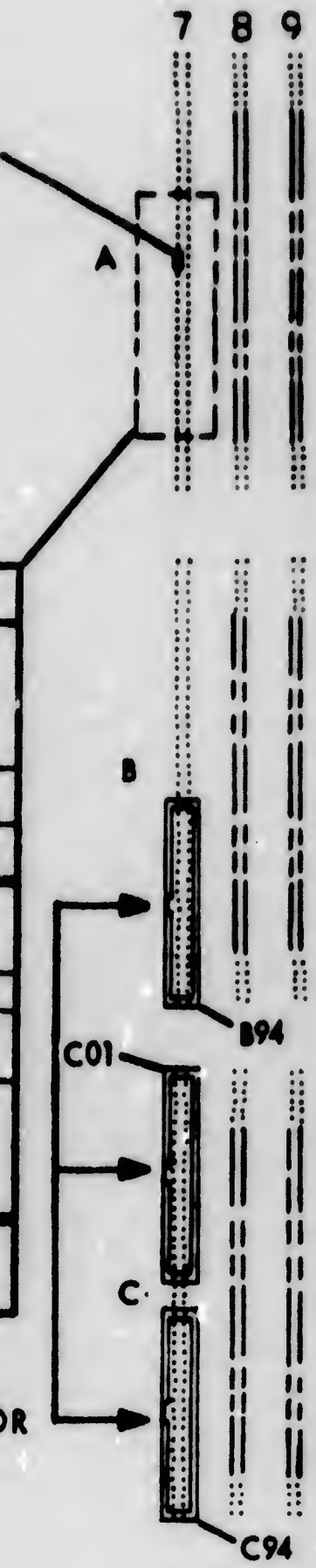


FIGURE 3
BACKPLANE SETUP

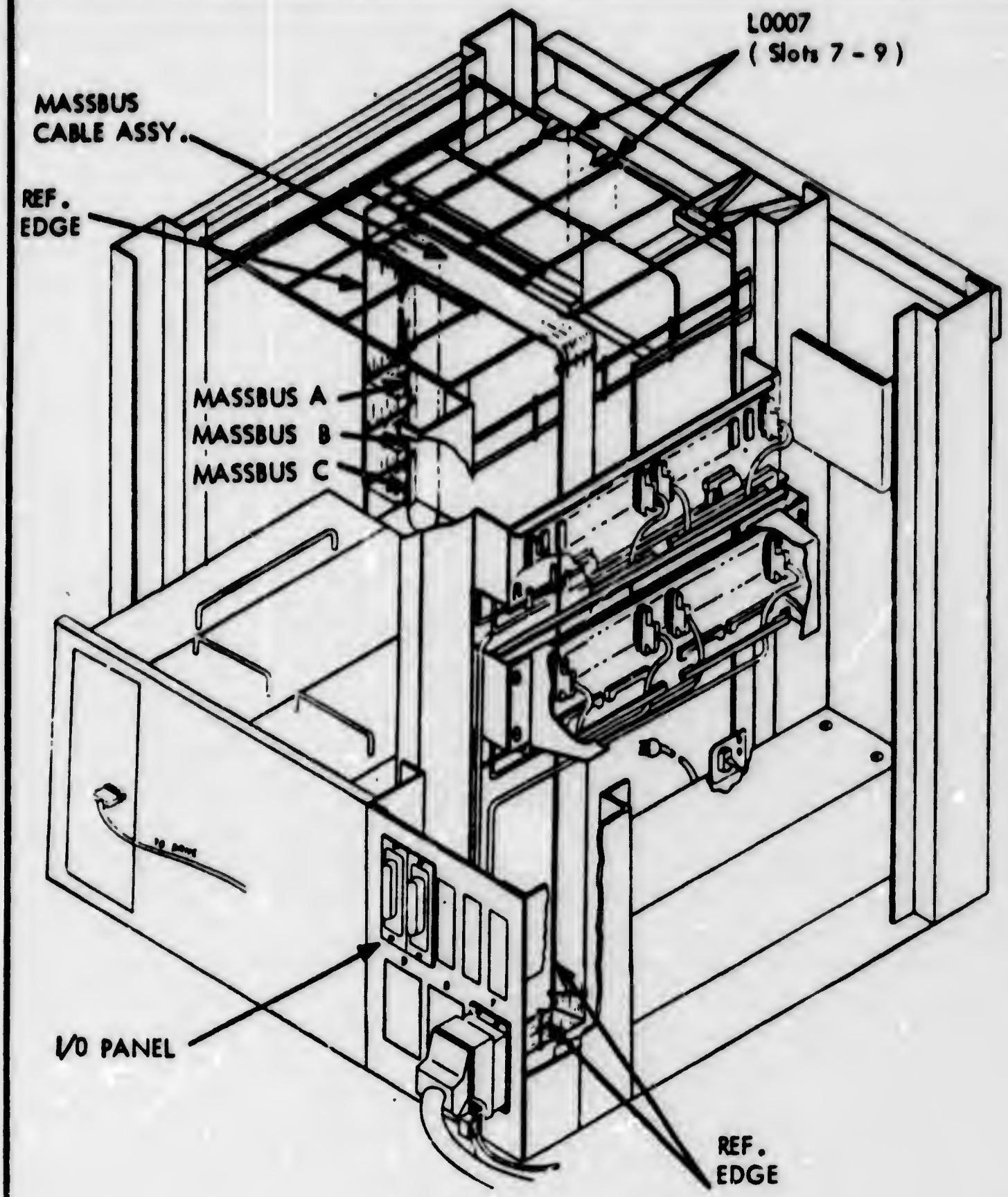


FIGURE 4
RH750 CABLE ROUTING

	SIZE	CODE	NUMBER	REV
	A	SP	MA-V2912-0-0	A

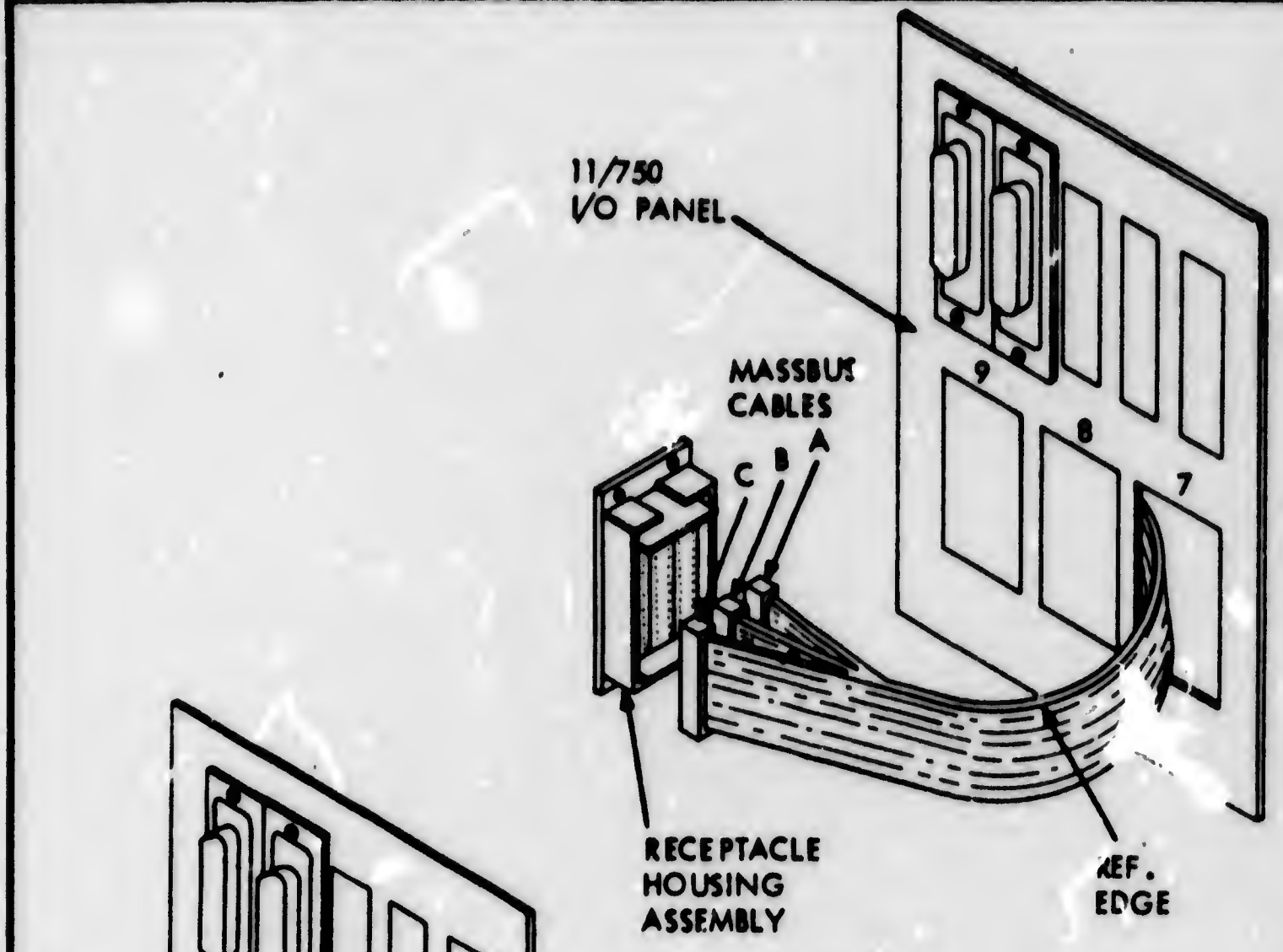


FIGURE 5
I/O PORT CABLING

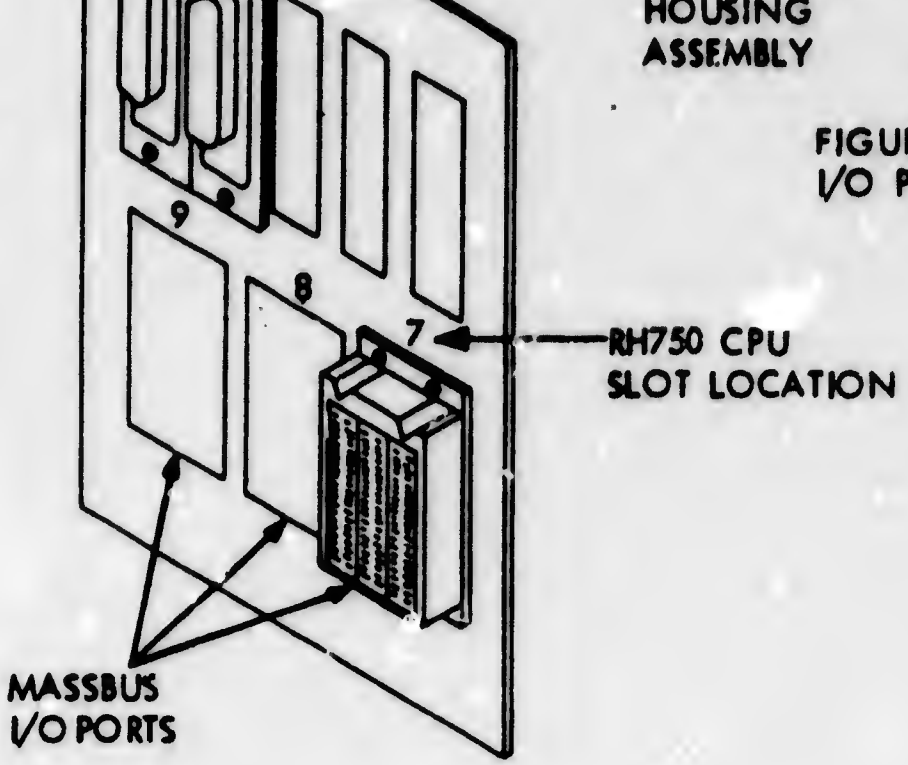


FIGURE 6
I/O PANEL WITH
MASSBUS CONNECTOR

DRAWING NO.	REV.NO.	PPS.	DESCRIPTION
A-SP-MAA6176	C	24	DPM50 DIST I/O SUBSYSTEM
A-SP-MAA6180	A	2	AR11 SYSTEM
A-SP-MAA6190	A	2	NC11 GAMMA CAMERA
A-SP-MAA6192	A	6	NCV11 GAMMERA CAMERA INTERFACE
A-SP-MAA6205	A	4	DR11-A GENERAL DEVICE
A-SP-MAA6210	A	4	DR11-B DMA DEVICE
A-SP-MAA6220	A	4	DR11-C GENERAL DEVICE
A-SP-MAA6225	A	3	DRV11 16 BIT PLU-PDP11/03
A-SP-MAA6227	A	8	DRV11-J PARALLEL INTERFACE
A-SP-MAA6230	A	2	DT03 BUS SWITCH
A-SP-MAA6240	A	2	DA11-BD UNIBUS WINDOW
A-SP-MAA6260	A	4	DR11-K GENERAL I/O
A-SP-MAA6275	A	5	DR11-W GENERAL PURPOSE (DMA)
A-SP-MAA7110	A	2	BD03 ASCII/BINA
A-SP-MAA7120	A	2	BD04 DISK INT ALARM
A-SP-MAA7130	A	2	BD05 LINE CONTROL
A-SP-MAA7210	A	2	REORDER TRAP DEVICE
A-SP-MAA7510	C	14	LPD-11/LPC01 INTERFACE
A-SP-MAA7600	A	10	CSIG2-A RAINBOW TST-ACCP.PROC.
A-SP-MAA8010	A	2	UNIBUS TESTER
A-SP-MAA9025	A	4	PRE ACCEPTANCE HARDWARE Q.C.
A-SP-MAD2440	A	12	KT8-A
A-SP-MAD4216	A	16	RL8-A/RL01
A-SP-MAE0050	C	6	MAST PHASE III UETP
A-SP-MAE1000	A	44	PHASE III BACKUP DOC. RSX11-M
A-SP-MAF1050	A	14	WPS-8/211 PHASE III USER'S GUIDE
A-SP-MAF2050	A	16	WPS-8/212 PHASE III USER'S GUIDE
A-SP-MAV2100	B	26	11/780 CPU
A-SP-MAV2102	A	32	11/750 MAST I

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE 20 June 80

TITLE DPM50 DISTRIBUTED I/O SUBSYSTEM

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	Updated and revised	MA-A0000 ML010		20/06/80		

ENG	APPD	SIZE	CODE	NUMBER	REV
BILL WHITBY	~~STU~~ ESTES	A	SP	MAA 6176-0-0	C

EN-01983-16-N572-(392)

DPM-50 DISTRIBUTED I/O SUBSYSTEM

1.0 INTRODUCTION:

The DPM-50 distributed systems are based on single boxed configurations of either the KD11-H LSI-11 microcomputer or the KDF11-AA (11/23) microcomputer,power supply,process I/O modules and DEC DATAWAY interface. The purpose is to provide process I/O for the LSI-11 and thereby offer low cost distributed intelligent systems fully supported by software. The KDF11-AA configuration offers in addition PDP-11/34 functionality on the LSI-11 bus, memory management as a standard feature and optional floating point option(KEF11-A).

2.0 REFERENCE DOCUMENTATION:

2.1 MANUALS:

2.1.1 MICROCOMPUTER HANDBOOK: EB 15836-18/79
2.1.2 MSV11-D,-E USERS MANUAL: EK MSV1D-OP-???
2.1.3 PROCESS I/O SUBSYSTEM USERS GUIDE: EK-PIOS-UG-???
2.1.4 DPM50 USERS GUIDE: EK-DPM50-UG-???
2.1.5 KDF11-AA USERS GUIDE: EK-KDF11-UG-???
2.1.6 MICROCOMPUTER INTERFACES HANDBOOK EB-17723-20/80

2.2 PRINTS AND SCHEMATICS:

2.2.1 H333 PRINT SET: MP00424
2.2.2 ISV11-A PRINT SET. MP00609
2.2.3 TEV11 PRINT SET: MP00074
2.2.4 [illegible] PRINT SET: MP00433
2.2.5 DLV11-F PRINT SET: MP00461
2.2.6 KDF11-AA PRINT SET MP00734
2.2.7 MSV11-D PRINT SET: MP00566

3.0 REQUIRED TEST EQUIPMENT:

3.1 HARDWARE AND MEDIA:

3.1.1 Valid DPM host system configuration.
3.1.2 RSX11-M on appropriate media.
3.1.3 Attenuation panel.
3.1.4 HEWLETT PACKARD DVM or equivalent accurate to .01V @ 15V.
3.1.5 Serial line unit IE. DLV11-F and terminal for LSI error information output (local).

4.0 REQUIRED DIAGNOSTIC PROGRAMS:

4.1 DPM50 Diagnostics Kit #ZP125-RD

	NAME	DESCRIPTION	MODE
4.1.1	DZKCI	Remote Terminal Tester	Remote
4.1.2	DZKCH	Serial Bus Exerciser	Remote
4.1.3	CZKMP	Task Handler	N/A
4.1.4	DVKAA	Basic Instruction Test	Local&Remote
4.1.5	DVKAB	EIS Instruction Test	Local&Remote
4.1.6	DVKAC	FIS Instruction Test	Local&Remote
4.1.7	DVKAD	LSI-11 Traps Test	Local&Remote
4.1.8	DVDVC	DLV11-F Test	Local&Remote
4.1.9	DVKAH	4K System Exerciser	Local
4.1.10	CZQMC	0-124K Memory Exerciser	Local&Remote
4.1.11	DVPCA	PCS Test	Local&Remote
4.1.12	CJKDA	F-11 MMU Test	Local&Remote
4.1.13	CJKDB	F-11 CPU Test	Local&Remote
4.1.14	CVDLA	DLV11-J Test	Local&Remote
4.1.15	CJKDC	KEF11-AA Diag 1	Local&Remote
4.1.16	CJKDD	KEF11-AA Diag 2	Local&Remote
4.1.17	CZKMA	0-124K Memory Exerciser	Local&remote

5.0 SPECIAL INSTRUCTIONS:

5.1.1 RSX11-M must be running in the host system with DPM50 diagnostics kit #ZP125-RD.

5.1.2 Due to power supply limitations, only two of the below supported options can be installed at any one time in F and H variations of the DPM50. Since a terminal interface is required to run diagnostics in local mode one of the two options must be the DLV11-F or DLV11-J

A. DLV11-F
B. DLV11-J/DLV11-KA
C. DZV11-B
D. MSV11-D
E. RXV11 or RXV21 *

* Floppy disk options not supported by a local boot.

6.0 INSTALLATION AND TEST SETUP INSTRUCTIONS:

6.1 UNPACKING AND INSPECTION:

6.1.1 Save all packing material for equipment to be shipped that is not cab mounted.

6.2 MODULE CONFIGURATION SETUPS FOR DPM50

6.2.1 KD11-H(M7264) LSI CPU MODULE

JUMPER DESIGNATION	JUMPER STATE
W1	OUT
W2	OUT
W3	OUT
W4	IN
W5	OUT
W6	OUT
W7	IN
W8	IN
W9	IN
W10	OUT
W11	OUT

The KEV11A EIS/FIS chip is installed in location E75 on M7264 LSI CPU module. Refer to Figure 1.

6.2.2 KDF11-AA(M8186) LSI 11/23 CPU module (DPM50 F/H variations only).

JUMPER DESIGNATION	JUMPER STATE
W1	IN
W2	AS RECEIVED
W3	AS RECEIVED
W4	OUT
W5	OUT
W6	OUT
W7	IN
W8 THRU W15	DON'T CARE
W16	IN
W17	IN
W18	IN

Reference Figure 2 for jumper locations.

6.2.3 MSV11-DD(M8044-D?) FIRST 32K

S1 SWITCHPACK	SWITCH STATE
SW1	ON
SW2	ON
SW3	ON
SW4	ON
W2	IN
W3	IN
PIN 1 TO 3	IN
PIN 5 TO 7	IN
PIN 10 TO 14	IN
PIN 15 TO 16	IN

Reference Figure 4 for switch and jumper locations.

6.2.4 DLV11-F(M8028) SERIAL LINE UNIT

JUMPER DESIGNATION	JUMPER STATE
T0	OUT
T1	IN
T2	OUT
T3	IN
R0	OUT
R1	IN
R2	OUT
R3	IN

The DLV11-F is default jumpered for console use,but the baud rate jumpers must be reconfigured from 110 baud operation to 300 baud.

The DLV11-F is not a standard part of the DPM50 system, but is a frequent option. See Figure 9 for jumper locations.

6.2.5 ISV11-A (M8080,5413290) SERIAL BUS INTERFACE

FACTORY CONFIGURED:

CSR ADDRESS	160140
	160142
	160144
VECTOR ADDRESS	300
	304

JUMPERS	STATE	LOCATION
W1 THRU W6	OUT	M8080
W7 THRU W10	IN	M8080
W11 THRU W16	OUT	M8080
W17 THRU W20	IN	M8080
W21 THRU W23	OUT	M8080
W1,W3,W5,W7,W9	IN	5413290
W2,W4,W6,W8,W10	OUT	5413290

See Figures 7.1 and 7.2 for jumper locations.

If DLV11-J installed default starting vector address of 300 must be reconfigured because of its conflict with the ISV11-A.

6.2.6 I/O CONTROL MODULE(M7958)

CSR ADDRESS 171000

VECTOR ADDRESS 234

VECTOR SWITCH PACK E7	SWITCH STATE
SW1	ON
SW2	ON
SW3	ON
SW4	OFF
SW5	OFF
SW6	ON
SW7	OFF
SW8	OFF

ADDRESS SWITCH PACK E34	SWITCH STATE
SW1	OFF
SW2	ON
SW3	OFF
SW4	OFF
SW5	ON
SW6	OFF
SW7	OFF
SW8	ON

Reference Figure 8 for switchpack locations.

6.2.7 TEV11(M9400-YB) TERMINATOR MODULE

JUMPER DESIGNATION	JUMPER STATE
W1	IN
W2	OUT
W3	IN
W4	OUT

Reference Figure 3 for jumper locations.

6.3 CABLING OF THE DPM50

6.3.1 Cabling of the DPM50 consists of a serial bus cable (70-15928-03) coming from the daughter board (54-13290) of the ISV11-A mother/daughter pair,which interconnects with the DEC DATAWAY cable (70-14152),which in turn is run through an attenuation panel to simulate cable length,finally exiting the attenuation panel and connecting to the host CPU'S ISB11. See Figures 5,7.2 and 10.

Attenuation panel is only used for test and is not shipped with the system.

DEC DATAWAY is keyed.

7.0 POWER CHECKS

7.1 +5.1VDC +.1-.15
+12VDC +.1-.36

If voltages are out of tolerance remove the H7870 power supply cover and slide the power supply out until access to the adjustments is possible. Reference Figure 6.

8.0 DIAGNOSTIC TEST PROCEDURE

The host processor,whether it be an 11/70 or 11/34 along with its ISB11'S must be fully checked out according to MAST prior to connecting a DPM50 to the DATAWAY.

8.1 DPM50 HOST SYSTEM BOOTING PROCEDURE

8.1.1 Obtain a disk pack for the appropriate host media which has the RSX11-M host package #AP-F152A-MC and install it into DRIVE #0. Load DRIVE #0 and insure that "WRITE PROTECT" is off.

8.1.2 When DRIVE #0 is ready and "ON LINE" (heads loaded) BOOT the drive.

8.1.3 When the program asks for the date and time, you may either enter the information or default it by typing a carriage return. An example would be 08:30 04-JUN-80.

8.1.4 The program will continue setting up parameters and will ask: "Do you want to load IPG diagnostics from magtape [Y/N]:". Type in a carriage return which will default your answer to a NO condition.

8.1.5 The program will now output:
>@ <EOF> (This signifies end of file and parameters are now set) and waits for you to key in a command.

8.1.6 Type in:
Set /UIC=[200,270] (This may not be necessary if the UIC is already at 200,270.)

8.2 RUN THE ERROR REPORT TASK IN ORDER TO CLEAR OUT THE ERROR LOG

8.2.1
```
>RUN ISBRPT--------------------------TYPE:<RUN ISBRPT>
ISBRPT-DEC DATAWAY ERROR REPORT TASK
>
PRINT SUMMARY [Y OR N]?N------------TYPE:<N>
PRINT ENTIRE FILE [Y OR N]?N--------TYPE:<N>
DELETE ERROR FILE [Y OR N]?Y--------TYPE:<Y>
ISBRPT...OPERATION COMPLETE
TASK "ISBRPT" TERMINATED
TASK EXIT WITH OUTSTANDING I/O
PC=125130
PS=170000
R0=120720
R1=125576
R2=125650
R3=000000
R4=143470
R5=000000
SP=120476
```

8.2.2 Type:CTRL C to terminate ISBRPT task and receive back MCR> prompt.

8.3 RUN THE DEC DATAWAY DIAGNOSTIC EXERCISER.

8.3.1 >RUN DZKCH----------TYPE:<RUN DZKCH>
DCP-A>STA----------TYPE:<STA>

#UNITS (D)?1----------TYPE:<1>
ENTER CONTROLLER NUMBER:(O)0?0------TYPE:<0>
ENTER TERMINALS ON THAT CONTROLLER:
(O)1?1----------TYPE:<1>
NUMBER OF ENTERED TERMINALS=1

UNIT**CONTROLLER**LOGICAL SB**LUN**
001 000 001 011

TOTAL ACTIVE PASSES = 21,ACTIVE TERMINALS=1, TIME=8:33

TOTAL ACTIVE PASSES = 41,ACTIVE TERMINALS=1, TIME=8:34

8.3.2 After required run time has elapsed terminate running of diagnostic by typing CTRL C.

TASK "TTO" TERMINATED
TASK EXIT WITH OUTSTANDING I/O
PC=046000
PS=170000
R0=000002
R1=000000
R2=000000
R3=000000
R4=000003
R5=000001
SP=001246

8.4 After DZKCH has run,The error log must be checked for errors that may have occured during running.

8.4.1 >RUN ISBRPT----------TYPE:<RUN ISBRPT>
ISBRPT-DECDATAWAY ERROR REPORT TASK
>
PRINT SUMMARY[Y OR N]?Y----------TYPE:<Y>
PRINT ENTIRE FILE [Y OR N]?N--------TYPE:<N>
OUTPUT TO LINE PRINTER [Y OR N]?N---TYPE:<N>
WANT ONE CONTROLLER [Y OR N]?N------TYPE:<N>
DELETE ERROR FILE [Y OR N]?N--------TYPE:<N>
ISBRPT...ERROR FILE IS EMPTY
ISBRPT...OPERATION COMPLETE

8.4.2 Type: CTRL C to terminate ISBRPT task and receive back MCR> prompt.

8.4.3 Error reporting can be in the form of hard errors, typed out immediately, or soft errors; Errors that are logged by the error logger. No errors are allowed.

8.5 RUN ROM RESIDENT TESTS OF ISV11-A

8.5.1
```
MCR>RUN CZKCIB----------------------TYPE:<RUN CZKCIB>
>
DCP-A>STA---------------------------TYPE:<STA>

# UNITS (D) ? 1---------------------TYPE:<1>

UNIT 1
ENTER CONTROLLER NUMBER:(0)0?0------TYPE:<0>
ENTER TERMINALS ON THAT CONTROLLER:
(D)1?1-----------------------------TYPE:<1>

SELECTED SERIAL LINE PORTS

UNIT**CONTROLLER**LOGICAL SB**LUN**TYPE
  1         0           001       9    DPM50-PORT 0

START OF TESTING

END OF PASS      0,    TIME = 9:29

END OF PASS      1,    TIME = 9:31
```

8.5.2 After required run time has elapsed terminate running of the diagnostic by typing CTRL C.

8.6 LOAD DIAGNOSTIC MONITOR CZKMPB

8.6.1
```
>RUN CZKMPB-------------------------TYPE:<RUN CZKMPB>
>
CZKMPB VERSION 2.2
SELECT MODE: LOCAL, HOST, AUTO-MAP, COMMUNICATION OR EXIT
(L,H,A,C,E)L-----------------------TYPE:<L>
ENTER NUMBER OF TERMINALS [D]=1-----TYPE:<1>
ENTER CONTROLLER NUMBER [0]=0-------TYPE:<0>
ENTER TERMINAL NUMBERS [0]=1--------TYPE:<1>
NUMBER OF ENTERED TERMINALS = 1
UNIT**CONTROLLER**LOGICAL SB**
  1         0           1
```

At this point the console terminal at the DPM50 subsystem comes on line and is used to ask for and run subsystem diagnostics.

If DPM50 contains an 11/23 CPU (KDF11-AA), proceed to section 8.8 otherwise go to section 8.7.

8.7 RUN 11/03 (KD11-H) BASED DPM50 LSI DIAGNOSTICS

See Figure 11 for explanation of monitor interaction at DPM50 local terminal.

LTC switch must be in the off position to run diagnostics.

8.7.1
```
>VKAAC0-------------------------------TYPE:<VKAAC0>
157776
@200G---------------------------------TYPE:<200G>
END PASS
END PASS
```

8.7.2 After required run time has elapsed, terminate running of the diagnostic by depressing the break key on the DPM50 console terminal.

8.7.3
```
@760144/000000 2----------------------TYPE:<760144/>
                                      TYPE:<2>
>VKABA0-------------------------------TYPE:<VKABA0>
157776
@200G---------------------------------TYPE:<200G>
END PASS
END PASS
```

8.7.4 After required run time has elapsed, terminate running of the diagnostic by depressing the break key on the DPM50 console terminal.

8.7.5
```
@760144/000000 2----------------------TYPE:<760144/>
                                      TYPE:<2>
>VKACC1-------------------------------TYPE:<VKACC1>
157776
@200G---------------------------------TYPE:<200G>
DVKACC-LSI-     LS INSTRUCTION TEST
END PASS
END PASS
```

8.7.6 After required run time has elapsed, terminate running of the diagnostic by depressing the break key on the DPM50 console terminal.

8.7.7 @760144/000000 2----------TYPE:<760144/>
TYPE:<2>
>VKADC0----------TYPE:<VKADC0>
157776
@200G----------TYPE:<200G>
CVKADC0 LSI-11 TRAPS TEST

EIS/FIS OPTION PRESENT
DIBOL INSTRUCTION SET NOT PRESENT
END OF PASS

8.7.8 After required run time has elapsed, terminate running of the diagnostic by depressing the break key on the DPM50 console terminal.

8.7.9 @ 60144/000000 2----------TYPE:<760144/>
TYPE:<2>
>ZKMAF0----------TYPE:<ZKMAF0>
157776
@200G----------TYPE:<200G>
CZKMAF0
000000--157776
TST 13 BNK 00
TST 13 BNK 01
TST 13 BNK 02
TST 13 BNK 03
TST 13 BNK 04
TST 13 BNK 05
TST 13 BNK 06
RELOC
TST 13 BNK 00
PASS# 01

8.7.10 After required run time has elapsed,terminate running of the diagnostic by depressing the break key on the DPM50 console terminal.

8.7.11 Load and run diagnostics for any additional LSI option modules added to the base DPM50 system, using same method used to run CPU tests.

8.7.12 After all LSI modules have been run, if any D Bus I/O modules exist, load in diagnostic VPCAE0 from the host processor and follow procedure P00-00C0A-00-000-WM-06-8055. Reference section 4.0 DIAGNOSTIC TESTING

8.8 RUN 11/23(KDF11-AA) BASED DPM50 DIAGNOSTICS

See Figure 11 for explanation of monitor interaction inputs and outputs at local DPM50 terminal.

LTC switch must be in OFF position to run diagnostics.

```
8.8.1 >JKDAC0------------------------------TYPE:<JKDAC0>
      157776
      @200G--------------------------------TYPE:<200G>
      CJKDAC0 KTF11-AA MMU DIAG.
      SWR=000000 NEW=CR--------------------TYPE:<CR>

      END PASS#   1  ;TOTAL ERRORS SINCE LAST START AT 200   0
```

8.8.2 After required run time has elapsed, terminate running of the diagnostic at the DPM50 console terminal by depressing the break key.

```
8.8.3 @760144/000000 2--------------------TYPE:<760144/>
                                          TYPE:<2>
      >JKDBC0------------------------------TYPE:<JKDBC0>
      157776
      @200G--------------------------------TYPE:<200G>
      CJKDBC0 DCF11-AA CPU DIAGNOSTIC
      END PASS#  1
      END PASS#  15
```

8.8.4 After required run time has elapsed,terminate running the diagnostic at the DPM50 console terminal by depressing the break key.

```
8.8.5 @760144/000000 2--------------------TYPE:<760144/>
                                          TYPE:<2>
      >ZQMCG0------------------------------TYPE:<ZQMCG0>
      157776
      @200G--------------------------------TYPE:<200G>
      SWR=000000 NEW= CR-------------------TYPE:<CR>

      KT11(MEMORY MANAGEMENT)AVAILABLE

      MEMORY MAP
      FROM 000000 TO 757777 (WITH 4 MSV11-D INSTALLED)
      NO PARITY REGISTERS FOUND
      PROGRAM RELOCATED TO 720000
      PROGRAM RELOCATED TO 000000
      END PASS# 1
```

Above will be received when 4 MSV11-D modules are installed, typeouts will vary with lesser amounts of memory. No relocation will occur when only 1 MSV11-D installed.

8.8.6 *NOTE THE following two tests are to be run if the optional KEF11 chip is installed.

8.8.7 @760144/000000 2----------TYPE:<760144/>
TYPE:<2>
>JKDCB0----------TYPE:<JKDCB0>
157776
@200G----------TYPE:<200G>
CJKDCB, KEF11-A FP DIAGNOSTIC PART 1

SWR = 000000 NEW=CR----------TYPE:<CR>

END PASS # 1
END PASS # 2

8.8.8 After required run time has elapsed, terminate running of the diagnostic at the DPM50 console terminal by depressing the break key.

8.8.9 @760144/000000 2----------TYPE:<760144/>
TYPE:<2>
>JKDDB0----------TYPE:<JKDDB0>
157776
@200G----------TYPE:<200G>
CJKDDB KEF11-A DIAGNOSTIC PART 2

SWR = 000000 NEW =CR----------TYPE:<CR>

END PASS # 1
END PASS # 2

8.8.10 After required run time has elapsed, terminate running of the diagnostic at the DPM50 console terminal by depressing the break key.

8.8.11 Load and run diagnostics for any additional LSI option modules installed, using same method used to run the CPU tests.

8.8.12 after all LSI modules have been run, if any D BUS I/O modules exist within the DPM50 subsystem, load diagnostic VPCAE0 and follow procedure P00-00C0A-00-0000WM-06-8055. Reference section 4.0 DIAGNOSTIC TESTING.

TITLE MODULAR APPROACH TO SYSTEM TEST

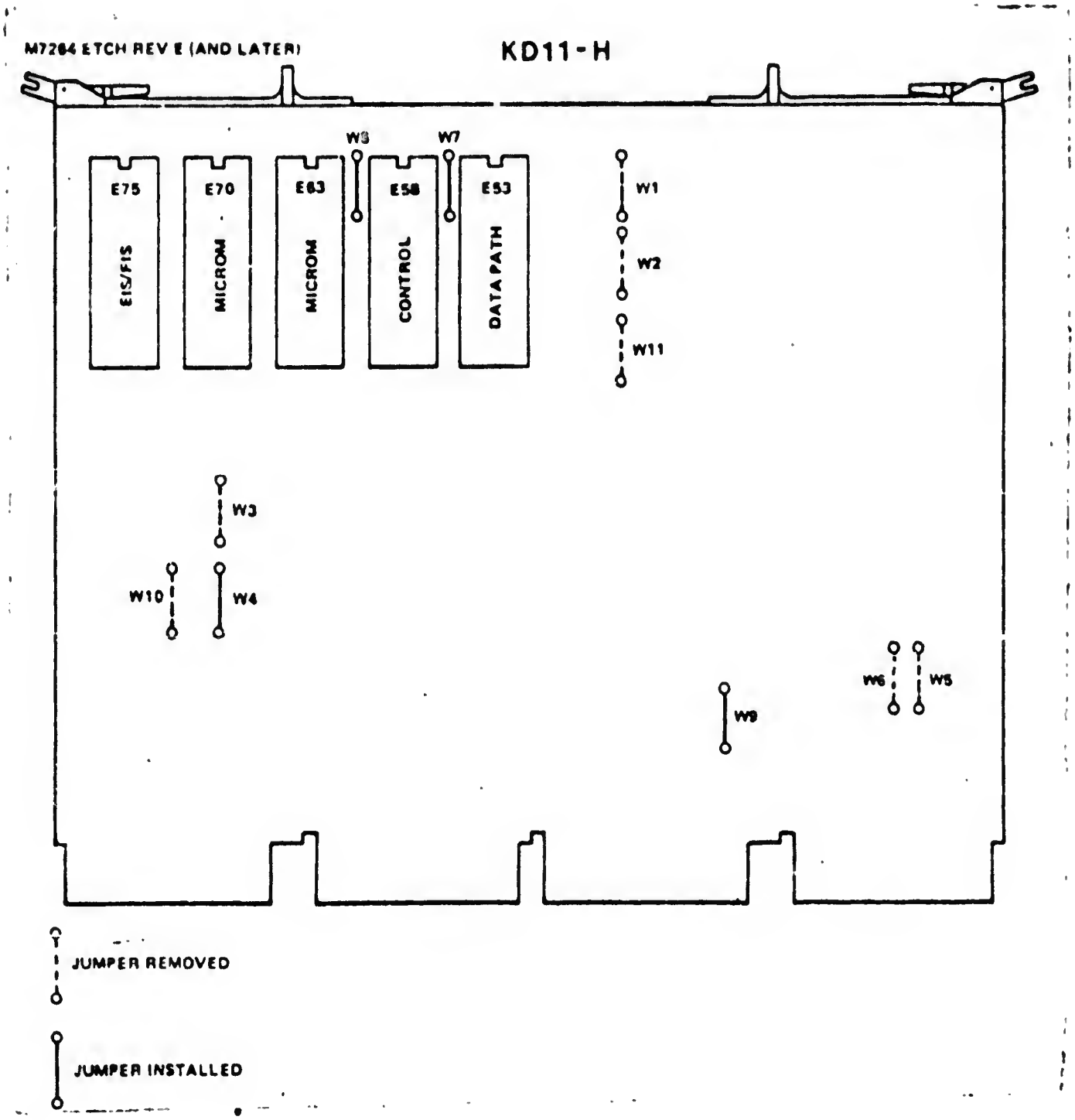
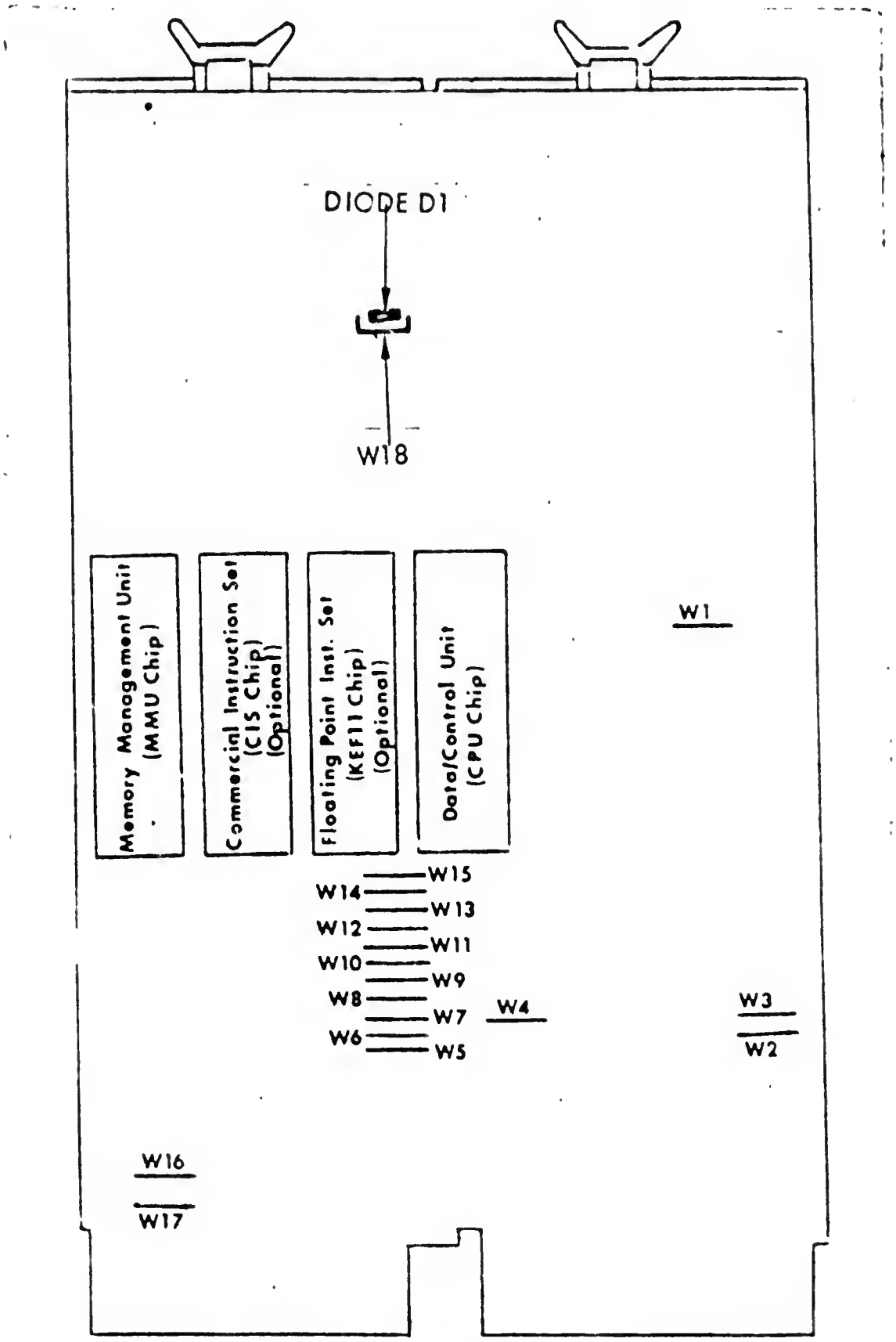


FIGURE 1

	SIZE	CODE	NUMBER	REV
	A	SP	MAA 6176-0-0	C



KDF11-AA

(M8186 DUAL SIZE MODULE)

FIGURE 2

	SIZE	CODE	NUMBER	REV
	A	SP	MAA 6176-0-0	C

TEV11 M9400-YB

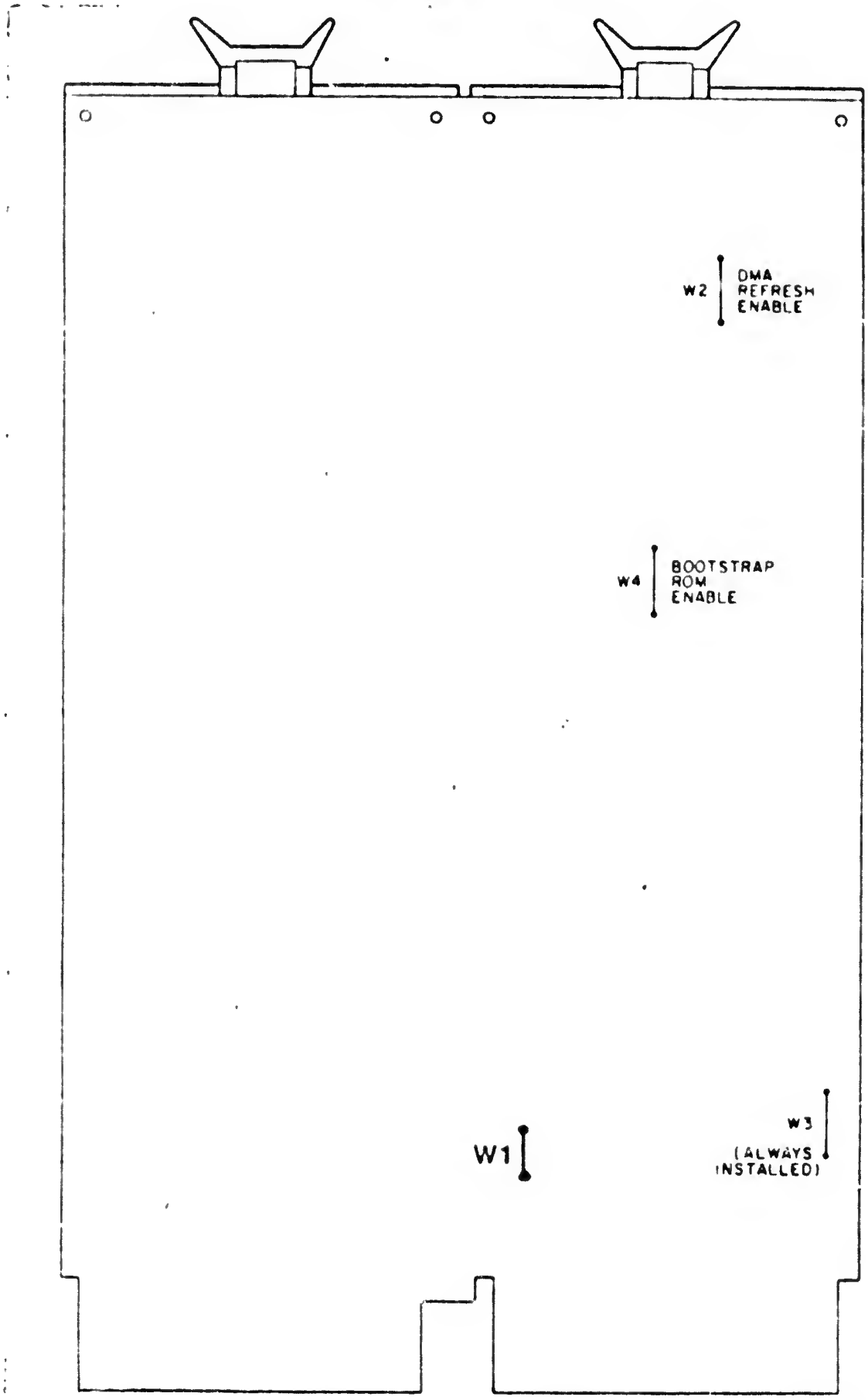


FIGURE 3

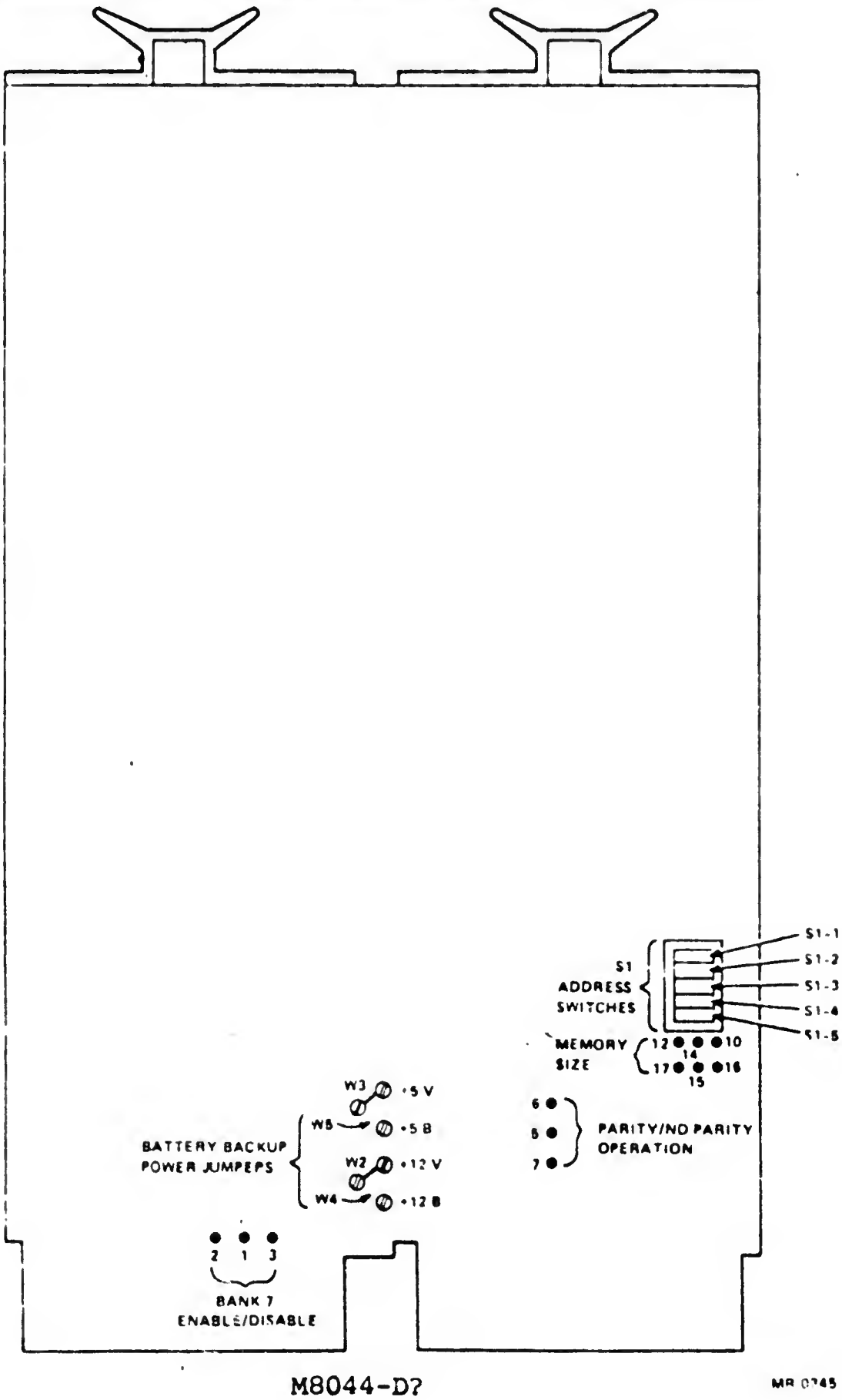


Figure 4 MSV11-D, MSV11-E Switch and Jumper Locations

	SIZE	CODE	NUMBER	REV
	A	SP	MAA 6176-0-0	C

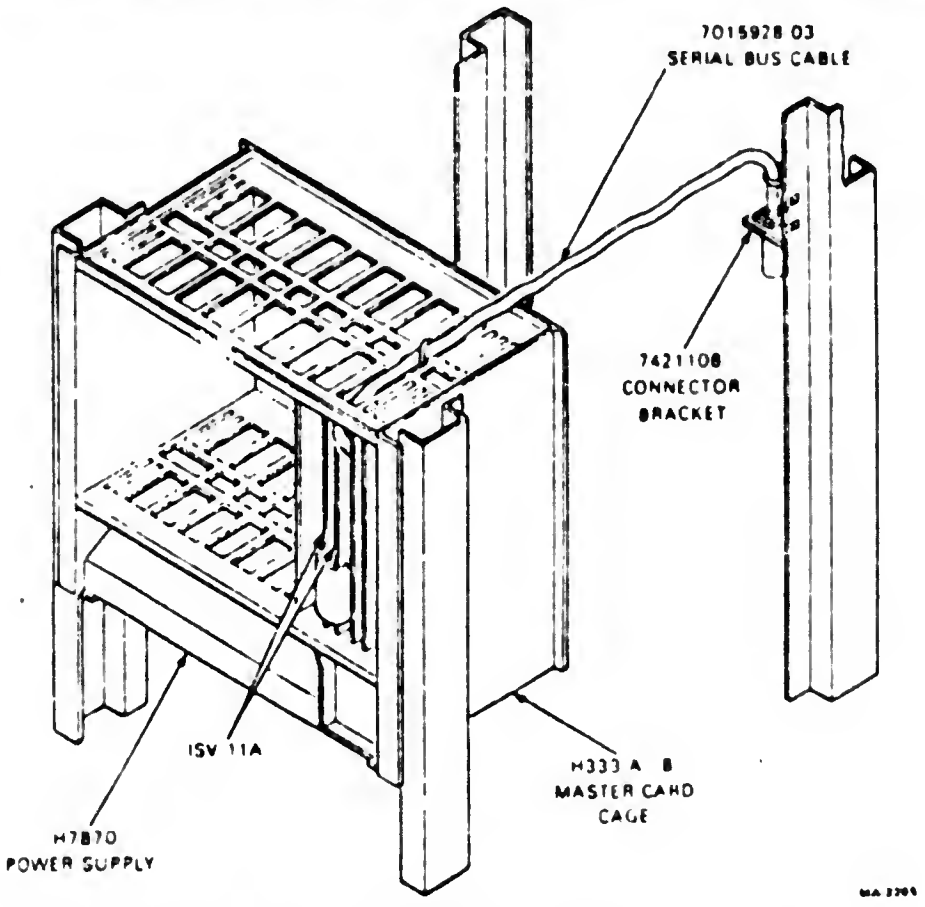


Figure 5 DECdataway Connector Mounting

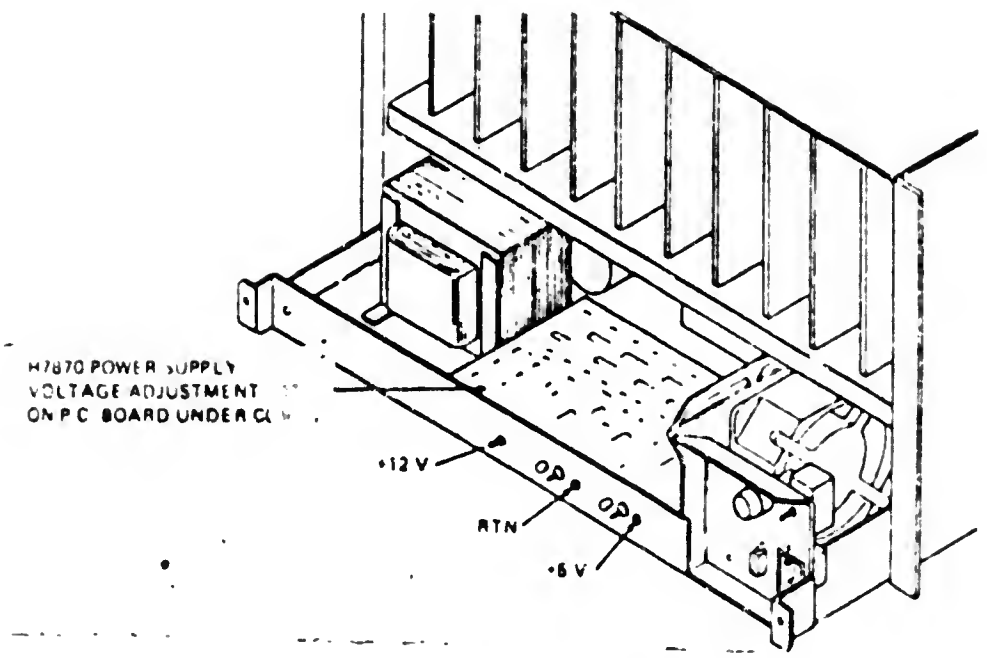


FIGURE 6

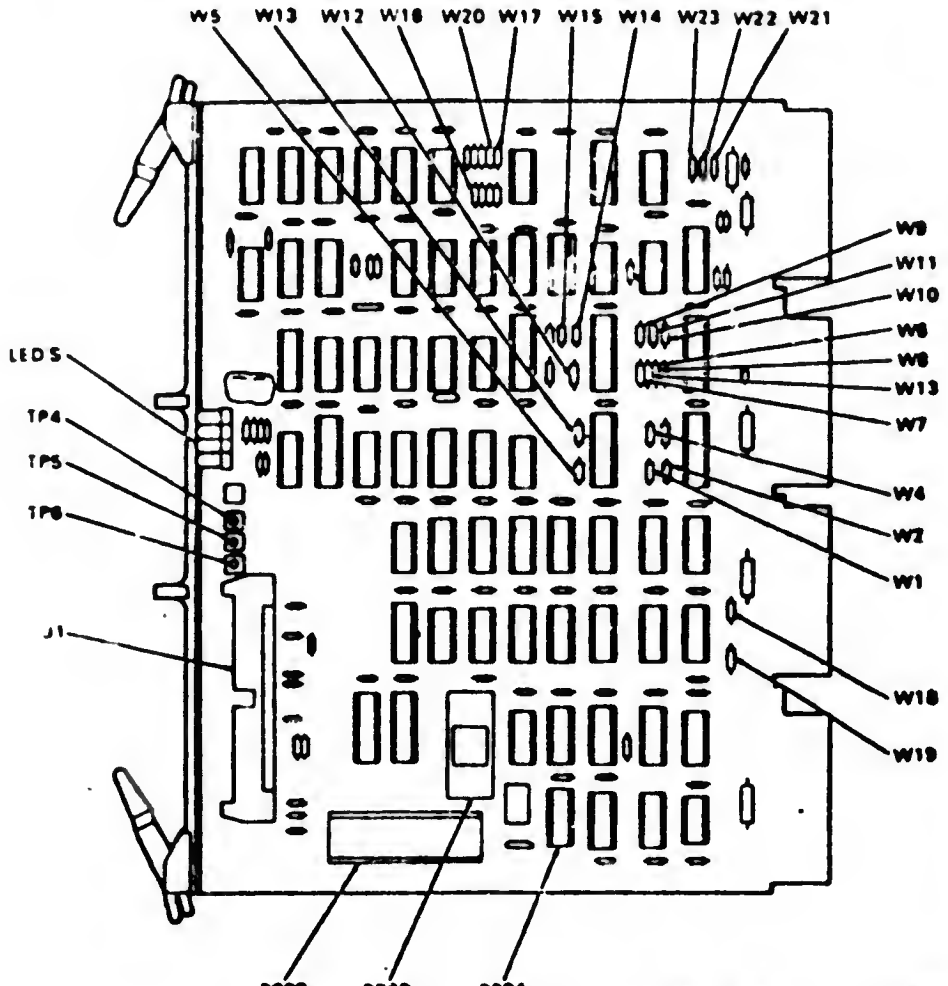


Figure 7-1 M8080 Board

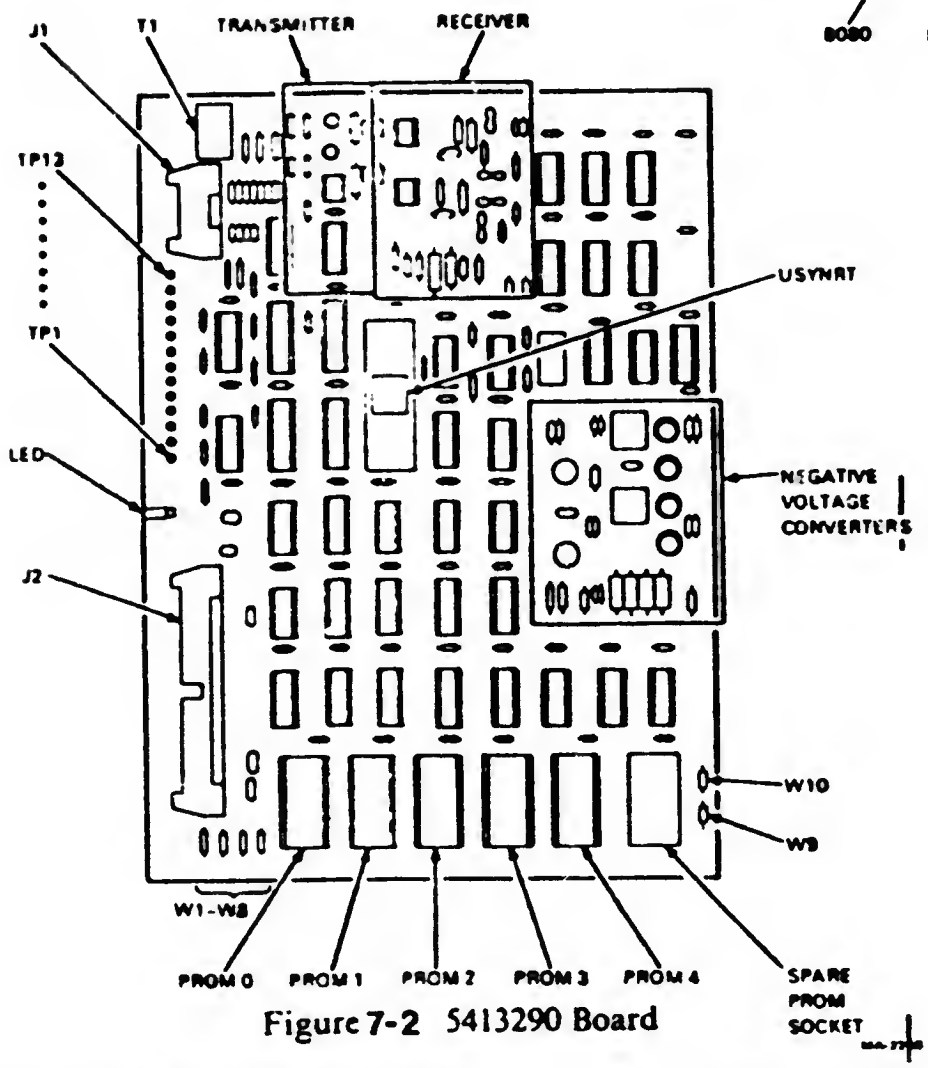


Figure 7-2 5413290 Board

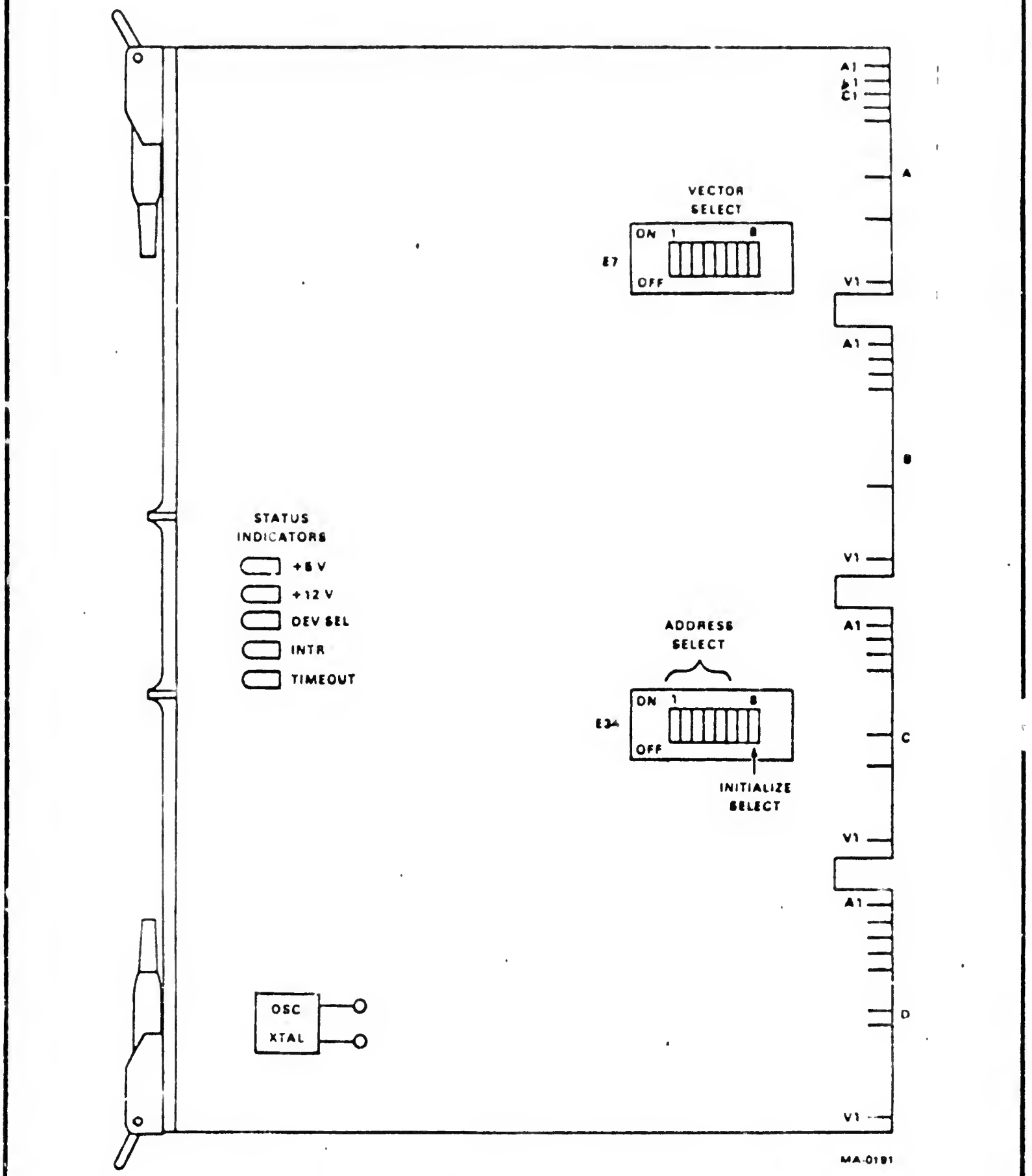


Figure 8 M7958 I/O Control Module

	SIZE	CODE	NUMBER	REV
	A	SP	MAA 6176-0-0	C

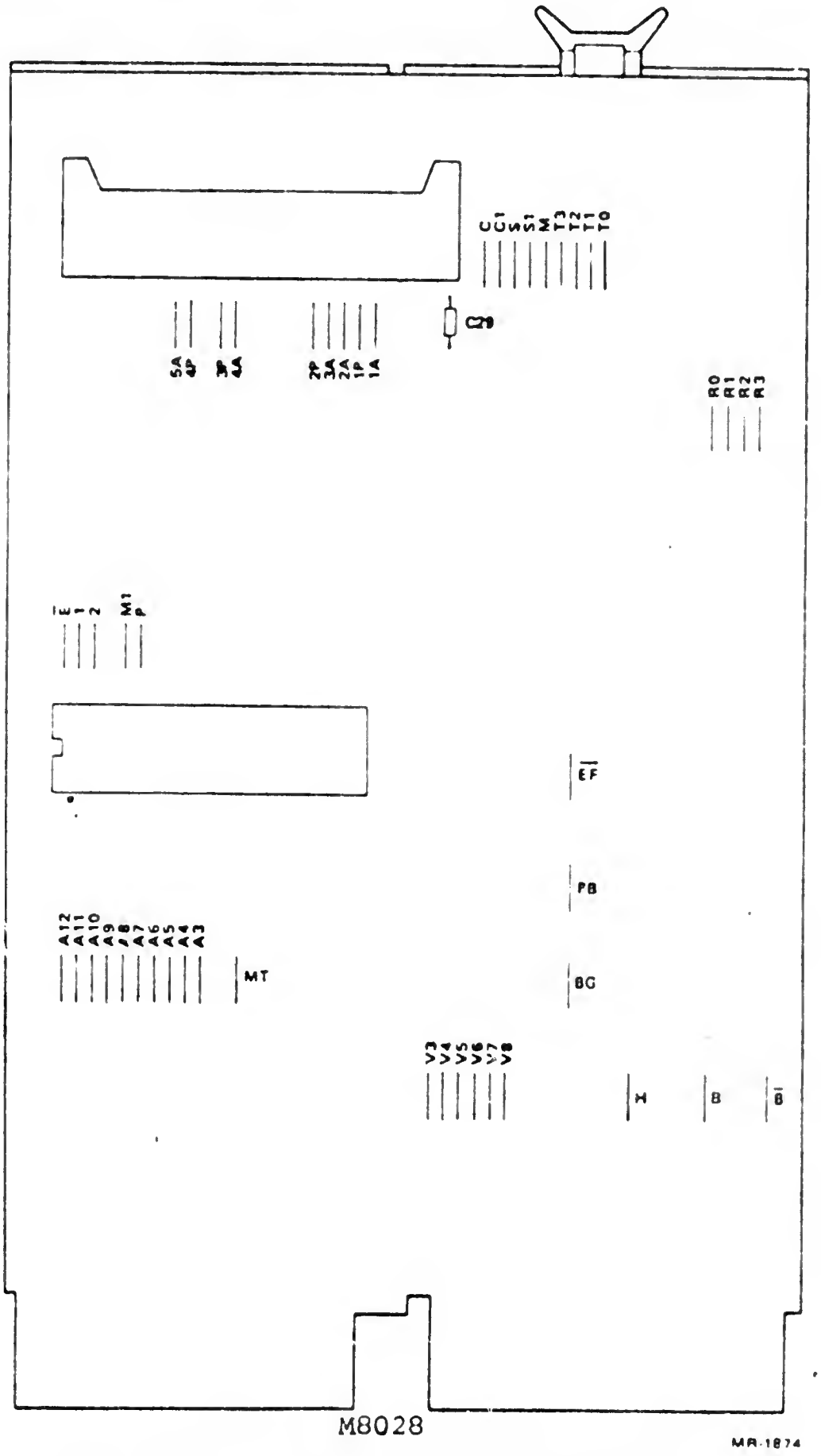
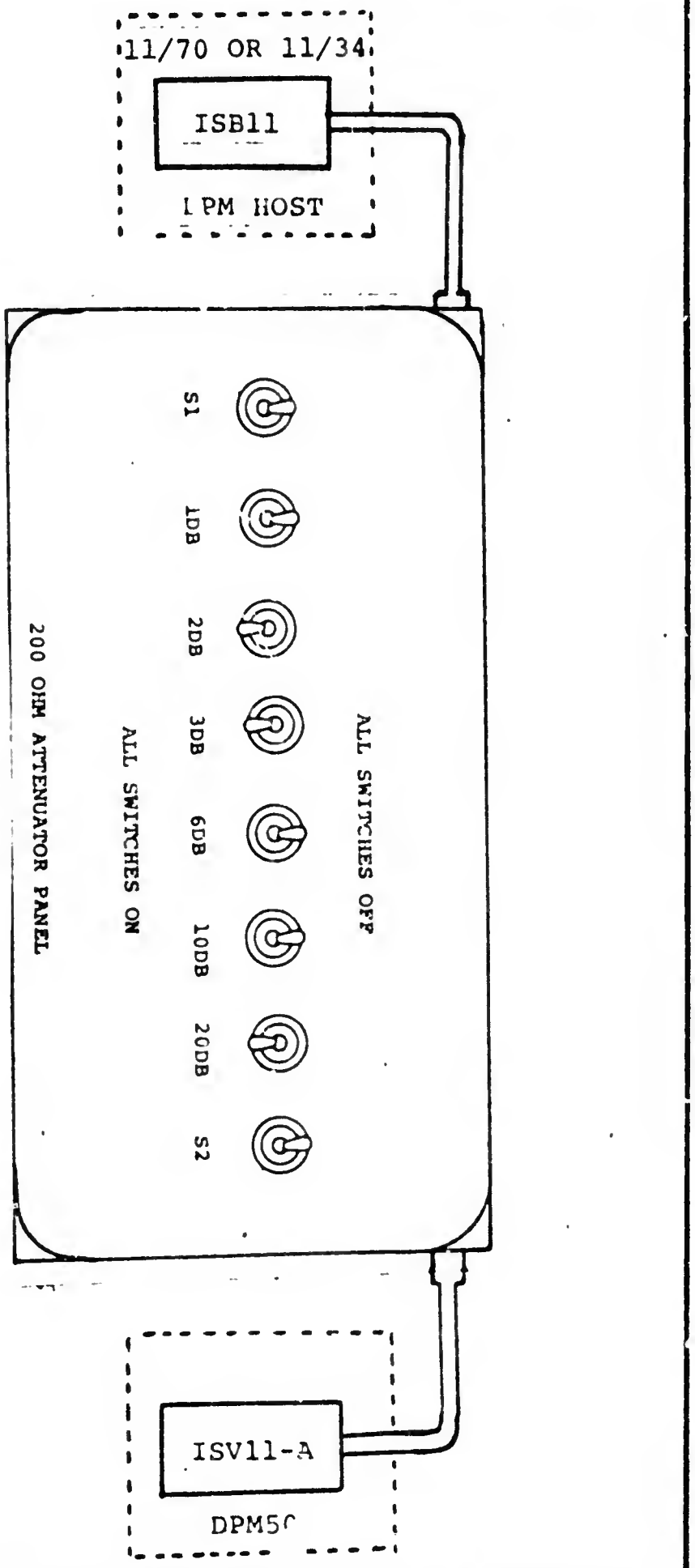


Figure 9 DLV11-F Jumper Locations



# OF TERMINALS	ATTENUATOR SETTING
1 TO 9	25DB
10 TO 19	24DB
20 TO 29	23DB
30 TO 39	22DB
40 TO 49	21DB
50 TO 59	20DB
60 TO 63	19DB

FIGURE 10

MONITOR INTERACTION AT LOCAL TERMINAL

Prompts		
	>	Operator may enter file name to call next diagnostic, or type control Z to put LSI-11 in ODT mode.
	@	If following 157776 after a file name has been entered, indicates the diagnostic is in the LSI-11 and the operator may communicate with it via ODT. If following "End pass" and the current PC, indicates the operator may give further instructions in ODT. Giving "760144" reestablishes communication with local monitor.
Inputs		
	File names	Used following ">" to call diagnostics
	200G	Not to monitor - starts diagnostic if LSI-11 is in ODT
	Break	Not to monitor - stops diagnostic.
	760144/	Reestablishes communication with local monitor if LSI-11 is in ODT
Deposit	2	Following "000000" tells monitor that operator wishes to run another diagnostic.
Deposit	1	Follow "000000" aborts monitor in host. This is the last input by the operator
	Control Z	Following ">" puts LSI-11 in ODT.
Outputs		
	157776	Following file name entry indicates the diagnostic has been downloaded
	NX	The requested file cannot be found.
	BDLD	The attempt to download the diagnostic was unsuccessful.
	END PASS	Diagnostic has completed a pass.
	Current PC	Following break indicates diagnostic has stopped at address printed
	000000	Following "760144" indicates operator may input further instructions to local monitor (1 or 2).
	EX .	Monitor has terminated at host.

FIGURE 11

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE ARII SYSTEM INSTALLATION AND ACCEPTANCE PROCEDURE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6180					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jekniewski	Tom Hall	A	SP	MAA6180-0-0	A

AR11 SYSTEM INSTALLATION AND ACCEPTANCE PROCEDURE

1.0 AR11 INSTALLATION/ACCEPTANCE

Refer to Document A-SP-AR11-0-4

1.1 Diagnostic Package

(A) AR11 Logic Test MainDEC-11-DZARA-A
(B) AR11 Analog Tests MainDEC-11-DZARB-A
(C) AR11 Wrap-Around Test MainDEC-11-DZARC-A

1.2 Error Diagnosis and Repair

Refer to Document A-SP-AR11-0-6

1.3 Other Related Documents

(A) AR11 Circuit Description A-SP-AR11-0-5
(B) AR11 Users Guide DEC-11-HARU6-B-D

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE NC 11-A GAMMA CAMERA INTERFACE Appendix A

REVISIONS

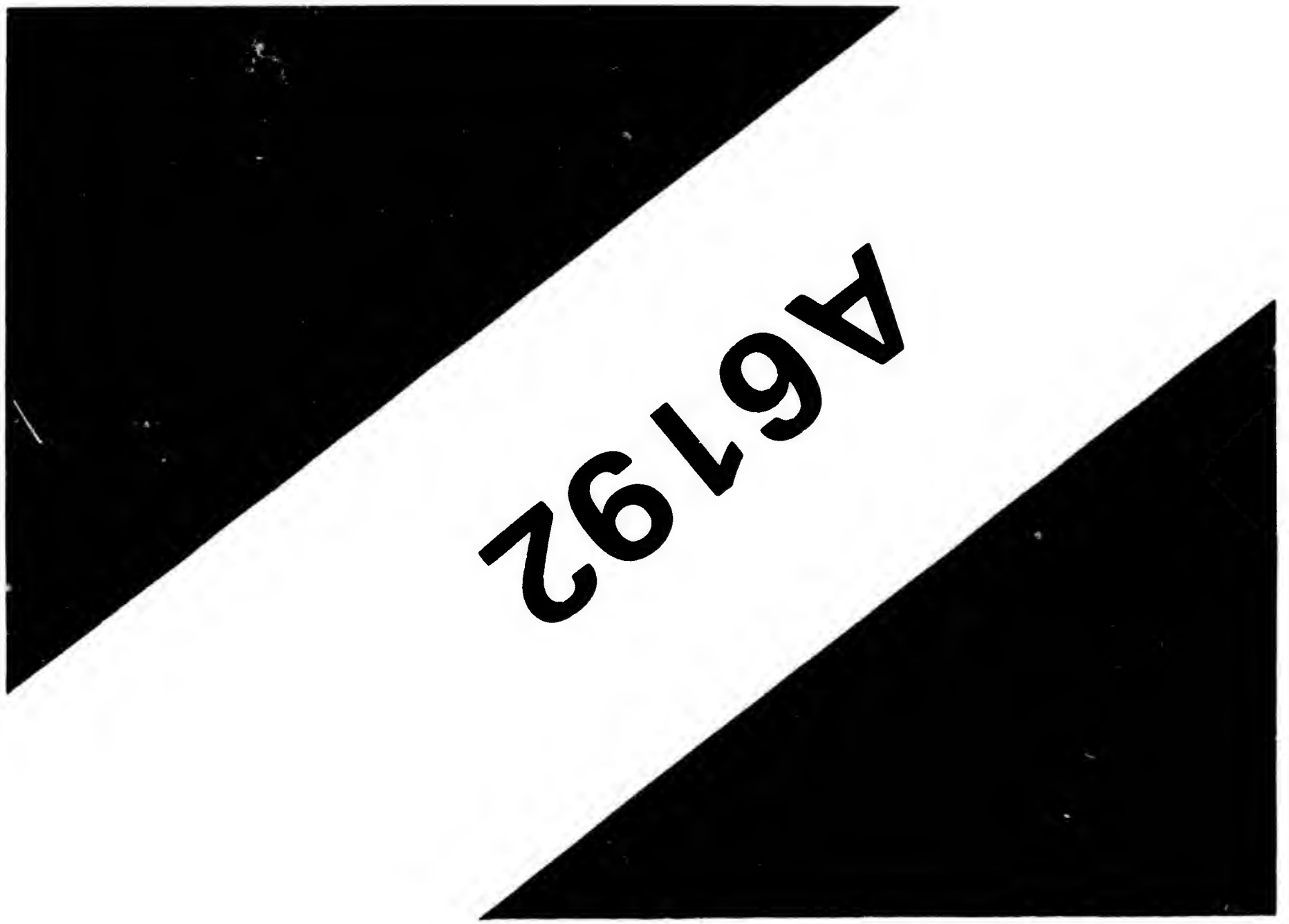
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6190					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelenkiewski		A	SP	MAA6190-0-0	A

NC 11-A GAMMA CAMERA INTERFACE

Ref. Adjustment Procedure A-SP-NC11-A-23

Checkout and Acceptance A-SP-NC11-A-22


A67192

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MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE NCV11 GAMMA CAMERA INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A						

ENG	APPD	SIZE	CODE	NUMBER	REV
Dwayne Herbert	Tom LeCouvet	A	SP	MAA6192-0-0	A

EN-01083-16-N672-(302)

NCV11 GAMMA CAMERA INTERFACE

1.0 INTRODUCTION:

The Gamma Camera is used to record the distribution of radioactive isotopes that are introduced into a patient under study and concentrated in the organ of interest. The output of the Gamma camera is processed by the NCV11 interface, loaded into a computer memory, and written on a mass storage device. The stored information may be called back and displayed at a later date.

2.0 REFERENCE DOCUMENTATION:

2.1 Reference Manual EK-NCV11-TM-???

2.2 Reference Parts List PL-NCV11

2.3 Checkout Procedure SP-NCV11-0-1?

2.4 Print Set MP00491

3.0 TEST EQUIPMENT:

3.1 Test philosophy will be to module swap and return for repair.

3.2 The Self Test connector (Part No. 70-12894) is the only special equipment required to run these tests. The connector is shipped with the NCV11 option. You may find it plugged into J1 on the AC17 module.

3.3 Add DVM - Voltmeter.

4.0 REQUIRED DIAGNOSTIC PROGRAMS:

4.1 DVNCA NCV11 Logic Test

4.2 DVNCA NCV11 Differential Linearity Test

5.0 SPECIAL INSTRUCTIONS:

None

6.0 INSTALLATION & TEST SET UP INSTRUCTIONS:

Unibus Based Systems - When making an add-on installation of the NCV11-B Interface Option to an existing Unibus-based system, proceed as follows:

6.1 Mount the DDV11-C backplane in the CPU or expander box in the same manner as a standard Unibus system mounting unit.

NOTE

Disks should normally be first on the Unibus to give them higher priority in DMA arbitration than that of the NCV11.

6.2 If it is necessary to provide an additional SPC slot for the M8217 Converter module, mount the DD11 backplane in the CPU or expansion box.

NOTE

Some old Unibus backplanes are incompatible with the M8217 module. If in doubt, check the DW11 Installation Manual.

6.3 Connect the backplane power harness(es) to the power distribution panel(s).

6.4 Install the M9401 module in slot AB01 of the DDV11-C backplane.

6.5 Install the M8217 in the Unibus backplane.

NOTE

When the M8217 module is mounted in a Unibus backplane, remove the NPG IN/NPG OUT jumper between pins CA1 and CB1 of the SPC slot to be used.

6.6 Connect the two BC05L cables between the M9401 and M8217 modules, J1 to J1, and J2 to J2 (colored stripe adjacent to pins UU/VV).

6.7 Install the NCV11 modules in the DDV11-C backplane in the sequence shown in Figure 2-1.

6.8 Install the M9400-YB module in slot AB02, direc'ly behind the M9401 module in the LSI-11 Bus backplane.

6.9 Install the H322 distribution panel.

6.10 Interconnect the NCV11 modules and the H322, shown in Figure 2-1.

7.0 POWER CHECKS:

7.1 Check BA11 box voltages. +5V ± 5%, +15V ± 5%, -15V ± 5%

8.0 DIAGNOSTIC TEST PROCEDURE:

"For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria; e.g. pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the CHECKLISTS."

8.1 NCV11 Logic Test (Checks the M8026 and M8036)

8.1.1 Load the MD-11-DVNCA program into memory.

8.1.2 Start the program at location 200. (Restart address is 204)

8.1.3 Type L (CR) to start the test

8.1.4 To terminate the test type CTRL/C.

8.2 NCV11 Differential Linearity Test (Checks the A017 and M8036)

8.2.1 Switch the Maintenance Switch (S1) on the A017 module to MAINTENANCE (toward the I/O connector).

8.2.2 Plug the Self Test Connector into J1 on the A017 module. Connect the red jumper wire on the connector to test point R (TPR) on the A017 module.

8.2.3 Load the MD-11-DVNCA program into memory.

8.2.4 Start the program at location 200.

8.2.5 Type D (CR) to start the test.

8.2.6 Type CTRL/C to terminate test.

8.3 NCV11 Final Acceptance Test (This test repeats the logic and differential linearity tests)

8.3.1 MD-11-DVNCA must be loaded into memory.

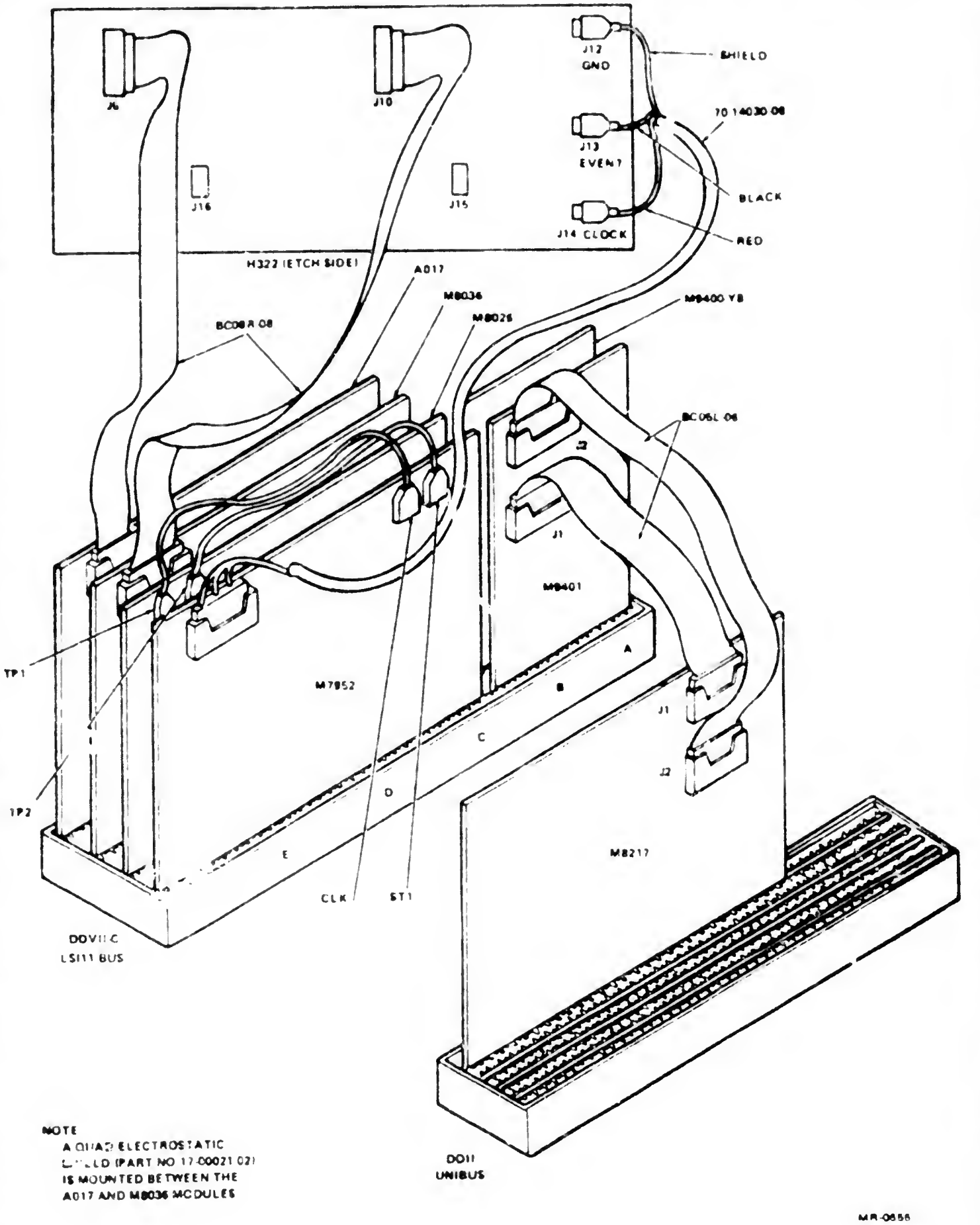
8.3.2 Make sure the Self Test Connector is plugged into connector J1 on the A017 module. The red jumper wire is connected to test point TPR on the A017, and switch S1 on the A017 module is switched to MAINTENANCE.

8.3.3 Type F (CR) to start the test

8.3.4 Type CTRL/C to terminate the test.

9.0 TEST PROCEDURE:

Reference 8.0



NOTE
A QUAD ELECTROSTATIC SHIELD (PART NO 17-00021-02) IS MOUNTED BETWEEN THE A017 AND M8036 MODULES

Figure 2-1 DW11-NCV11-H322 Interconnections (Unibus-Based System)

	SIZE	CODE	NUMBER	REV
	A	SP	MAA6192-0-0	A

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TITLE DR11-A GENERAL DEVICE INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6205					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekerace SEC	Tom	A	SP	MAA6205-0-0	A

DR11-A GENERAL DEVICE INTERFACE

REFERENCE DOCUMENTS

DR11-A Engineering Drawings, Print Set.

MAST Phase I Check-Off List.

Workmanship Manual, DEC.

Finish and Color Standard, DEC STD 092.

REQUIRED TEST EQUIPMENT

PDP-11 System with input device.

M980 Maintenance Module.

Digital Voltmeter, Fluke Model 465 or equivalent.

REQUIRED TEST SOFTWARE

MAINDEC-11-D8LA Diagnostic Write-up, DR11A Device Register Test.

MAINDEC-11-D8LA Diagnostic Tape.

CHECKOUT INSPECTION

Following Receipt of the test item(s), perform a brief (quick scan) visual inspection for obviou discrepancies per the DEC Workmanship Manual and DEC STD 092.

TEST SET-UP

Set-up the test item(s), with all power off, in the configuration shown in Figure 1. Note that the test item has a floating vector. Check that it has the proper jumper configuration.

VOLTAGE CHECKOUT

Power up the system to check the +5VDC at each SPC slot containing a test plan. Use the digital voltmeter to measure the voltage between pins A2 (+5VDC and C2 (GND) at each applicable SPC slot on backplane. The voltage shall be 5.00 VDC ±0.25 VDC. Note that the H744 Regulator has a +5 VDC voltage adjust potentiometer.

11 SYSTEMS CHECKOUT TEST PROCEDURE

Perform the checkout test in the sequence detailed in this section. Program starting address, switch settings and operator action are contained herein. However, refer to the Diagnostic Write-Up, MAINDEC-11-DL8A, for more detailed information, should the need arise.

DEVICE REGISTER TEST

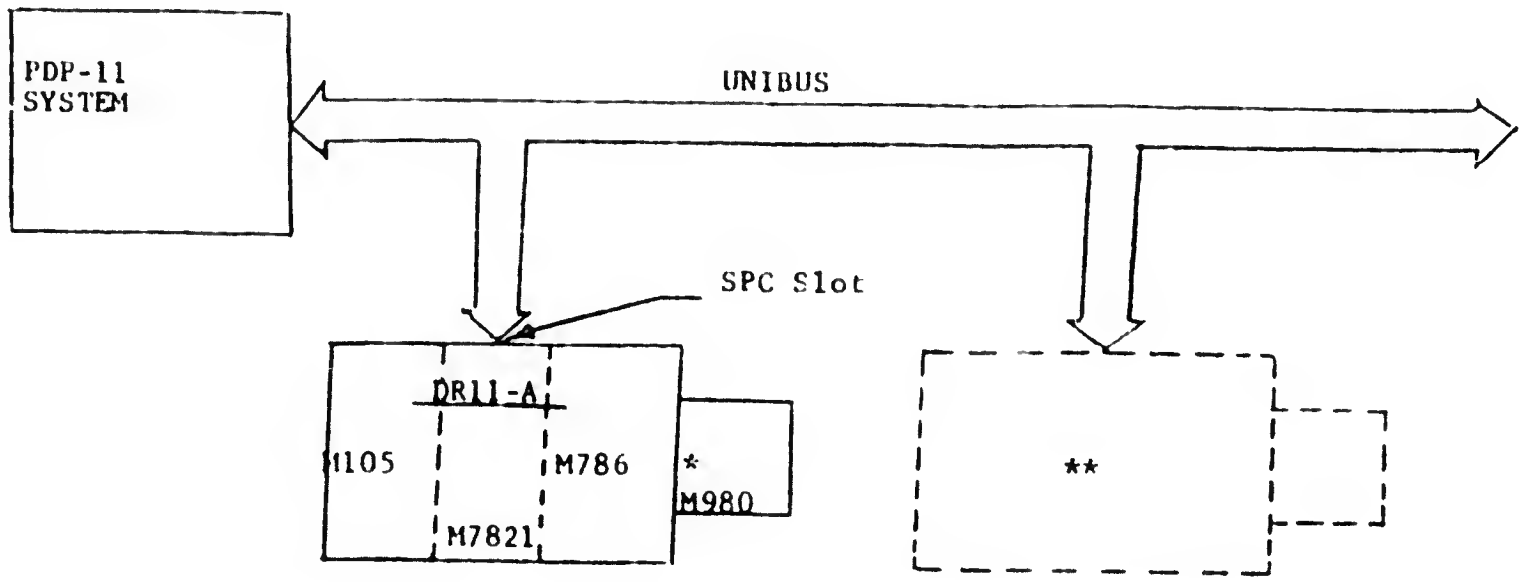
Load starting address 200.

Start program with all control switches down (zero).

Allow test to run for 15 minutes. Note that bell will ring at completion of each pass.

No errors allowed.

For restart after fix, repeat 7.1.1 and 7.1.2.



Notes:

* An M980 Special Maintenance Module must be connected to each DR11-A at the M786 dual connectors.

** A maximum total of 32 sequential DR11-A's may be connected for test.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DR11-B DIRECT MEMORY (DMA) INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6210					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM SEKANIEWSKI	TOM	A	SP	MAA6210-0-0	A

DR11-B DIRECT MEMORY (DMA) INTERFACE

REFERENCE DOCUMENTS

DR11-B Engineering Drawings, Print Set.

MAST Phase I Check-Off List.

Workmanship Manual, DEC.

Finish and Color Standard, DEC STD 092.

DR11-B Manual, DEC-11-HDRC-D.

REQUIRED TEST EQUIPMENT

PDP-11 System with input device.

Digital Voltmeter, Fluke Model 465 or equivalent.

REQUIRED TEST SOFTWARE

MAINDEC-11 DZDRB Diagnostic Write-up, DR11B PDP11 General NPR Interface.

MAINDEC-11-DZDRB Diagnostic Tape.

CHECKOUT INSPECTION

Following Receipt of the test item, perform a brief (quick scan) visual inspection for obvious discrepancies per the DEC Workmanship Manual and DEC STD 092.

TEST SET-UP

Set-up the test item, with all power off, in the configuration shown in Figure 1. Remove modules from slots CD4. Then transfer the Test Board from Slots AB2 to Slots CD4.

VOLTAGE CHECKOUT

Power up the system to check the +5VDC at the test item backplane. Use the digital voltmeter to measure the voltage between pins A2 (+5 FDC) and C2 (GND) on the backplane. The voltage shall be 5.00 VDC $\pm$ 0.25 VDC. Note that the H744 Regulator has a +5 VDC voltage adjust potentiometer.

11 SYSTEMS CHECKOUT TEST PROCEDURE

Perform the checkout test in the sequence detailed in this section. Program starting address, switch settings and operator action are contained herein. However, refer to the Diagnostic Write-Up, MAINDEC-11-DZDRB, for more detailed information, should the need arise.

DEVICE REGISTER TEST

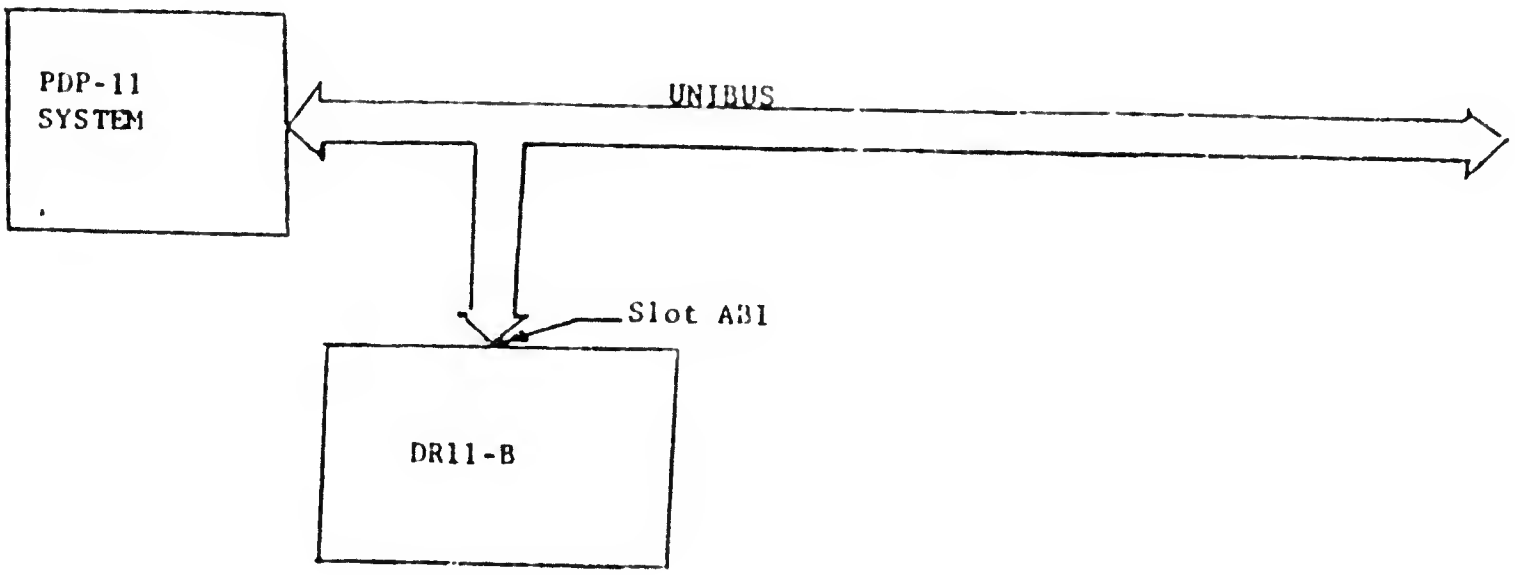
Load starting address 200.

Start program with all control switches down (zero).

Allow test to run for 30 minutes.

No errors allowed.

For restart after fix, repeat first two steps of this section.



FUNCTIONAL TEST CONFIGURATION

FIGURE 1

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DR11-C GENERAL DEVICE INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6220					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jedrzejewski	Frank	A	SP	MAA0220-0-0	A

DR11-C GENERAL DEVICE INTERFACE

REFERENCE DOCUMENTS

DR11-C Engineering Drawings, Print Set.

MAST Phase I Check-Off List.

Workmanship Manual, DEC.

Finish and Color Standard, DEC STD 092.

DR11-C General Device Interface Manual, DEC-11-HRDCA-D-D.

REQUIRED TEST EQUIPMENT

PDP-11 System with input device.

BCØ8R Maintenance Cable.

Digital Voltmeter, Fluke Model 465 or equivalent.

REQUIRED TEST SOFTWARE

MAINDEC-11 DZDRC Diagnostic Write-up, DR11C Device Register Test.

MAINDEC-11-DZDRC Diagnostic Tape.

CHECKOUT PROCEDURE

Following Receipt of the test item(s), perform a brief (quick scan) visual inspection for obvious discrepancies per the DEC Workmanship Manual and DEC STD 092.

TEST SET-UP

Set-up the test item(s), with all power off. in the configuration shown in Figure 1. Note that the test item has a floating vector. Check that it has the proper jumper configuration.

VOLTAGE CHECKOUT

Power up the system to check the +5VDC at each SPC slot containing a test item. Use the digital voltmeter to measure the voltage between pins A2 (+5 VDC) and C2 (GND) at each applicable SPC slot on backplane. The voltage shall be 5.00 VDC $\pm$ 0.25 VDC.

11 SYSTEMS CHECKOUT TEST PROCEDURE

Perform the checkout test in the sequence detailed in this section. Program starting address, switch settings and operator action are contained herein. However, refer to the Diagnostic Write-Up, MAINDEC-11-DZDRC, for more detailed information, should the need arise.

DEVICE REGISTER TEST

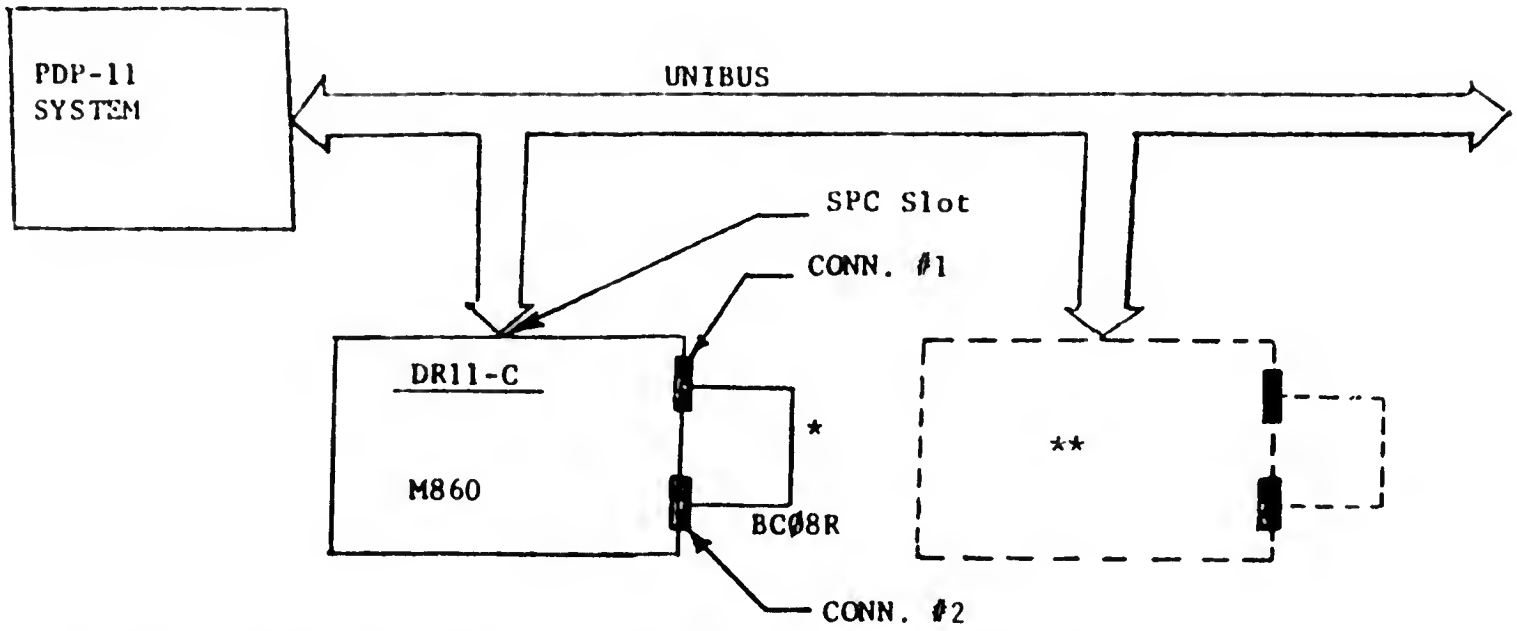
Load starting address 200.

Start program with all control switches down (zero).

Allow test to run for one pass. Note that at completion of each pass, of each test item, an * will be printed.

No errors allowed.

For restart after fix, repeat first two steps of this sect[illegible]



Notes: *A BCØ8R Special Maintenance Cable must be connected to each DR11-C at the M860 dual connectors.

**A maximum total of 32 sequential DR11-C's may be connected for test.

FUNCTIONAL TEST CONFIGURATION

FIGURE 1

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DRV11 16 IT PARALLEL LINE UNIT FOR PDP 11/03 Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6225					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Jelenipewski		A	SP	MAA0225-0-0	A

EN-01293-16-N678-(DP8)

DRV11 16 BIT PARALLEL LINE UNIT FOR PDP -11/Ø3

1.0 INTRODUCTION

The intent of this procedure is to summarize the diagnostic writeups. For the purpose of expediency, the procedure has been kept brief, and to the point, to keep from confusing the user. For additional information, it will be necesaary to refer to the diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Workmanship Manual (STD 116)

2.2 DRV11 Engineering Specification A-SP-DRV11

2.3 LSI11 PDP 11/Ø3 User's Manual EK LSI11-TM-ØØ1

2.4 DRV11 Printset

2.5 ADV11-A, KWV11-A, AAV11-A, DRV11-A, User's Manual EK-ADV11-OP-ØØ1

2.6 LSI11 PDP 11/Ø3 Configuration and Installation Guide EK-LSI11-IN-ØØ1

3.0 REQUIRED TEST EQUIPMENT

3.1 LSI11 Standard Computer

3.2 DRV11 Module

3.3 BCØ8R-1 Test Cable

3.4 Output terminal/DLV11

4.0 REQUIRED TEST SOFTWARE

4.1 MAINDEC 11-DVKAF DRV11 Test Diagnostic and Write up

4.2 MAINDEC 11-DXDRC DEC/X11 Exerciser and Write up

5.0 SPECIAL INSPECTIONS AND CHECKS

5.1 If part of DEC LAB Ø3 System variation H or J, module will have 2 BCØ42-15 cables plugged into J1 and J2 for communication with the outside world.

6.0 TEST SET UP

6.1 Insure that jumpers A3 thru A11 are removed and jumper A12 is inserted for a device address of 167770.

6.2 Insure that vector jumpers V3, V4, and V5 are installed and vector jumpers V6 and V7 are removed for a vector of 300.

6.3 Install BC08R-1 Test Cable into Berg connectors J1 and J2.

7.0 11 SYSTEM INTEGRATION TEST PROCEDURE

7.1 DRV11 Test (DVKAF)

7.1.1 Load program through appropriate load media

7.1.2 Program starting address

7.1.2.1 Load address 200
7.1.2.2 Start 000000 software SR default value

7.1.3 Alternate software SR settings (loc 122)

7.1.3.1 SWR15 = 1 Continue on error
7.1.3.2 SWR14 = 1 Loop on current error
7.1.3.3 SWR10 = 1 Loop on current test
7.1.3.4 SWR 9 = 1 Run test module

7.1.4 Operator Action

7.1.4.1 Type 200G

7.1.5 Evidence of End of Pass and Runtime

7.1.5.1 "END OF PASS" will be typed every 10 seconds.

7.1.6 Acceptable Errors: None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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 12/11/81

TITLE MAST BACKUP PROCEDURE FOR DRV11-J PARALLEL INTERFACE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
*	PRELIMINARY		A. RICHARD	12/11/81	BOB BECK	
A	ORIGINAL	ML016	A. RICHARD			3/11/82

ENG	APPD	SIZE	CODE	NUMBER	REV
ART RICHARD	BOB BECK	A	SP	MA-A6227-0-0	A

TITLE MAST BACKUP PROCEDURE FOR DRV11-J PARALLEL INTERFACE

TABLE OF CONTENTS

DRV11-J (M8049) PARALLEL INTERFACE

1.0 SCOPE:

1.1 The DRV11-J is a double-height parallel line interface module designed for use in LSI-11 microcomputer systems. It contains four programable ports designated A, B, C, and D. Each port contains 16 I/O lines and is capable of transferring a 16-bit word between the LSI-11 bus and the user device(s).

1.2 This procedure establishes the minimum test and electrical standards that a DRV11-J must meet to be considered acceptable for customer shipment.

2.0 RESPONSIBILITY:

2.1 It is the responsibility of the originator to maintain this document. Changes should be requested through the originator if possible, or his/her group (if originator is no longer available), or through MAST Administration in Salem (NI).

3.0 REFERENCE DOCUMENTATION:

3.1 Manuals & Engineering Specifications:

3.1.1 DRV11-J Engineering Specification	SP-DRV11-J-2
3.1.2 DRV11-J Parallel Interface User's Guide	EK-DRV1J-UG

3.2 Prints and Schematics:

3.2.1 DRV11-J Field Maintenance Print Set	MP00866

4.0 REQUIRED TEST EQUIPMENT:

4.1 Hardware & Media:

4.1.1 LSI CPU with a console device (LA36 or equivalent).

4.1.2 At least 16K words of memory.

4.1.3 Digital voltmeter accurate to .01V @ 15V.

5.0 REQUIRED DIAGNOSTIC PROGRAMS:

5.1 CVDRC DRV11-J Diagnostic Part 1

5.2 CVDRD DRV11-J Diagnostic Part 2

6.0 SPECIAL INSTRUCTIONS:

6.1 None.

7.0 INSTALLATION & TEST SET-UP INSTRUCTIONS:

7.1 Module Jumper Configurations:

7.1.1 Jumpers W10 and W11 must be in.

Note: Refer to DRV11-J Parallel Interface User's Guide, EK-DRV1J-UG, for further information.

7.1.2 Three standard device addresses have been assigned for use with DRV11-Js. The DRV11-J module, M8049, is configured at the factory for an address of 764160. If more than one DRV11-J is used in a system, the modules are configured as follows:

1st DRV11-J address = 764160
2nd DRV11-J address = 764140
3rd DRV11-J address = 764120

Reference Table A located and Figure 1 for appropriate jumper configuration.

7.1.3 If the system application requires more than three DRV11-Js, addresses for the additional modules must be selected from the user-reserved area of the address map and assigned in descending order in a modulus of 20 (octal). When selecting addresses other than the three standard addresses, refer to the current issue of the "Microcomputer Interfaces Handbook" to avoid possible I/O device address conflicts.

7.1.4 The DRV11-J interrupt vector addresses are to be programmed into a RAM (vector address memory) and cannot be jumper or switch selected.

7.2 Loopback Cable Installation:

7.2.1 The loopback cable BC05W-02 is installed with a half twist connecting J1-1 to J2-50. This cable must be in for test purposes.

TABLE A

Address Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Jumper				W1	W2	W3	W4	W5	W6	W7	W8	W9				
Device Address																
764160					X					X	X	X				
764140					X					X	X					
764120					X					X		X				

X = Jumper in for a logical 1. All other jumpers out.

8.0 POWER CHECKS:

8.1 The following voltages must be present and within tolerance on the backplane containing the DRV11-J:

VOLTAGE	TOLERANCE	MEASURED AT
+5VDC	+4.75 VDC to +5.25 VDC	AA2

9.0 DIAGNOSTIC TEST PROCEDURE:

For the specific sequence of diagnostics to be run in any particular situation, and for current MAST minimum test criteria (e.g. pass-counts, etc.), refer to the appropriate MAST CHECKLIST. The following is a list of step-by-step instructions for executing each individual diagnostic contained in the CHECKLIST. No errors are allowed.

9.1 Run the DRV11-J Diagnostic Test Part 1, CVDRC:

9.1.1 The starting location is 200 and the switch register should = 000000.

9.1.2 This diagnostic does not "auto-size" the number of DRV11-Js connected. If more than one DRV11-J is to be tested, the user must set up "DEVM" address location 1246 for the diagnostic to sequentially test up to four DRV11-Js. If only one DRV11-J is to be tested, modification to this address location is not necessary.

Set address location 1246 to = 3 if two DRV11-Js.
Set address location 1246 to = 7 if three DRV11-Js.
Set address location 1246 to = 17 if four DRV11-Js.

1st DRV11-J = address 764160
2nd DRV11-J = address 764140
3rd DRV11-J = address 764120
4th DRV11-J = address 764100

```
CVDRCA DRV11J DIAG TEST PART 1

DRV11J CABLE REQ'D

SWR = 000000  NEW = <CR>

END PASS
```

9.2 Run the DRV11-J Diagnostic Test Part 2, CVDRD:

9.2.1 The starting location is 200 and the switch register should = 000000.

9.2.2 This diagnostic does not "auto-size" the number of DRV11-Js connected. If more than one DRV11-J is to be tested, the user must set up "DEVM" address location 2246 for the diagnostic to sequentially test up to four DRV11-Js. If only one DRV11-J is to be tested, modification to this address location is not necessary.

Set address location 2246 to = 3 if two DRV11-Js.
Set address location 2246 to = 7 if three DRV11-Js.
Set address location 2246 to = 17 if four DRV11-Js.

1st DRV11-J = address 764160
2nd DRV11-J = address 764140
3rd DRV11-J = address 764120
4th DRV11-J = address 764100

```
CVDRDA DRV11J DIAG TEST PART 2

DRV11J CABLE REQ'D

SWR = 000000  NEW = <CR>

END PASS
```

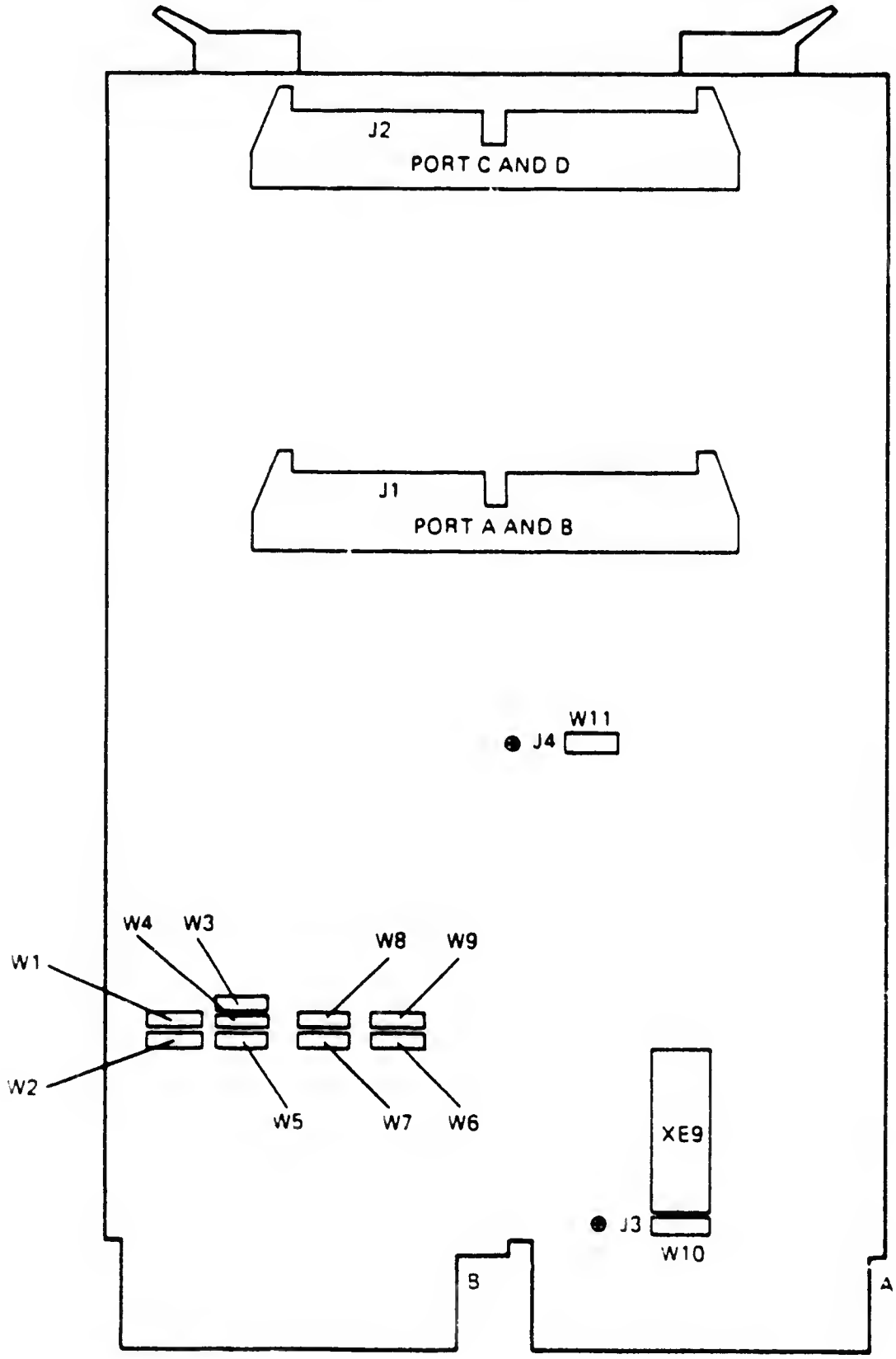

Figure 1 DRV11-J M8049

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MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DT03 - FM - FP Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6230					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jeremiewski		A	SP	MAA6230-0-0	A

EN-01083-16-N672-(392)

DT03 - FM - FP

SPECIAL INSTRUCTIONS

Before powering up DT03-FM/FP read the option description thoroughly.

The DT03-FM/FP Power Supply, and all shared bus ("C" Bus) devices power source must be on non-switched power from the 861-Power Controller, or from some other unswitched power source.

TEST EQUIPMENT

Two (2) PDP-11 processors
Unibus tester, or a I/O device that can be shared by both PDP-11 CPU's.
For further information refer to option description.

REFERENCE DOCUMENTATION

Manuals:	CSS-MO-F-1[illegible]-19 Option Description
Checkout Procedures:	Reference Option Description Page 2.3 Section 2.5 thru 2.6
Acceptance Procedures:	Reference Option Description Page A-2 Section A.5 thru A.7
Engineering Specs:	Reference Option Description Page 1-3 Section 1.6
Prints:	DT03-F
MAINDEC Listings:	DEC SPEC-11-ATV-ADC ABS MU1:T:TY Processer Diag. DEC SPEC-11-AXAAXC DAS Must be used with slavc module DATS DEC SPEC-11-AXJAXB DAS DT03FR Controller Module (Single Device) DEC SPEC-11-AXTAXA DAS DT03FR Controller Module (Multiple Device) DEC SPEC-11-AXASXA SRC DTAS Slavc Module for DTAC

A6240

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DA11-BD Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6240					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jeknifewski		A	SP	MAA6240-0-0	A

DA11-BD

SPECIAL INSTRUCTIONS

Reference option description page 2-1, section 2.1 for site considerations, and section 2.2 for cabling.

For further information, read the option documentation.

TEST EQUIPMENT

Two (2) PDP-11 processors

For further information refer to the option description, and the DR11-B Manual.

REFERENCE DOCUMENTATION

Manuals:	CSS-MO-F-10.4-19A
Checkout Procedures:	Page 2.2, section 2.4.1
Acceptance Procedures:	Reference Diagnostic Listing page 7, section twelve (12)
Engineering Specs:	Page 1, section 1.3
Prints:	Reference DR11-B-DA11-B
MAINDEC Listings:	DEC SPEC-11-DZDRB-C-D HBS DEC SPEC-11-AWYAX8 OBJ. (DEC X11)

A6260

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE DR11-K GENERAL DIGITAL I/O INTERFACE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-6260					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jeleniewski		A	SP	MAA6260-0-0	A

DR11-K GENERAL DIGITAL I/O INTERFACE

REFERENCE DOCUMENTS

DR11-K Engineering Drawings, Print Set.

MAST Phase I Check-Off List.

Workmanship Manual, DEC.

Finish and Color Standard, DEC STD 092.

DR11-K Interface User's Guide and Maintenance Manual, EK-DR11K-MM-001.

REQUIRED TEST EQUIPMENT

PDP-11 System with input device.

DD11-A or DD11-B.

BC08-R-1, one foot long Maintenance Cable.

Digital Voltmeter, Fluke Model 465 or equivalent.

REQUIRED TEST SOFTWARE

MAINDEC-11-DZDRG Diagnostic Write-up, DR11-K Digital I/O Test.

MAINDEC-11-DZDRG Diagnostic Tape.

CHECKOUT INSPECTION

Following Receipt of the test item(s), perform a brief (quick scan) visual inspection for obvious discrepancies per the DEC Workmanship Manual and DEC STD 092.

TEST SET-UP

Set-up the test item(s), with all power off, in the configuration shown in Figure 1. Note that the test item has a floating vector. Check that it has the proper "factory" jumper configuration and M7843 Interrupt Enable switch positions per Chapter 5 of the Maintenance Manual, EK-DR11K-MM-001.

VOLTAGE CHECKOUT

Power up the system to check the +5VDC at each SPC slot containing a test item. Use the digital voltmeter to measure the voltage between pins A2 (+5 VDC) and C2 (GND) at each applicable SPC slot on backplane. The voltage shall be 5.00 VDC ± 0.25 VDC. Note that the M744 Regulator has a +5 VDC voltage adjust potentiometer.

11 SYSTEMS CHECKOUT TEST PROCEDURE

Jumper W21, W22 and W23 in the A position.

Perform the checkout test in the sequence detailed in this section.

Program starting address, switch settings and operator action are contained herein. However, refer to the Diagnostic Write-Up, MAINDEC-11-DCLAG, for more detailed information, should the need arise.

LOGIC TEST

1. Load starting address 200.

2. Set all the M7843 Module INTERRUPT ENABLE switches on.

3. Start program with all control switches down (zero).

4. Allow test to run for five minutes.

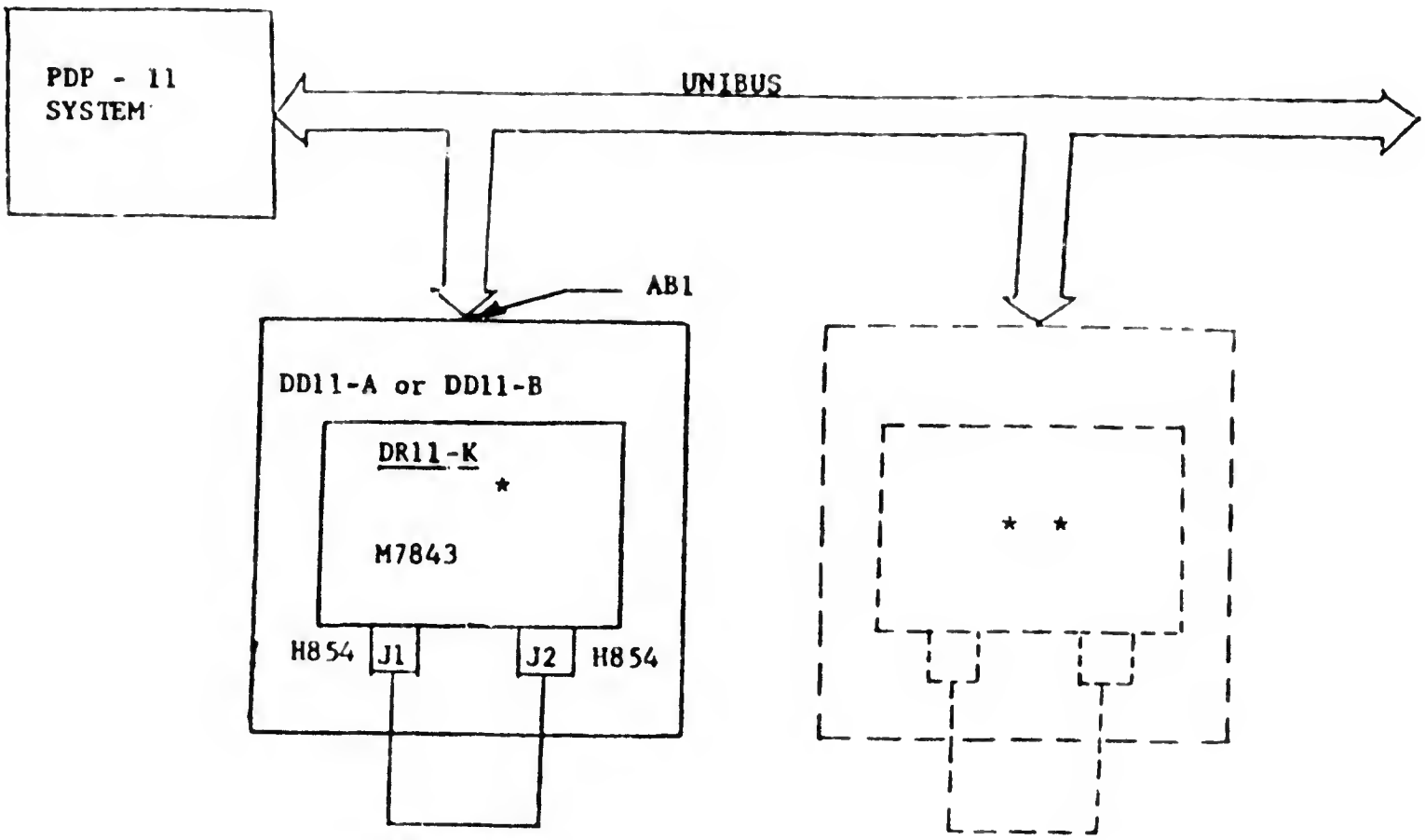
5. Set all the M7843 Module INTERRUPT ENABLE switches off.

6. Start this program with all control switches down (zero).

7. Allow test to run for ten minutes.

   No errors allowed.

   For restart after fix, repeat 1 through 3 for the Interrupt Enable switches on test and repeat 1, 5, and 6 for the Interrupt Enable switches off test.

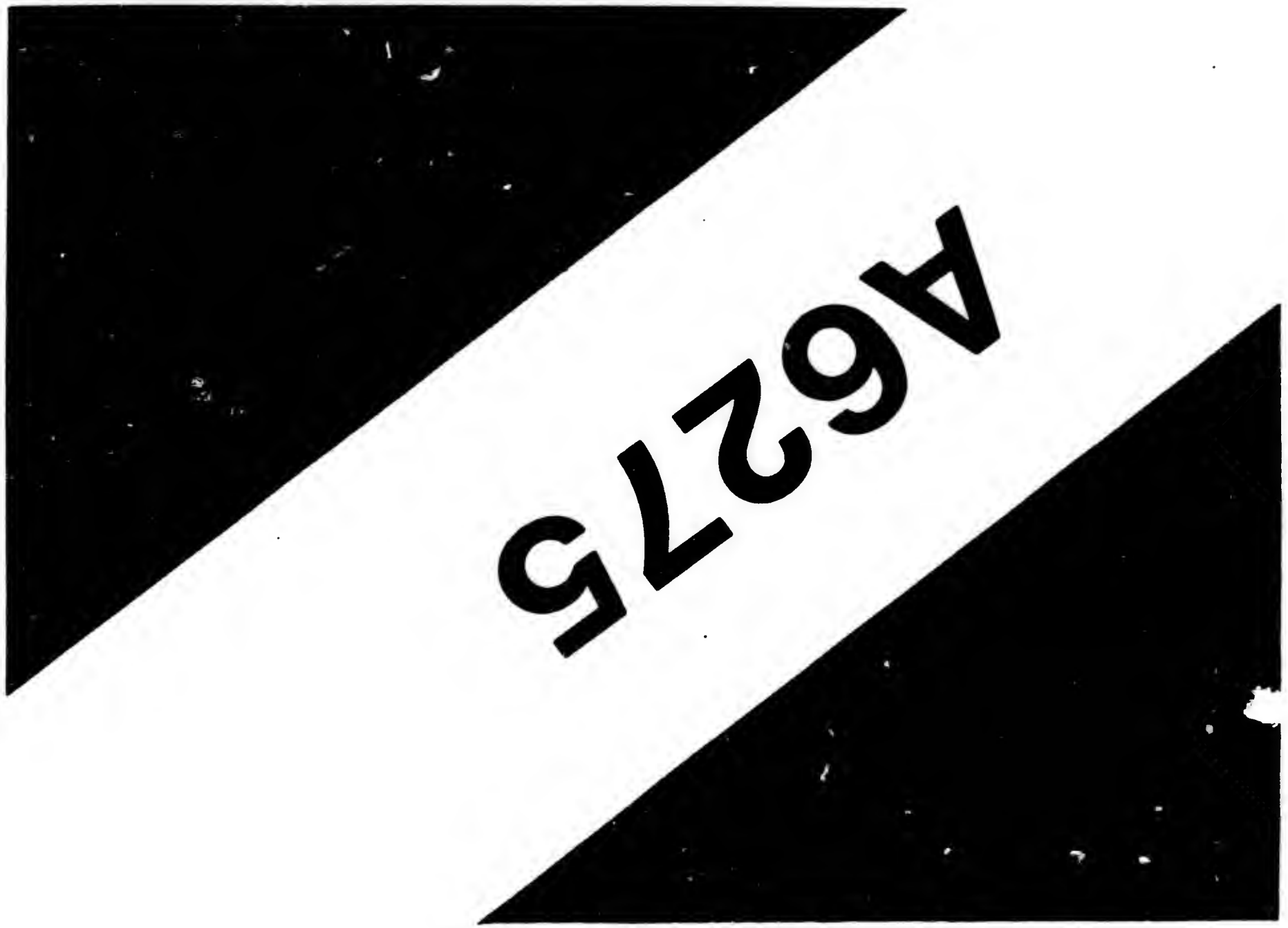


Notes: * The DRK-11 plugs into SPC slot 2 or 3 of the DD11-B or SPC slot 2 of the DD11-A.

** All DR11-K's have the same interrupt switch settings and data path jumpers.

FUNCTIONAL TEST CONFIGURATION

Figure 1


A6,9A
2715

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE 3/27/80

TITLE PHASE I BACKUP DOCUMENTATION FOR DR11-W

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A		MA-A0000-ML009	L. LECLERC	8-80	S. ESTES	8-80

ENG	APPD	SIZE	CODE	NUMBER	REV
BILL WHITBY	TOM JELENIEWSKI	A	SP	MAA6275-0-0	A

1.0 INTRODUCTION

The DR11-W is a general purpose, direct memory access (DMA) device that operates directly to or from memory. It is designed for use in any hex (SPC) small peripheral controller slot. The DR11W can be interfaced with a DRV11B (Q Bus) as well as connected back to back with another DR11-W to form an interprocessor system link. Any number can be added to a single system, with respect to existing configuration guidelines.

The purpose of this document is to define minimum test criteria for FA&T for a single module option and any special steps required to set up option for test. For multiples of this option, refer to reference documentation and diagnostic writeup.

2.0 REFERENCE DOCUMENTATION

2.1 Manuals and Engineering Specifications:

2.1.1 DR11W Engineering Specification SP DR11-W-C

2.1.2 DR11W Users' Guide EK-DR11W-UG

2.2 Prints and Schematics:

2.2.1 DR11W Field Maintenance Print Set MP00693

3.0 REQUIRED TEST EQUIPMENT

3.1 Hardware & Media:

3.1.1 PDP11 with available Hex SPC Slot

3.1.2 8K of Memory

3.1.3 [illegible] console device

3.1.4 B[illegible]5L-01 Loopback Cable (Supplied with DR11-W)

3.1.5 Digital Voltmeter fluke Model 465 or equivalent

3.2 Special Tools:

3.2.1 None

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 CZDRL.?? DR11-W Gen. NPR INTFC.

NOTE: Additional Diagnostic CZDRK?? DR11-W IntrProc. Exer. is not run in FA&T due to need for additional DMA interface and PDP11 Processor.

5.0 SPECIAL INSTRUCTIONS

5.1 For Unibus-11 Systems capacitor C8 (1600 mmf.) must be cut off of of DR11-W Module.

5.2 For UBA (Unibus Adapter) of VAX, both C7 (820 mmf.) and C8 (1600 mmf.) must be installed. Reference Figure 1 drawing for locations of above components.

5.3 Wire in backplane between CA01 and CB01 (NPG jumper) must be removed from slot in which DR11-W is installed.

NOTE: Jumper must be reinstalled when module is removed unless module is replaced with another DMA (Direct Memory Access) device.

6.0 INSTALLATION AND TEST SET-UP INSTRUCTIONS

6.1 Unpacking Instructions:

6.1.1 If DR11-W module is to be installed in a system, dispose of box it was packed in. If part of an option order, retain for repacking.

6.2 Set-Up Instructions:

6.2.1 Remove G727A grant card from hex slot to be used.

6.2.2 Insure DR11-W module has DVA (Device Address) configured for 77241X. Switch pack E120 will have switches 2, 4, 6, 7, 8 and 9 on and 1, 3, 5 and 10 off. Reference Figure 1.

6.2.3 Insure DR11-W module has vector address configured for 124. Switchpack E15 will have switches 3, 5, 7 and 8 on and 2, 4, and 6 off. Switch #1 is unused and its position does not matter. Reference Figure 1.

6.2.4 Insure DR11-W module has operational mode switchpack E105 configured with switches 1, 3 and 4 on and 2 and 5 off. Reference Figure 1.

6.2.5 Insure burst mode switch S1 is in down position (toward row F of module) to select two-cycle burst operation. Reference Figure 1.

6.2.6 Insure BR plug is installed on module in E67 socket. BR5 is the standard plug part #54-08778. (Supplied with DR11-W).

6.2.7 Install BC05L-01 cable (without a twist) between J1 and J2 of DR11-W module.

6.2.8 Install DR11-W module in hex slot in which backplane jumper was removed.

7.0 POWER CHECKS

7.1 Typically when an additional module is installed in a backplane, it will cause a slight dip in voltage. Use a Digital voltmeter to insure that +5V is still within tolerance ±0.25VDC. To do this place voltmeter leads between A2 and C2 (any row) of slot in which module is installed. If necessary adjust applicable regulator for proper voltage.

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 CZDRL?? DR11-W Gen. NPR INTFC.

8.1.1 Load program into memory using applicable load device.

8.1.2 Load address 200 and press start.

8.1.3 After "Do you wish burst data late calibration? (Y = yes, N = no):" is typed out, type <N>

8.1.4 After "Do you wish multiple board dialogue? (Y = yes, N = no):" is typed out, type <N>

8.1.5 If software switch register is invoked, then the following will be printed "SWR = XXXXXX New = ", type<CR>

8.1.6 Program will now test module in maint. & cable mode/with iterations.

8.1.7 End of pass will be indicated by "End Pass #XXXXXX" after approximately 7 seconds for first pass and 60 seconds for each subsequent pass.

8.2 Allowable Errors:

8.2.1 None

M8176

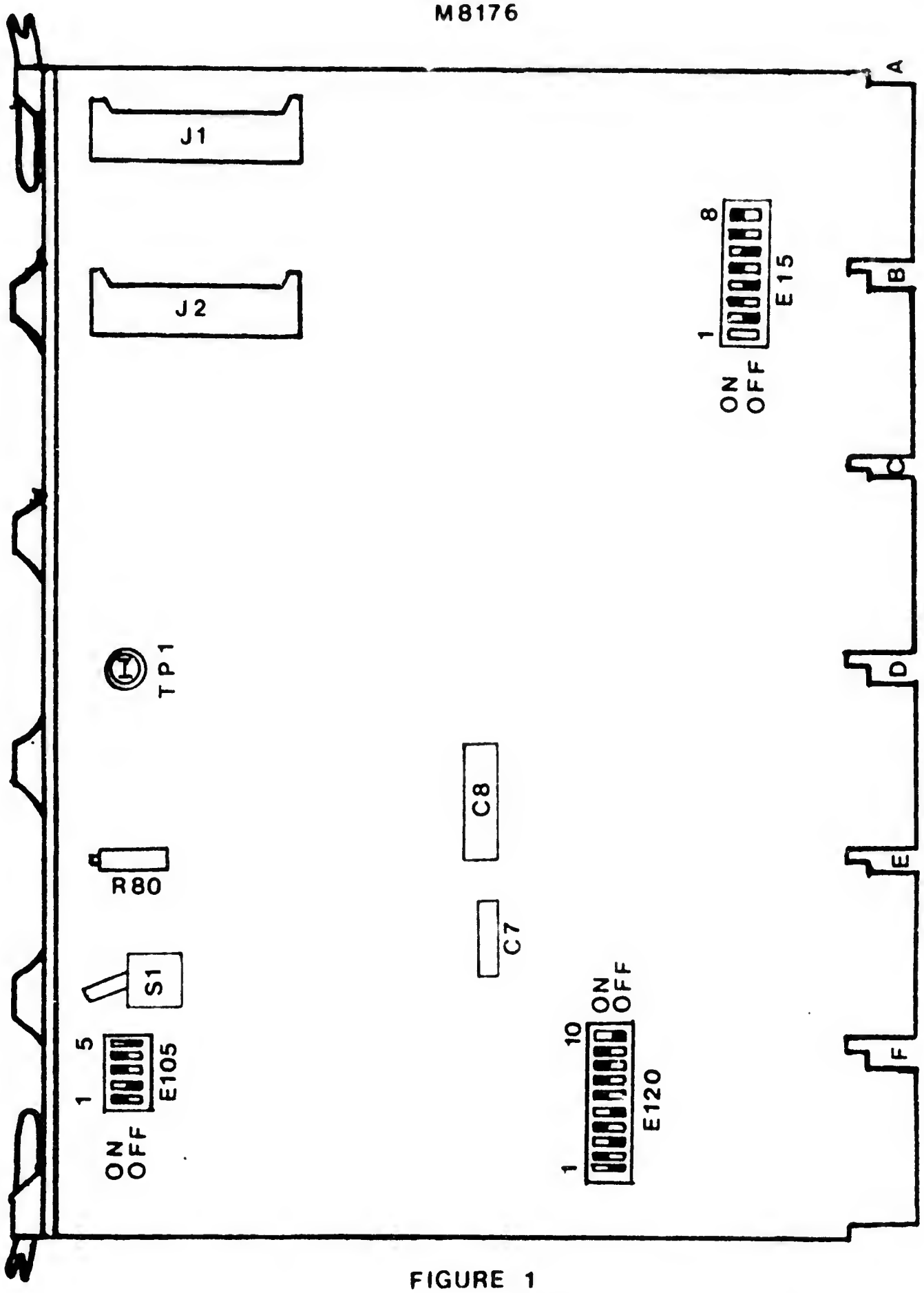


FIGURE 1

	SIZE	CODE	NUMBER	REV
	A	SP	MAA6275 — 0 - 0	A

A710

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE BD03 BINARY/ASCII/BINARY CONVERTER Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7110					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jelenewski		A	SP	MAA7110-0-0	A

MANUFACTURING SPECIFICATION [redacted]

TITLE MODULAR APPROACH TO SYSTEMS TEST Appendix A

BD03 BINARY/ASCII/BINARY CONVERTER

SPECIAL INSTRUCTIONS

Refer to Option Description, Appendix A, Page A-1

TEST EQUIPMENT

REFERENCE DOCUMENTATION

Manuals:	Documentation #CSS-MO-F-4.4-8B
Checkout & Acceptance:	OPT. DES. SECT. 2.3 & 2.4
Engineering Specs:	OPT. DES. PAGE 1-1, SEC. 1.2
Prints:	Drawing Sets #A-ML-BD03-0
MainDEC Listings:	DECSFEC-11-AUXADD

	SIZE	CODE	NUMBER	REV
	A	SP	MAA7110-0-0	A

DEC 16-(392)-1082-N672

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE BD04 DISK INTERRUPT ALARM Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7120					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekowski	Tom	A	SP	MAA7120-0-0	A

BD04 DISK INTERRUPT ALARM

SPECIAL INSTRUCTIONS

BD04 must be cabled to RF11 controller with cable P/N (ATOK cable BD04) Cable plugs into slot D09 of RF11 and slot B02 of BD04, and requires the addition of a write from RF11 pin D09H2 to D16J2 (to be handwired).

TEST EQUIPMENT

Refer to Option Description Page 2-1

Section 2.1-2.4 and page 5-1, sect. 5.1

REFERENCE DOCUMENTATION

Manuals:	Document #CSS-MO-F-54-11
Checkout & Acceptance:	Option Description Page 2-2, Section 2.3.2
Prints:	Drawing Set #A-ML-BD04-0
MainDEC Listings:	DECSPEC-11-AUYADC


A713

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE: BDO5 LINE INTERFACE CONTROLLER Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7130					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Sekerawski	Tom Smith	A	SP	MAA7130-0-0	A

BD05 LINE INTERFACE CONTROLLER

SPECIAL INSTRUCTIONS

Refer to Option Description Page A-1, Appendix A for all checkout and acceptance procedures.

To check for indication of a test failure, transmitter test - refer to App. A, section A.5.1.5.
Receiver Test - refer to App. A, section A.6.

For DECX11 System Exerciser see System Description CSS-MS-F-73-4A, section 5.4

TEST EQUIPMENT

Refer to Option Description page A-2, section A.4.2
For test box connections and section A.5 thru A.7
For setting up test box and running the diagnostic.

REFERENCE DOCUMENTATION

Manuals:	Document No. CSS-MO-F-33-17-A
Engineering Specs:	Option Description page 1-2, section 1.3
Prints:	A-ML-BD05-0
MainDEC Listings:	DECSPC-11-AUZAD-?


A721C10

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE REORDER TRAP DEVICE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7210					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Lebkowski		A	SP	MAA7210-0-0	A

REORDER TRAP DEVICE

SPECIAL INSTRUCTIONS

There are twelve (12) K281 fixed memory. They are to be inserted into Row "C" from right to left for the frist test. (viewed from module side of logic blocks).

For test two (2) the K281 modules must be moved to Row "D".

TEST EQUIPMENT

Refer to Option Description: page A-1, section A-2

REFERENCE DOCUMENTATION

Manuals:	Document No. CSS-MO-F-37-3-B
Checkout Procedures:	Refer to Option Description page A-1 section A.3 thru A.4.2
Acceptance Procedures:	Same as Checkout Procedure
Engineering Specs:	Refer to section 3.9.3 (M)
Prints:	Drawing Set No. A-ML-7606207-0
MainDEC Listings:	DECSPEC-11-ASOADA-PB

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 4/15/80

TITLE LPC01/LPD11 M.A.S.T.

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	Added sections 8.2.13 thru 8.2.15 and Table G	MA-A0000-ML009	L.LECLERC	8-80	S. ESTES	8-80

4

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Ayotte	Steven Estes	A	SP	MA-A7510-0-0	C

LPC01/LPD11 M.A.S.T.

1.0 INTRODUCTION

The LPC01 is a general purpose interface used in conjunction with an LDP11. It can be used by most PDP-11's to provide output to a number of photo-composition machines. All I/O from the PDP-11 thru the LPD11, thru the LPC01 to the Photocomposer is done under program control. The LPC01 includes test circuitry to simulate the photocomposer.

2.0 REFERENCE DOCUMENTATION

2.1 Manuals and Engineering Specifications

2.1.1 LPC01 Maintenance Manual EK-LPC01-MM

2.1.2 LDP11 Maintenance Manual DEC-11-HLPDA

2.2 Prints and Schematics

2.2.1 LPC01 Maintenance Print Set DD-LPC01-0

2.2.2 LDP11 Maintenance Print Set DD-LDP11-0

3.0 REQUIRED TEST EQUIPMENT

3.1 PDP-11 System with an operators console.

3.2 Line Clock.

3.3 Two (2) BC06J-XX cables.

3.4 A DVM accurate to .1V at 15VDC.

3.5 Oscilloscope, Tektronics Model 453 or equivalent.

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 LPD11 Interface Diagnostic ..... DZLPJ

5.0 SPECIAL INSTRUCTIONS

5.1 NOTE - The LPC01 must be tested in conjunction with an LPD11.

The LPD11 requires the adjustment of the "DELAY TIME". Using a scope check the delay settings of the M3020 module at pins B07F2 (adjust TOP POT) and B07T2 (adjust BOTTOM POT). Delay settings will differ according to which model of the LPC01 that it will interface to. Use the following charts to determine the pulse width and backplane pins that must be wired together that will apply to the configuration you have.

NOTES

- Be sure to measure the "Positive" pulse width.

- Before an adjustment can be made it will be necessary to have the following "toggle-in" program running:

```
200/    CLR   R0             5000
        CLR   R1             5001
NEXT:   INC   R1             5201
        MOV   R1, 1727X2     10137, 1727X2
LOOP:   INC   R0             5200
        BNE   LOOP           1376
        BR    NEXT           770
```

LPD11 DELAY TIME SETTINGS

TABLE A (M3020 ADJUSTMENT SETTINGS FOR TOP POT)

LPC01 TYPES	DELAYTIME	CONNECT PIN TO	PIN
A A/B	1.5 M SEC	L2	E1
B A/B	150 uSEC	L2	J1
C A/B	100 uSEC	L2	J1
D A/B	3.5 M SEC	L2	E1
E A/B	300 uSEC	L2	J1
F A/B	4.5 M SEC	L2	E1
H A/B	2 M SEC	L2	E1
J A/B	2.5 M SEC	L2	E1
K A/B	1.0 M SEC	L2	E1
L A/B	100 uSEC	L2	J1
M A/B	1.5 M SEC	L2	E1
N A/B	1.5 M SEC	L2	E1
P A/B	150 uSEC	L2	J1
R A/B	60 uSEC	L2	J1
S A/B	50 uSEC	L2	J1
T A/B	200 uSEC	L2	J1
U A/B	50 uSEC	L2	D1
V A/B	2.5 M SEC	L2	E1
W A/B	100 uSEC	L2	J1

TABLE B (M3020 ADJUSTMENT SETTINGS FOR BOTTOM POT)

LPC01 TYPES	DELAYTIME	CONNECT PIN TO	PIN
A A/B	500 uSEC	S2	U1
B A/B	1 M SEC	S2	P1
C A/B	500 uSEC	S2	U1
D A/B	10 uSEC	S2	S1
E A/B	100 uSEC	S2	U1
F A/B	500 uSEC	S2	U1
H A/B	1 M SEC	S2	P1
J A/B	100 uSEC	S2	U1
K A/B	350 uSEC	S2	U1
L A/B	100 uSEC	S2	U1
M A/B	200 uSEC	S2	U1
N A/B	3.5 M SEC	S2	P1
P A/B	50 uSEC	S2	U1
R A/B	35 uSEC	S2	U1
S A/B	50 uSEC	S2	U1
T A/B	35 uSEC	S2	U1
U A/B	50 uSEC	S2	S1
V A/B	100 uSEC	S2	U1
W A/B	25 uSEC	S2	S1

6.1 Unpacking Instructions as Received from High Volume.

6.1.1 The LPC01 is packed in a cardboard shipping container. Unpack the LPC01 as follows:

A. Remove the LPC01 from the shipping container.

B. Remove the polyethylene cover from the unit.

C. Ensure that the unit is clean and free of any foreign material or damage.

D. Place the LPC01 in the location in which it is to be used (tested).

E. Save all packing material if the unit is to be shipped.

6.1.2 The LPD11 is packed in a cardboard shipping container. Unpack the LPD11 as follows:

A. Remove the LPD11 Logic Backplane from it's container and mount as per configuration sheet.

B. Unpack the modules and insert them into the LPD11 Backplane as per MUL (Module Utilization List).

C. Remove the H740-D power supply from it's shipping container and mount it in the cab as per configuration sheet.

D. For ADDRESS and VECTOR assignments, reference the Product Line supplied Configuration Sheets for your system.
NOTE - The use of the FLOAT PROGRAM is illegal in determining these assignments due to "TYPESET" software limitations.

NOTE - For OPTION ORDERS use the following:
ADDRESS - 172720
VECTOR - 340

ADDRESS - M105 - JUMPER "IN" = a logical 0
VECTOR - M7821 - JUMPER "IN" = a logical 1

6.2 LPC01/LPD11 Cabling and Terminations

6.2.1 The LPD11 Interface is connected to the PDP11 Unibus using a BC11A cable of appropriate length (refer to Configuration sheet). The BC11A cable is plugged into LPD11 slot AB01, and either a Unibus Terminator or a BC11A Unibus cable is plugged into slot AB02.

The LPC01 Interface is connected to the LPD11 Control Interface via a BC06J-XX I/O cable from slot location B01 on the LPC01 to LPD11 slot location A12.
NOTE - Both ends of the BC06J-XX Interface cable have identical single-height M908 cable connectors ..... either connector can be inserted into the control interface or the universal interface.

NOTE - The maximum allowable length for the BC06J-XX interface cable is 250 feet.

7.0 POWER CHECKS

7.1 Refer to TABLES C and D.

TABLE C

LPC01 BACKPLANE VOLTAGE CHECKOUT

VOLTAGE	TOLERANCE	PIN NO.
+5VDC	+/-.25V	A01A2
-12VDC	+/-0.6V	B07R1

TABLE D

LPD11 BACKPLANE VOLTAGE CHECKOUT

VOLTAGE	TOLERANCE	PIN NO.
+5VDC	+/-.25V	A01A2
-15VDC	+/-1.0V	A01B2

8.0 DIAGNOSTIC TEST PROCEDURE

For the specific sequence of diagnostics to be run in any situation, or for the current MAST minimum test criteria, e.g.: pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are the detailed step-by-step instructions for executing each individual diagnostic contained in the "CHECKLIST".

NOTE - The LPD11 will be tested in stand-alone mode by itself.....and then the LPD11/LPC01 will be tested together. Also note that in either case; the same diagnostic is used (DZLPJ).

8.1 LPD11 STAND-ALONE ..... DZLPJ

8.1.1 Check to be sure that there is an M783 module in location B04 and no module in location A05. Also check the switch settings on the M523 module in location A10 for the correct settings as per TABLE E. Note that SW 2-8 should be ON for testing purposes.

TABLE E

LPD11 --- M523 SWITCH SETTINGS

SWITCH	1	2	3	4	5	6	7	8	
1	ON	ON	ON	ON	ON	ON	ON	ON	
2	ON	ON	ON	ON	OFF	OFF	OFF	OFF	-normal/ON-test
3	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	

8.1.2 Load and start the diagnostic at location 200 with the switch register equal to 0.

8.1.3 The console will ask for VECTOR and ADDRESS. Follow the instructions on the print out.

8.1.4 Halt the CPU load address 204, set switches to all zeros and start. It should run with no errors and type "END OF PASS".

8.1.5 Set the console switch 13 to a "1", depress CONTINUE twice. It must run for 10 minutes error free. NOTE - This test will continuously run the logic/data tests and therefore will not print an END-OF-PASS message.

8.1.6 Halt the CPU power down and move the M783 module from location B04 to location A05. Plug the BC06J-XX cable into location A12 and the other end into location B15.

8.1.7 Power up, restart the maintenance diagnostic at location 204 with console switch 13 on a "1". It must run for 10 minutes error free.

8.1.8 Halt the CPU power down and move the M783 module from location A05 to location B04. Remove the BC06J-XX cable from locations A12 and B15. Power up, restart the maintenance diagnostic at location 204 with console switch 11 on a "1". It must run for 5 minutes error free.

8.2 LPD11/LPC01 TESTING ..... DZLPJ

8.2.1 Connect the LPC01 to the LPD11 by plugging the LPD11 I/O cable into LPC01 location B01 and LPD11 location A12.

8.2.2 Plug in another BC06J-XX cable into location B06 of the LPC01 and LPD11 location B15.

8.2.3 Set all switches on the M523 module in the LPC01 to the off position.

8.2.4 Set switch 2-(8) on the M523 on the LPD11 to a "1" and remove the M783 from B04 and plug it into A05.

8.2.5 Plug an M111 module into location A07 of the LPC01 and remove any modules that may be in slots A04, A05, A06.

8.2.6 Put all switches on the LPC01 control panel to the normal position (DOWN).

8.2.7 Load and start the LPD Maintenance Diagnostic at location 200 with SWR = 13.

8.2.8 The program will ask for VECTOR and ADDRESS. Answer it accordingly. Run the program for 5 minutes error free.

8.2.9 Halt the program and power down the system. Remove the LPD11 I/O cable from LPC01 location B01 and plug it into B03. Put SYSTEM 1/SYSTEM 2 switch to SYSTEM 2 position and perform section 8.2.6 - 8.2.7 again.

8.2.10 Halt the program and power down the system. Remove the LPD11 I/O cable from LPC01 location B03 and plug it into B04. Place SYSTEM 1/SYSTEM 2 switch back to SYSTEM 1 position. Place ON-LINE/OFF-LINE switch to the OFF-LINE position and repeat sections 8.2.6 - 8.2.7.

8.2.11 Halt the program and power down the system. Remove the LPD11 I/O cable from LPC01 location B04 and plug it into B01. Place the ON-LINE/OFF-LINE switch back to the ON-LINE position. Place the TEST ENABLE switch in the ENABLE position and remove the IN-HOUSE test cable from the LPD11 and LPC01. Place switch S2-(8) on the M523 module in the LPD11 to the OFF (0) position.

8.2.12 Remove the M783 module from A05 and plug it into slot B04 of the LPD11.

8.2.13 Run the OUTPUT SECTION of the LPD11 Maintenance Diagnostic by setting SWR bit 6 to a "1" and restart the program at location 204. Place the LPC01 TEST ENABLE switch to the "ON" position, place the LPD11 in the "NORMAL MODE" of operation (M523 SW 2-8=0) and type a G. Then enter a series of numeric characters (0-377) and terminate with a "T". This will transmit the characters to the LPC01. Now depress the "TEST" button on the LPC01 and the octal patterns that were transmitted will appear in the DATA LIGHTS of the LPC01.

8.2.14 Power down the system. Remove the LPD11 I/O cable. Set the switches on the M523 module as per TABLE E for the LPD11 and TABLE G for the LPC01, then plug the correct modules into slots A04, or A05, or 6, or A07 etc. as per Table F.

8.2.15 All modules should be left plugged into their proper slots in the backplane and the LPC01 cover should be secured in place using the screws provided.

TABLE F

PHOTOCOMP DRIVE/POLARITY

NOTE - LPC01 module usage is dependant on variation.

LPC01	M050	M111	M205	M624	B7M1 TO *	READER CABLE	INTERFACE CABLE		M5925	
	A4	A5	A6	A7	B10	A6	A7	B7B2	B4	B6	B11	AB12	AB13
A	Y	N	N	N	N	N	N	B7A2	YES	Y	N	N	N
B	N	N	Y	N	N	N	N	B7A2	YES	Y	N	/\	/\
C	N	N	Y	N	N	N	N	B7A2	YES	Y	N	|	|
D	N	N	N	Y	Y	N	N	B7A2	YES	Y	N	|	|
E	N	N	Y	N	N	N	N	B7A2	YES	Y	N	|	|
F	N	N	Y	N	N	N	N	B7A2	YES	Y	N	|	|
H	Y	N	N	N	N	N	N	B7B2	---	Y	N	|	|
J	N	N	N	Y	N	N	N	B7A2	YES	Y	N	|	|
K	N	N	Y	N	N	N	N	B7A2	YES	Y	N	|	|
L	N	N	Y	N	N	N	N	B7A2	YES	Y	N	|	|
M	N	N	Y	N	N	N	N	B7A2	---	Y	N	|	|
N	N	N	Y	N	N	N	N	B7A2	---	Y	N	|	|
P	N	N	N	Y	Y	N	N	B7A2	---	Y	N	|	|
R	N	N	N	N	N	N	N	B7A2	---	Y	N	|	|
S	N	N	N	N	N	N	Y	B7B2	---	N	Y	|	|
T	N	N	N	N	N	N	Y	B7A2	---	N	Y	|	|
U	N	N	N	N	N	Y	N	B7B2	---	N	Y	\/	\/
V**	N	N	N	N	N	N	N	--	---	N	N	N	Y
W	N	N	N	N	N	N	N	--	---	N	N	Y	N

Notes from the chart on the previous page:

* - Wire B7M1 as directed by the above chart for the desired option.

** - The LPC01-V uses an M112 module in slot A14 and an M113 module in slot A15.

TABLE G

M523 SWITCH SETTINGS (SLOT B21 OF THE LPC01)

LPC01 OPTION	SWITCH PACK 1								SWITCH PACK 2								SWITCH PACK 3							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
A	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	0	0	0	0	0	1	0	0	1
B	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
C	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
D	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0
E	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1
F	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
H	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	1	0	0	0	0	0	1	0
J	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1
K	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1
L	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
M	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
N	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0
P	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0
S	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0
T	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1
U	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1
V	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1 = Switch "ON" / 0 = Switch "OFF"

A7600

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE CS1G2-A RAINBOW TEST & ACCEPTANCE PROCEDURE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-7600					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Selemiewski		A	SP	MAA7600-0-0	A

CS1G2-A RAINBOW TEST & ACCEPTANCE PROCEDURE

1.0 INTRODUCTION

This procedure will be used in conjunction with other Mast Procedures to test the minimum and maximum rainbow equipment.

Optional rainbow equipment will also be included as part of this procedure, but will be separated prior to shipment.

1.1 The minimum configuration will be comprised of the following hardware:

1.1.1 1134A-DH - 16K Mos Memory, 10.5" box.

1.1.2 MS11-JP - 16K Mos Memory.

1.1.3 M9301-YX - Xerox Boot Terminator.

1.1.4 DL11-WB - SLU/RTC with BC05C-25.

1.1.5 DR11-K - Digital I/O Interface.

1.1.6 H775-CA - Battery Backup for 1134A.

1.1.7 X020 & X030 - CDC Disk Interface.

1.1.8 X020 & X021 - Character Dispatcher.

1.1.9 X026 - IG Output.

1.1.10 X027 - IG Input

1.1.11 X025 - Font Memory.

1.1.12 X604 - 14 Slot Backplane mounted in the 1134A.

1.1.13 BA11-LH - 5.25 Expander Box.

1.1.14 X605 - 9 Slot Backplane mounted in the BA11-LH.

1.1.15 X023 - Ampex Tape Controller.

1.1.16 X031 - 5V Regulator

1.1.17 BC11A-02 - 2 ft Unibus Cable

1.1.18 M9202 - Unibus Connector

1.1.19 M9001-YX - Connector module

1.1.20 BC08R-08 - Cable

1.2 The maximum configuration will be comprised of the following hardware:

1.2.1 The minimum configuration, minus BC11A-02.

1.2.2 XAUC - Auxillary Unibus Controller.

1.2.3 X025 - Font Memory (3 additional array modules).

1.2.4 MS11-JP - 16K Mos Memory (2 additional) total of 32K on the Aux. Bus.

1.2.5 M7850 - Parity Controller for memory on the Aux. Bus.

2.0 REFERENCE DOCUMENTATI N

2.1 Standard DEC Equipment

2.1.1 Prints:

2.1.1.1 1134A Print Set - MP00190

2.1.1.2 H775 Print Set - MP00014

2.1.1.3 DR11-K Print Set

2.1.1.4 BA11-L Print Set - MP00018

2.1.2 Manuals:

2.1.2.1 EK-KD1EA-MM

2.1.2.2 11/34 System User's Guide - EK-11034-OP

2.1.2.3 M9301 - EK -M9301 - TM

2.1.2.4 MS11-E-J - EK-MS11E-MM

2.1.2.5 M7850 - EK-M7850-MM

2.1.2.6 BA11-L - EK-BA11L-MM

2.1.2.7 DR11-K - EK-DR11K-MM

2.1.2.8 DL11-W - EK-DL11W-MM

2.1.2.9 PDP 1134A Power System Desc EK-1134A-TM

2.2 Rainbow Equipment:

2.2.1 Prints:

2.2.1.1 CS1G2-A Print Set MP00548

2.2.2 Manuals:

2.2.2.1 IG-CSS-MO-F-4.3-17

2.2.2.2 CD-CSS-MO-F-4.3-16

2.2.2.3 X023 Tape - CSS-MO-F-5.9-01

2.2.2.4 X022 - CSS-MO-F-10.3-11

2.2.2.5 X030 -

3 0 REQUIRED TEST EQUIPMENT

3.1 CDC Disk Drive (9762)

3.2 ACT 11 or equivalent

3.3 VOM or Oscilloscope

3.4 LA36 or equivalent

3.5 VT50 or equivalent

3.6 Ampex Tape Drive

3.7 Three (3) X025 Font Memory Arrays

3.8 Two (2) MS11-JP Mos Memories

3.9 M7850 Parity Controller

3.10 Prewritten Tape for Ampex Tape Drive

3.11 XAUC

4.0 AVAILABLE DIAGNOSTICS

4.1 11/34 Lib Kit - ZJF04-RB

4.2 DR11-K Lib Kit - ZJ187-RB

4.3 Disk Controller (X020-X030)
Maindec-11-CIBBJ
Maindec-11-CIBBL

4.4 CD/IG Maindec-11-CIBBI

4.5 Tape Maindec-11- CIBBK

4.6 Aux Window Maindec-11-CIBBH

4.7 DECX-11

4.7.1 Rainbow DECX-11 Module

4.7.1.1 Disk - RRA

4.7.1.2 Tape - TXA

4.7.1.3 CD/IG - CXA

4.8 Diagnostic to generate prewritten tape for Ampex Drive.
Use tape diagnostic Maindec-11-CIBBK, answer questions.

5.0 INSTALLATION INSTRUCTIONS

5.1 Install the H785 Regulator into the 1134A. See 1134A Power Description Manual - EK-1134A-TM.

5.2 Mount the X604 Backplane into the 1134A box.

5.3 Mount the X605 Backplane into the BA11-L Expander Box.

5.4 Remove the Battery Backup jumpers fromthe DD11-PK Processor Backplane. See drawing C-IA-7011523 in the 1134A Print Set.

5.5 Connect the H775-B to the H785 Regulator using cable 7011906.

5.6 Remove the NPG wire (DD11-PK Backplane) C08A1 to C08B1.

5.7 Remove the NPG wire (X604 Backplane) C02A1 to C02B1. (X020 Disk controller)

5.8 Remove the NPG wire (X604 Backplane) C12A1 to C12B1 (X020 CD controller)

6.0 TEST SET UP

6.1 Place switch 2 on the M9301 to the "OFF" position.

6.2 Set the DR11-K to the following device and vector addresses

Device = 767770
Vector = 000150
Set the priority to BR4

6.3 Set the DL11-W to the following device and vector addresses:

Device = 777560
Vector = 000060
Set the priority to BR4

6.4 Set the DL11-W RCVR/TRAN. Baud to 300.

6.5 Check the disk controller for the followi: device and vector addresses:

Device = 764000
Vector = 000160
Check the priority for BR5 (X020 & X030)

6.6 Check the CD (X020 & X021) for the following device and vector addresses:

Device = 764300
Vector = 000270
Check the priority for BR5

6.7 Check the tape controller (X023) for the following device and vector addresses:

Device = 764100
Vector = 000110
Check priority for BR5

6.8 Set the MS11-JP memories to the following starting addresses:

1st - 000000
2nd - 100000
3rd - 200000 } Test Memories will be placed on the Aux Bus.
4th - 300000 }

6.9 Check the parity controllers for the following device addresses:

1st - 772100
2nd - 772102 (Aux Bus)

6.10 Install modules according to UA drawings. Refer to CS1G2-A Print Set, Drawing E-UA-CS1G2-A-0.

7.0 POWER CHECKS

7.1 Check the 1134A voltages as per Mast CA2260, Section 6.5.2

7.2 Connect the H775-B to the H785 regulator.

7.3 Check the H775-C for proper "BATT" status indication. See Mast Procedure (CA2832).

7.4 Check H775-C voltages. See Mast Procedure (CA2832).

7.5 Check X604 Backplane voltages. The voltage values are labeled (etched) onto the Backplane.

7.6 Check BA11-L Expander Box voltages. See Mast CA2260, Section 6.5.1.

NOTE: The core regulator will not be present; therefore, +20V and -5V voltages, will be zero.

7.7 Check X031 for $-5V$. Use test point located on X031 module, voltage is not adjustable.

8.0 DIAGNOSTIC TEST PROCEDURE

8.1 Test 1134A as per Mast Procedure CA2260. See checklist for CA2260.

8.1.1 Memory CA 2825.

8.2 Test DL11-W as per Mast Procedure CA 5330. See checklist for CA 5330.

8.3 Test DR11-K as per Mast Procedure CA6260. See checklist for CA6260.

8.4 Test H775-C as per Mast Procedure CA2832. See checklist for CA2832.

8.5 Test M9301 as per Mast Procedure CA3330. See checklist for CA3330. Use the following CRC = 521
LPC = 46526

8.6 Test the disk controller off-line diagnostic.

8.6.1 Load into memory the disk diagnostic MAINDEC-11-CIBBJ

8.6.2 Set the switch register to 000000.
Load and start 000200. Run in accordance to checklist.

8.6.3 Pass indicator. "END PASS #"

8.7 Test Disk interface on-line

8.7.1 Cable the disk to the controller. Place disk on-line.

8.7.2 Load into memory MAINDEC-11- CIBBL.

8.7.3 Set the switch register to 000000.

8.7.4 Load and start 000200. Run in accordance to checklist.

8.7.5 Pass indicator. "END PASS #"

8.8 Test the CD and IG

8.8.1 Connect the CD to the IG.

8.8.2 Load into memory the CD diagnostic, MAINDEC-11-CIBBI.

8.8.3 Set the switch register to 000000.
Load and start 000200. Run in accordance to checklist.

8.8.4 Pass indicator. "END PASS #"

8.9 Test the tape controller

8.9.1 Maintenance Mode

8.9.1.1 Load into memory the tape diagnostic MAINDEC-11-CIBBK

8.9.1.2 Set switch register to 000000.
Load and start 000200, Run in accordance to checklist.

8.9.1.3 Pass indicator. "END PASS #"

8.9.2 On-Line

8.9.2.1 Connect tape drive to the tape controller.

8.9.2.2 Set switch register to 000000.

8.9.2.3 Load and start 000200. Run as per checklist.

8.9.2.4 Pass indicator. "END PASS #"

8.10 Test minimum configuration with DECX-11 (off-line)

8.10.1 Load into memory the configured DECX-11.

NOTE: Enable DECX-11 to run off-line. See checklist

8.10.2 Load and start. Run in accordance with Mast checklist.

NOTE: Run with disk deselected.

8.11 Test minimum configuration with DECX-11 (on-line)

8.11.1 Connect tape and disk drives to controllers. Place both on-line.

NOTE: Prewritten tape for DECX-11 must be installed on the tape drive.

8.11.2 Load and start. Run as per Mast checklist.

8.11.3 Perform Unibus margining. See Mast Checklist.

8.12 Test maximum configuration (on-line)

8.12.1 Reconfigure system for maximum configuration.

8.12.2 Test auxilliary Unibus control

8.12.2.1 Load into memory the AUC diagnostic, MAINDEC-11-CIBBH

8.12.2.2 Set the switch register to 000000.

8.12.2.3 Load and start 000200. Run as per Mast checklist.

8.12.2.4 Pass indicator. "END PASS #25"

8.12.3 Load into memory DECX-11 for maximum system.

8.12.4 Load and start. Run as per Mast checklist.

8.13 Test system as per specified on construction requisition (max or min).

8.13.1 If necessary, reconfigure to minimum system configuration.

8.13.2 Load and start DECX-11, on-line. Run as per Mast Checklist.

8.14 Check serial bit stream from IG.

8.15 Test DL11-W's @ 9600 Baud.

8.15.1 Load into memory MAINDEC `1-DZDLD.

8.15.2 Run as per Mast Procedur for DL11-WB. See Mast CA5330.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE UNIBUS TESTER Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-8010					

ENG	APPD	SIZE	CODE	NUMBER	REV
TOM Sdeniewski		A	SP	MAA8010-0-0	A

UNIBUS TESTER

INSTRUCTIONS

Insure that the Bus Tester is grounded to the System Under Test. (Use ground strap provided)

Always power up tester first and down last.

REFERENCE DOCUMENTATION

Maint. Manual	A-SP-7605829-12
Engr. Specs:	A-SP-7605829-11
Prints:	D-BS-7605829-0-
MAINDEC Listing:	11-D8A Unibus Test Diag.

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE PRE ACCEPTANCE QC HARDWARE Appendix A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Prev. 7668001-0-9025					

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Jekanowski		A	SP	MAA9025-0-0	A

EN-01083-16-N672-(392)

PRE ACCEPTANCE QC

HARDWARE

1. All hardware with option(s) or system.
2. All hardware tight (screws, subassemblies, sliding racks, etc.)
3. Check for damaged hardware (crushed dents, deep scratches, etc.)
4. Spin fans for bearing or rubbing problems.
5. Wrong hardware (screws too long or short, wrong type washers, etc.)
6. Check alignment of black latches.
7. Filler bars between cabs, kick plates where applicable.
8. Jones strip covers in place.
9. Check extractor and module guides for tightness or cracks.
10. Cabs using only one carousel fan at top must have a plate covering second hole.
11. Check all cab fans for proper direction of air flow. (see prints)
12. Door pins must be secured with "E" rings.
13. Levelers firm with skid.
14. Sliding track mounted units should not interfere with other units in system (verify by sliding in and out to each extreme).
15. Check for missing turn fastners (devices with covers).
16. Three screws must be used on all ends of sliding tracks.

MODULES AND LOGICS

17. Shippability status. (REVCON vs. ECO Status Sheet physical inrpection of current ECO's).
18. Visually inspect any exposed modules for broken components. (pull modules if necessary).
19. DL11 modules must have crystals taped. (tape part #90-08269)

20. Copper shield between MM11L 8K memory increments. (e.g. between slots 3&4 on 16K memory system) (between slots 3,4,6 and 7 on 24K memory system).

21. Check logics for improper wraps or shorts (workmanship).

22. Check logics for cracks, bent pins, and pin markers (on wired logic only).

23. Shrinkies on all pin connectors on logics (capacitors, resistors, etc.)

WIRING/BLING

24. Harnesses and wiring meet workmanship standards.

25. Check cables for stripped wires and proper labeling (workmanship).

26. Check cable stickons for tightness, etc.

27. Pin crimps secured properly in connectors.

28. All panel mounted power supply panels must be grounded to cabinet frame using screw and Tinnerman clamp not at each mounting hole.

29. No pinched wire insulation.

30. Loose tie wraps.

31. Strain reliefs or cable clamps on tubing not wires.

32. No sharp edges near wiring.

33. Check black and white power wiring on reel motor in TU10 for proper crimping.

34. All mate-n-lock wiring in expander box should not be excessively stressed. (Pin crimps should have limited stress on them)

35. Check for cat grommet when blank panels are used near logics.

IDENTIFICATION

36. Correct decals (115V or 240V).

37. Seven digit serial tag (system no.) Top left hand corner of processing bay.

38. U.L. stickers where applicable.

39. Patent decals Mechanical and caution stickers on BA11 boxes.

40. All fuses for proper decals.

MISCELLANEOUS

41. Check all circuit breaker switches for tightness and action.

42. Check console keys for rubbing, etc.

43. Check for recent ECO's.

44. Check cabs and doors for proper grounding.

45. Make sure slide on connectors are crimped properly.

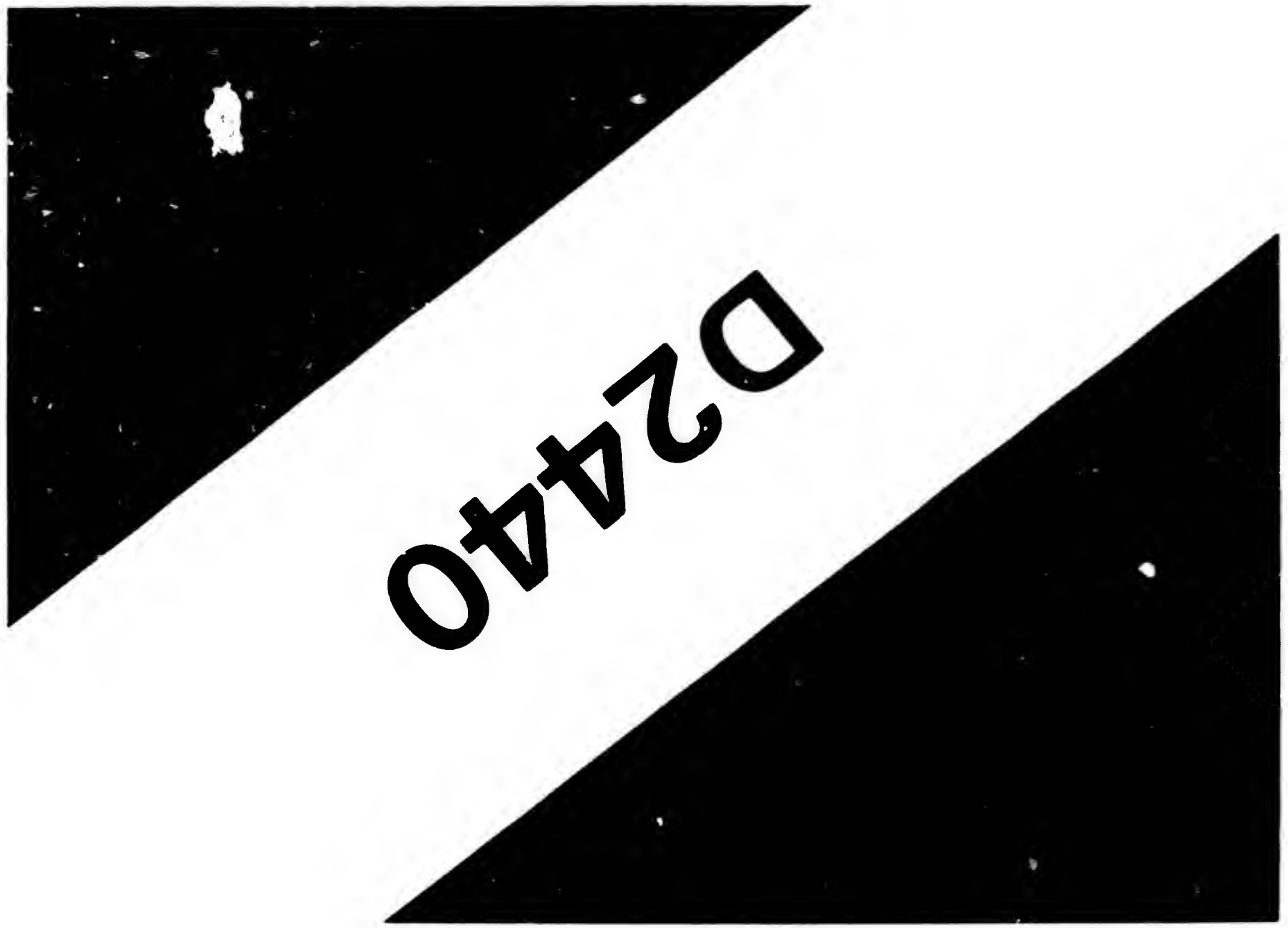
46. Tight shipping blocks and flush with cab.

47. Filters on all cabs.

48. Cardboard on short cabs to eliminate excessive scratching.

49. Hour meters (hooked up at final inspection only). Exception - TU10 bay uses a slave timer to be removed at final inspection.

50. Check for push pennies on logics.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DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE 2/19/79

TITLE KT8-A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ORIG. PER ECO	ML003	L.LECLERC	15-MAY-79	TEJ/JM	7-18-79

ENG	APPD	SIZE	CODE	NUMBER	REV
D. AYOTTE	Tom Jelenevich	A	SI	MA-D2440-0-0	A

FN:01064.1b:Nuno-(392)

KT8-A

1.0 Introduction

The KT8-A is a memory management option that extends the memory capabilities of a PDP8 (KK8-A or KK8-F) CPU from 32K to 128K words. It offers virtual field addressing and memory protection in multi-user, realtime applications with full access of main memory space by DMA devices. In other words; memory addresses are generated by the CPU and by direct memory access (DMA) peripherals. However; the CPU can only provide a 12-bit address and DMA devices are limited to 15-bit addresses. Therefore; to reach a full potential of 128K word memory address space, the KT8-A adds 5 bits to a CPU generated address and 2 bits to a DMA generated addresses.

The intent of this procedure is to provide the necessary information needed for installation and checkout (acceptance) of the KT8-A.

2.0 Reference Documentation

2.1 Manuals & Engineering Specifications

2.1.1 Engineering Product Spec.(A-SP-KT8-A)
2.1.2 User's Manual (EK-KT08A-UG)

2.2 Prints and Schematics (both dev. & controller)

2.2.1 Manufacturing Print Set(MP00561)
2.2.2 Field Print Set (B-TC-KT8-A)

3.0 Required Test Equipment

3.1 Hardware & Media

3.1.1 Any KK8-A or KK8-F CPU
3.1.2 At least 4K of memory
3.1.3 KM8-AC Option

3.1.4 Console Device
3.1.5 DVM accurate to .1 volts at +/-15 volts
3.1.6 Oscilloscope (453 or equivalent)
3.1.7 Assorted soldering tools

4.0 Required Diagnostic Programs

4.1 AJKTA-??

6.0 Installation & Test Set - Up Instructions

6.1 The KT8-A consists of a hex height M8416 memory management control module. Although the M8416 module may be installed in any unused slot with an "E" connector ; it is normally installed in slot 4 or 8 depending on what type of CPU you have. If you have an 8A600 (KK8-F); the KT8-A should be installed in slot 8. But if your CPU is an 8A400 (KK8-A); then the KT8-A should be installed in slot 4.

A system with the KT8-A o[illegible] can only be configured using any combination of MM8AB (16K core) and MS8C (16K or 32K MOS) memories.

6.2 The KM8-AC must have its jumpers reconfigured if the system has more than 32K of memory. (see table A and refer to figure 3)

TABLE A

If System Has -	W1	W2	W3	W4
MORE THAN 32K -	OUT	IN	IN	IN
LESS THAN 32K -	IN	OUT	OUT	OUT

6.3 MM8AB (CORE MEMORY)

6.3.1 If the system is made up of MM8AB core memories (16K), then they must be modified per ECO MM8AB #7. But if the total memory is 32K or less; then no changes need be made. (see table B and refer to figure 2)

TABLE B

MM8-AB 16K CORE MEMORY CONNECTIONS

MEMORY BANK	FIELD	CONNECTIONS WIRE *	JUMPERS **
0	0-3 (0-16K)	AB1 to EB2	1-3, 3-4 in
	4-7 (16-32K)	AB1 to EB2	2-4, 3-4 in
1	0-3 (32-48K)	AB1 to ED2	1-3, 3-4 in
	4-7 (48-64K)	AB1 to ED2	2-4, 3-4 in
2	0-3 (64-80K)	AB1 to EL2	1-3, 3-4 in
	4-7 (80-96K)	AB1 to EL2	2-4, 3-4 in
3	0-3 (96-112K)	AB1 to ER2	1-3, 3-4 in
	4-7 (112-128k)	AB1 to ER2	2-4, 3-4 in

* - A wire must be tack soldered to the fingers of the module for the purpose of Bank Select.
** - See figure 2 for locations

6.4 MS8C (MOS MEMORY - M8417)

6.3.1 If the system is made up of MS8C type memories (16K or 32K MOS), then refer to table C and D for the appropriate switch configuration.

TABLE C

MS8-CA 16K MOS MEMORY SWITCH SETTINGS

MEMORY		SWITCHES SET TO "OFF"	
BANK	FIELD	ALL OTHERS "ON"	***
0	0-3 (0-16K)	S1-1	
	4-7 (16-32K)	S1-2	
1	0-3 (32-48K)	S1-3	
	4-7 (48-64K)	S1-4	
2	0-3 (64-80K)	S1-5	
	4-7 (80-96K)	S1-6	
3	0-3 (96-112K)	S1-7	
	4-7 (112-128K)	S1-8	

*** - See figure 2 for illustration

TABLE D

MS8-CB 32K MOS MEMORY SWITCH SETTING

MEMORY		SWITCHES SET TO "OFF"	
BANK	FIELD	ALL OTHERS "ON"	***
0	0-7 (0-32K)	S1-1 and S1-2	
1	0-7 (32-64K)	S1-3 and S1-4	
2	0-7 (64-96K)	S1-5 and S1-6	
3	0-7 (96-128K)	S1-7 and S1-8	

*** - See figure 2 for illustration

7.0 Power Checks

7.1	Voltage	Backplane Pin	Tolerance
	+5	ANY A2	+/-.25

8.0 Diagnostic Test Procedure

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria, e.g.: Pass Counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the "CHECKLIST".

8.1 AJKTA-?? KT8-A MEMORY MANAGEMENT DIAGNOSTIC

8.1.1 It is assumed that all basic CPU and memory diagnostics have been run successfully before attempting to run the KT8-A diagnostic.

8.1.2 Load the diagnostic using the appropriate load mediam. eg.(APT,RX,RL,ETC.)
The starting and running of the test is determined by the absence or presence of an operators console.

8.1.3 Starting and running with a console-
A. Load address 200 -
B. Select the desired control switch settings-(see table E)
C. Depress clear; then continue-
D. The program will then print:

"AJKTA-??"
KT8-A MEMORY MANAGEMENT OPTION

AMOUNT OF MEMORY(1-37)?" XX<CR>

note - XX is operator input for the number of memory fields. One field = 4K

Examples: 8K = 01
16K = 03
32K = 07

At this point you should enter the number of memory fields available for testing. This figure is required for running the basic addressing section of the diagnostic. If a "0" is typed then the addressing test is not run.

E. Upon completion the diagnostic will type :

"END PASS # N."

No errors are allowed.

TABLE E

CONTROL SWITCHES

SWITCH	STATE	DESCRIPTION
0	0	Halt on error
	1	Inhibit error halt continues on to next test.
1	0	Continue on error
	1	Loop on error
2	0	Don't loop on test
	1	Loop on test displayed in switches 6-11
3	0	Continue testing after a completed pass.
	1	Halt at the end of a pass.
4	0	Print all errors
	1	Inhibit error type-outs
5	UNUSED	

8.1.5 Starting and running without an operators console.

A. Because a hardware console is not necessary a console package has been added to the KT8-A diagnostic. In order to utilize and activate the console package there are three parameter control words that must be altered. These three words are contained in memory locations 20,21 and 22 where:

Location 20 / PSEUDO SWITCH REGISTER

Location 21 / HARDWARE IDENTIFIER 1

Location 22 / HARDWARE IDENTIFIER 2

8.1.6 To activate the console package, you must set location 22 - bit 3=1 and you must also set location 21 - bit 0=0 in order to enable the pseudo switch register.
You can access these locations by running ODT (Octal Debugging Technique) before starting the program. As the following example depicts.

note - the underscored characters are user inputs

```
TYPE:              .ODT
RESPONSE:
TYPE:              20/ ???? XXXX<LF>
TYPE:              217 ???? 3000<LF> (SYS. HAS OPT
                                1&2)
TYPE:              22/ ???? 400<CR> (SYS. HAS NO
                                CONS.)
```

note - The ? are previous contents of.
The X are your desired contents

note - see table E for
control switch settings

See tables F and G for a complete breakdown of the hardware identifier 1 and 2 functions.

8.1.7 Starting the program can be accomplished by typing in the following:

200G<CR>

8.1.8 The program will then print the following message:

"AJKTA-??"
KT8-A MEMORY MANAGEMENT OPTION

AMOUNT OF MEMORY(1-37)?" <CR>

note - <CR> is the default

8.1.9 Type in the number of extended memory fields and type a caraige return. The program should run error free and will terminate with the message:

"END PASS # N."

Run times will vary according to how much memory is selected.

8.1.10 Control characters are supplied to give the user the ability to perform various functions while the program is running. They are as follows:

CONTROL C (^C)	This forces a restart at location 7600 of field zero or return to the console monitor.
CONTROL S (^S)	This will stop any output to a console terminal. The only way to continue is to type a ^Q to resume printing or a ^C to abort the program completely. This is a non printing character.
CONTROL Q (^Q)	This is to continue a program after a ^S is typed. This is a non printing character.

CONTROL G (^G) The ^G allows the user to change the value of the psuedo-switch register. Upon typing ^G the console terminal will print "^G" and then the switch register question. At this point the user may change the value of the pseudo-switches or type a terminating character.

TABLE F

LOCATION 21 / HARDWARE IDENTIFIER 1

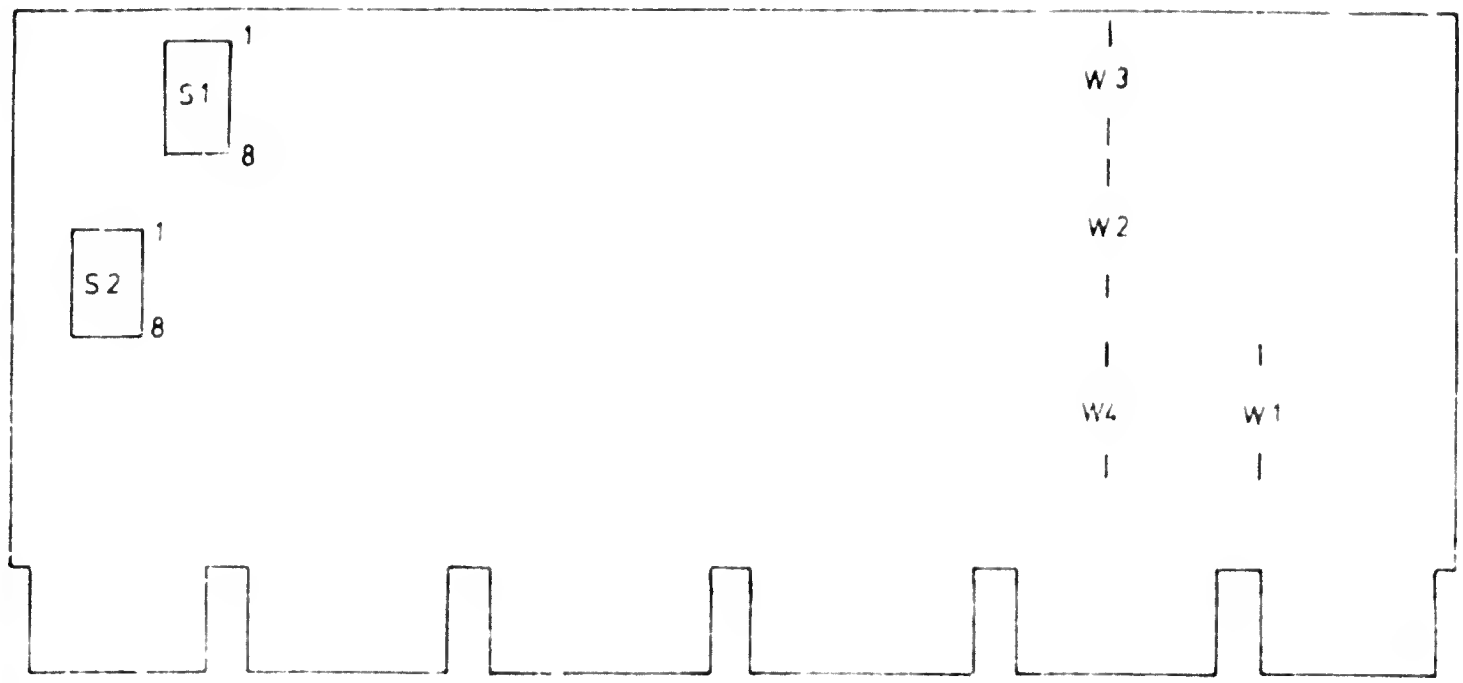
BIT	OCTAL VALUE	FUNCTION WHEN 0	FUNCTION WHEN 1
0	4000	use pseudo switches	use hard switches
1	2000	no option 1	has option 1
2	1000	no option 2	has option 2
3	400	no 8A simulator	has simulator
4	200	no option simulator	has simulator
5	100	not on 8A XOR	on 8A XOR
6	40	not PDP8-E type CPU	PDP8-E type CPU
7-11		8A memory size EX. 4K = 00 8K = 01 28K = 06 128K = 37	

TABLE G

LOCATION 22 / HARDWARE IDENTIFIER 2

BIT	OCTAL VALUE	FUNCTION WHEN 0	FUNCTION WHEN 1
0	4000	not on API line	on API &A line
1	2000	not on ACT line	on ACT &E line
2	1000	not yet defined	
3	400	use pseudo switches	

KM8 -AC (M8317-YB)



SWITCH SETTINGS

	1	2	3	4	5	6	7	8
S1	OFF	ON	ON	OFF	OFF	ON	ON	ON
S2	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON

FIGURE 1

MM8-AB CORE MEMORY

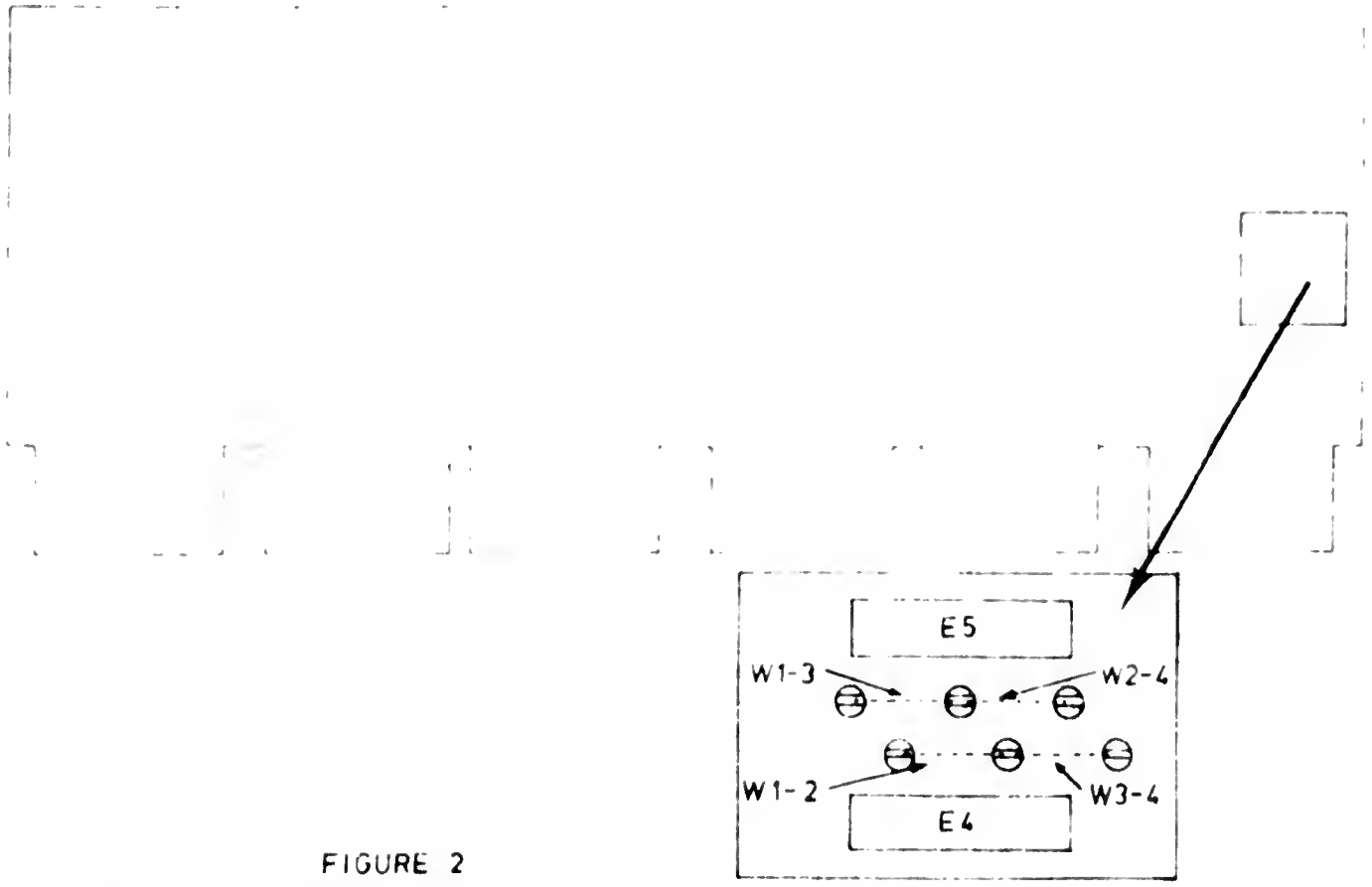
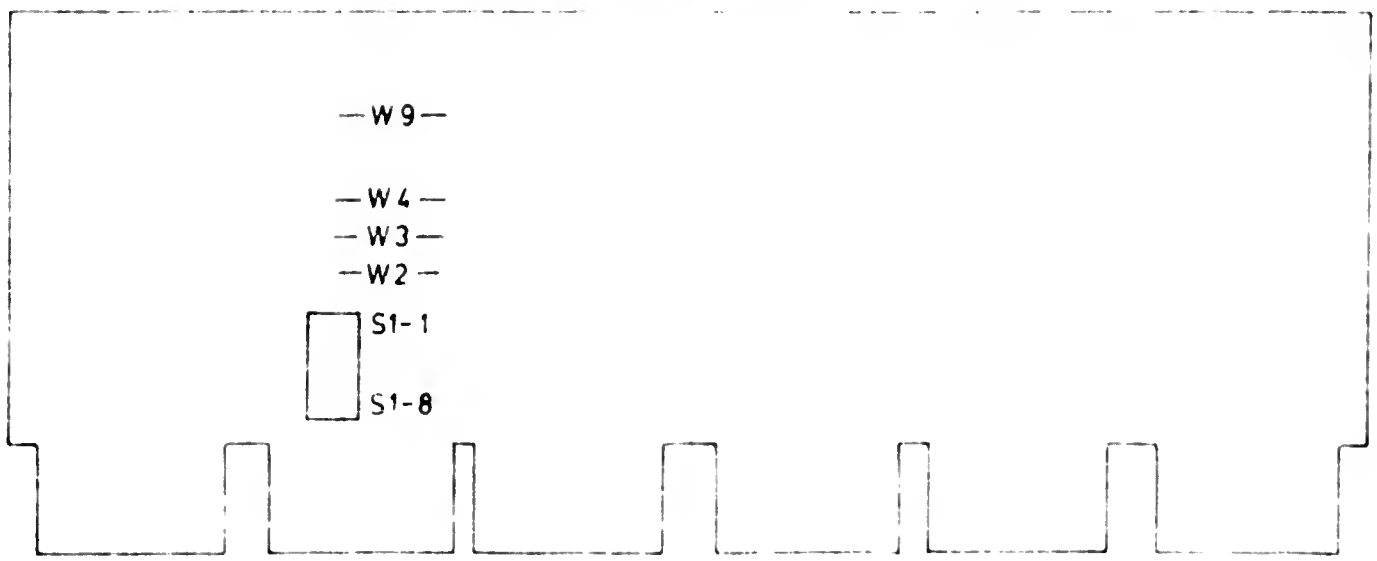


FIGURE 2

MS8-CA/CB (M8417)



JUMPER CONFIGURATIONS (REFERENCE ONLY-SET AT FACTORY):

IN: W2, W3, W4, W9

OUT W1, W5, W6, W7, W8, W10, W12, W13, W14, W15, W16

FIGURE 3


D42716

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE 2/20/79

TITLE RL8-A/RL01

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ORIG. PER ECO	ML0003	L LECLERC	15-MAY-79	[illegible]	7-15-79

ENG	APPD	SIZE	CODE	NUMBER	REV
D. AYOTTE	Tom Lecuyer	A	SP	MA-D4216-0-0	A

RL8-A/RL01

1.0 Introduction

The RL8-A/RL01 Disk Subsystem is a random access, mass storage system that stores up to 3.5 million 12-bit words (per disk) in fixed length blocks on pre-formatted disk cartriges. The RL8-A controller provides the interface and the control functions between all Omnibus PDP-8's and the RL01 disk drives.

The RL8-A (M8433) interface and control logic is contained on a single multi-layer hex height module. It is inserted into the Omnibus backplane and connected to the first drive via a BC08J-20 interface cable. Connections between the controller and the drives are made using the conventional daisy chain method with a 70-12122-08 cable.

The RL8-A controller can control up to four RL01 disk drives. It can communicate with one or more drives, but can only transfer data to or from one drive at a time.

2.0 Reference Documentation

2.1 Manuals & Engineering Specifications

2.1.1 RL8-A Omnibus controller Technical Manual	EK-RL8A-TM
2.1.2 RL01 Drive Technical Description Manual	EK-RL01-TD
2.1.3 RL01 Disk Subsystem Service Manual	EK-RL01-SV
2.1.4 RL01 Disk Drive, Parts Breakdown	EK-RL01-IPB
2.1.5 PDP8-A Miniprocessor User's Manual	EK-81002-MM
2.1.6 PDP8-A Operator's Handbook	DEC-8A-HOPHB

2.2 Prints and Schematics (Both Drive & Controller)

2.2.1 RL8A Field Maintenance Print Set MP00538

2.2.2 RL01 Field Maintenance Print Set MP00527

3.0 Required Test Equipment

3.1 Hardware & Media

3.1.1 A PDP8A,E,F or 8M CPU

3.1.2 At least 8K of memory

3.1.3 An RL8A/RL01 Controller/Drive

3.1.4 Diagnostic loader (Diskette,Paper tape,etc.)

3.1.5 A console device

3.1.6 DVM, accurate at .1V @ 15V

4.0 Required Diagnostic Programs

4.1 08-AJRLA.....DISKLESSS CONTROLLER

4.2 08-AJRLB.....DRIVE FUNCTION 1

4.3 08-AJRLC.....DRIVE FUNCTION 2

4.4 08-AJRLD.....DRIVE COMPATIBILITY

4.5 08-AJRLE.....PERFORMANCE EXERCISER

4.6 08-AJRLG.....PACK VERIFIER

5.0 Special Instructions

5.1 When converting a RL01 from 115V to 230V, it is only necessary to invert the voltage selector plug, change the power plug and the serial tag. The voltage range plug should be left on "NOM".

6.0 Installation And Test Set Up Instruction

6.1 Unpacking and Installation

6.1.1 Remove the drive from the shipping carton and inspect for physical signs of shipping damage. The shipping carton should contain the following items:

1 - RL01 disk drive assembly
1 - envelope w/paperwork
1 - I/O cable assembly - 10 ft.
1 - Set of chassis slides
1 - Bag of mounting hardware (quantities and P/N's specified by A-PL-RL02-A-0)
1 - RL01 Disk subsystem users guide
1 - Field Maintenance print set

6.1.2 Shipping Brackets

6.1.2.1 There is a shipping bracket; the head retainer bracket. When the drive is powered on, the top cover may be opened and the bracket can be seen in front of the positioner assembly. Loosen the one screw holding it in place, and let the bracket pivot downwards 90 degrees. Re-tighten the screw.

6.1.2.2 When shipping the drive, restore the head restraint shipping bracket to its upright position, and if the drive is slide mounted, install the 2 shipping brackets which were contained in the hardware kit. For instructions, refer to drawings E-UA-RL02A-0-0 or E-UA-RL01AK-0-0 for bracket location.

6.2 Controller Installation

6.2.1 To make the RL8-A (M8433) compatable with the FI02 disk (double density), remove W3 and install W8. Refer to figure 1.

6.2.2 Verify that the IOT Device code and Break Priority jumpers are configured properly. Refer to tables A, B and C. (See figure 1 for jumper and ROM locations.)

NOTE - standard Device Codes are 60/61 and priority 0

TABLE A

IOT DEV. CODE	JUMPERS INSTALLED	
	W1	W2
60/61	IN	OUT
62/63	IN	IN

TABLE B

BREAK PRIORITY	JUMPERS INSTALLED		
	W3	W4	W5
0	IN	OUT	IN
1	OUT	IN	OUT

TABLE C

FACTOPY INST. JUMPERS	W1	1--3	2--5	W6	W7
ROM PN# 23012E2-00	IN	OUT	IN	IN	OUT
UV PROM PN# 23040B7-00	IN	IN	OUT	OUT	IN

6.2.3 Dress the BC08J-20 interface cable in the PDP-8 chassis and connect the Berg connector to the M8433 controller module.

6.2.4 Install the M8433 module in any unused slot that lies below the last memory slot in the Omnibus backplane. (Slot 17 in KK8-F "Word Processors")

6.2.5 Insert the free end of the BC08J-20 interface cable into the RL01 "CABLE IN" connector of the rear of the first disk drive.

6.2.6 If this is a multi-drive system, connect the daisy chain cable (70-12122-08) from the "CABLE OUT" connector of the previous drive to the "CABLE IN" connector on the next drive.

6.2.7 Install the drive terminator module (70-12293) in the last drive's connector marked, "CABLE OUT".

6.2.8 Install the proper unit select plug at the front of each drive.

SELECT PLUG	PART NUMBER
0	12-12691-00
1	12-12691-01
2	12-12691-02
3	12-12691-03

7.0 Power Checks:

7.1 Inspect the terminal block assembly at the rear of the drive to ensure that it is configured properly for the input power to be used. There are two voltage ranges: Low 90-132 VAC, High 180-264 VAC

The power requirements for the RL8-A (M8433) are:

+5 Vdc +/- .25 V -at test point/Finger AA2
+15 Vdc +/- .5 V -at test point/Finger DA2
-15 Vdc +/- .5 V -at test point/Finger DB2

8.0 Diagnostic Test Procedure

"For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimum test criteria, e.g.: pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the CHECKLIST."

The diagnostics that are run to checkout the RL8-A/RL01 all contain the "CONSOLE PACKAGE". This package is a part of every diagnostic and supplies the user with a software switch register and a few control keys that allow operator intervention. A description of the control keys; along with a complete breakdown of the solftware parameters (switch register, etc.), can be found in the diagnostic listings.

8.1 08-AJRLA - Diskless Controller Diagnostic

8.1.1 It is assumed that the CPU, console device and all available memory have successfully run their respective diagnostics.

8.1.2 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX, APT,etc.)

note - the drive with the terminator must be powered off or turned off line because this is a "diskless" diagnostic.

8.1.3 With the switch register = 0; start the program by typing:

200G

8.1.4 Upon start-up the program will ask the following :

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLA?? RL8-A DSKLS CTRLR	
SR=0000	<CR>
ENTER AMOUNT OF CONTIGUOUS MEMORY AVAILABLE FOR USE:	XX<CR>

where XX = 1 - 8K
2 - 12K
3 - 16K
4 - 20K
5 - 24K
6 - 28K
7 - 32K

EXECUTE PHASE LOCKED LOOP ADJUSTMENT ROUTINE? <CR>

"END PASS 000X"

8.2 C8-AJRLB - Drive Function 1

8.2.1 It is assumed that the diskless controller diagnostic (AJRLA) has been run error free before continuing.

8.2.2 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX,APT,etc.)

note - power up all drives

8.2.3 With the switch register = 0; start the program by typing:

200G

8.2.4 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLB?? RL8-A/RL01 DR PT1	
SR=0000	<CR>
TEST DRIVE 0 ?	Y/N<CR>
TEST DRIVE 1 ?	Y/N<CR>
TEST DRIVE 2 ?	Y/N<CR>
TEST DRIVE 3 ?	Y/N<CR>
IS 8/A OPTION 1 AVAILABLE?	Y<CR>
DO YOU WISH TO SELECT NON-DEFAULT PARAMETERS?	N<CR>
END PASS 000X	

8.3 08-AJRLC - Drive Function 2

8.3.1 It is assumed that the drive function 1 diagnostic (AJRLB) has been run error free before continuing.

8.3.2 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX,APT,etc.)

8.3.3 With the switch register = 0; start the program by typing:

200G

8.3.4 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLC?? RL8-A/RL01 DR PT2	
SR=0000	<CR>
TEST DRIVE 0 ?	Y/N<CR>
TEST DRIVE 1 ?	Y/N<CR>
TEST DRIVE 2 ?	Y/N<CR>
TEST DRIVE 3 ?	Y/N<CR>
IS 8/A OPTION 1 AVAILABLE?	Y<CR>

DO YOU WISH TO SELECT NON-DEFAULT PARAMETERS? <CR>

END PASS 000X

8.4 08-AJRLG - Pack Verifier

8.4.1 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX,APT,etc.)

8.4.2 With the switch register = 0; start the program by typing:

200G

8.4.3 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLG?? RL8/RL01 PCK VFYR	
SELECT NON-DEFAULT PARAMETERS?	<CR>
TEST DRIVE 0 ?	Y/N<CR>
TEST DRIVE 1 ?	Y/N<CR>
TEST DRIVE 2 ?	Y/N<CR>
TEST DRIVE 3 ?	Y/N<CR>
ARE YOU SURE?	YES<CR>

WORKING ON UNIT X

PACK SERIAL NO.: XXXXXX

NO NEW BAD SECTORS FOUND (FIELD FILES NOT REWRITTEN)

DONE

8.5 08-AJRLD - Drive Compatibility

8.5.1 Load the program into memory fields 0 and 1 using the appropriate load device.(eg RX,APT,etc.)

NOTE - at least 2 disk drives are needed along with one RL01 Disk Pack with not more than 16 bad sectors

8.5.2 With the switch register = 0; start the program by typing:

200G

8.5.4 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJB1LD?? RL8A/RL01 DRIVE COMPATIBILITY TEST	
UNIT 0 = DRIVE (0-7)?	0<CR>
UNIT 0 ON THIS SYSTEM (Y/N)?	Y<CR>
DEVICE CODE (60,61) (Y/N)?	Y<CR>
UNIT 1 = DRIVE (0-7)?	1<CR>
UNIT 1 ON THIS SYSTEM (Y/N)?	Y<CR>
DEVICE CODE (60,61) (Y/N)?	Y<CR>
UNIT 2 = DRIVE (0-7)?	2<CR>
UNIT 2 ON THIS SYSTEM (Y/N)?	Y/N<CR>
DEVICE CODE (60,61) (Y/N)?	Y<CR>
UNIT 3 = DRIVE (0-7)?	3<CR>
UNIT 3 ON THIS SYSTEM (Y/N)?	Y/N<CR>
DEVICE CODE (60,61)?	Y<CR>
SR=0000	<CR>
ARE YOU SURE (Y/N)?	Y<CR>

NOTE - the following dialogue is for two drives selected

MOUNT PACK ON DRIVE 0 THIS SYSTEM

WAIT FOR DRIVE READY

TYPE <RETURN> TO CONTINUE . . . <CR>

MOUNT PACK ON DRIVE 1 THIS SYSTEM

WAIT FOR DRIVE READY

TYPE <RETURN> TO CONTINUE . . . <CR>

TEST COMPLETE - ALL DRIVES COMPATIBLE

NOTE - a <CR> will restart the program without the dialogue
- a <LF> will restart the program completly

8.6 08-AJRLE - Performance Exercisor

8.6.1 Load the program into memory fields 0 and 1 using the appropriate load device.(eg., RX,APT,etc.)

8.3.3 With the switch register = 0; start the program by typing:

200G

8.3.4 Upon start-up the program will ask the following questions:

PROGRAM PROMPT	OPERATOR RESPONSE
AJRLE?? RL8A/RL01 PERFORMANCE EXERCISER	
NUM FLDS EXTD R/W MEM (1-7)?	XX<CR> where X = 1 - 8K 2 - 12K 3 - 16K 4 - 20K 5 - 24K 6 - 28K 7 - 32K
TEST DRIVE 0 (Y/N)?	Y/N<CR>
TEST DRIVE 1 (Y/N)?	Y/N<CR>
TEST DRIVE 2 (Y/N)?	Y/N<CR>
TEST DRIVE 3 (Y/N)?	Y/N<CR>
DC (60,61) (Y/N)?	Y<CR>
SR=0000	<CR>
ACPT MODE (Y/N)?	Y<CR>
ARE YOU SURE (Y/N)?	Y<CR>

NOTE - the following is for two drives (0 and 1)

DRIVE 0 PACK WRITTEN

DRIVE 0 PACK READ OK

DRIVE 1 PACK WRITTEN

DRIVE 1 PACK READ OK

END PASS DRIVE 0 SEEK

END PASS DRIVE 1 SEEK

END PASS DRIVE 0 DATA

END PASS DRIVE 1 DATA

END PASS DRIVE 0 ACPTD

END PASS DRIVE 1 ACPTD

8.7 Error Summary - no errors allowed

RL01
DISK CONTROLLER BOARD
M8433

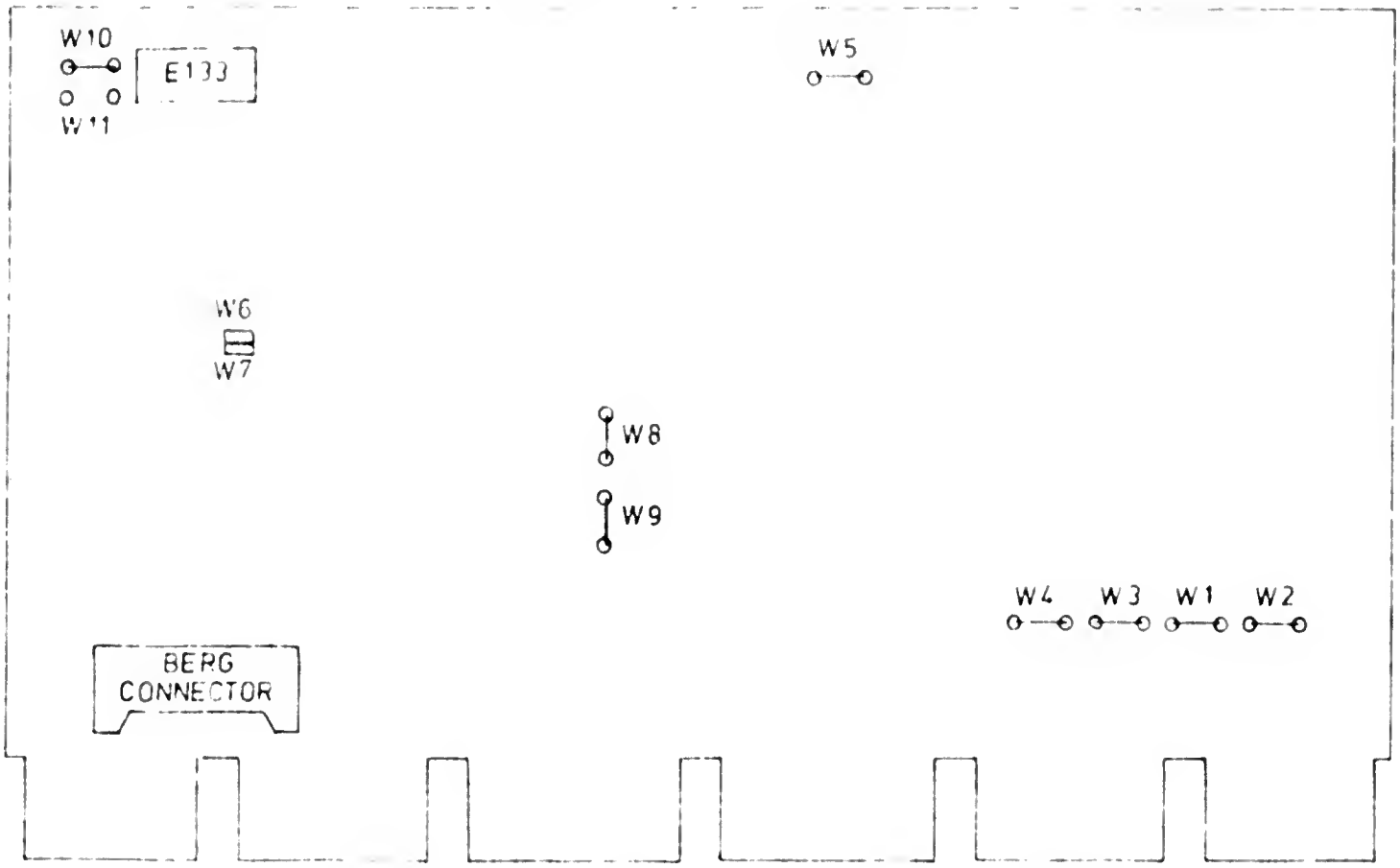
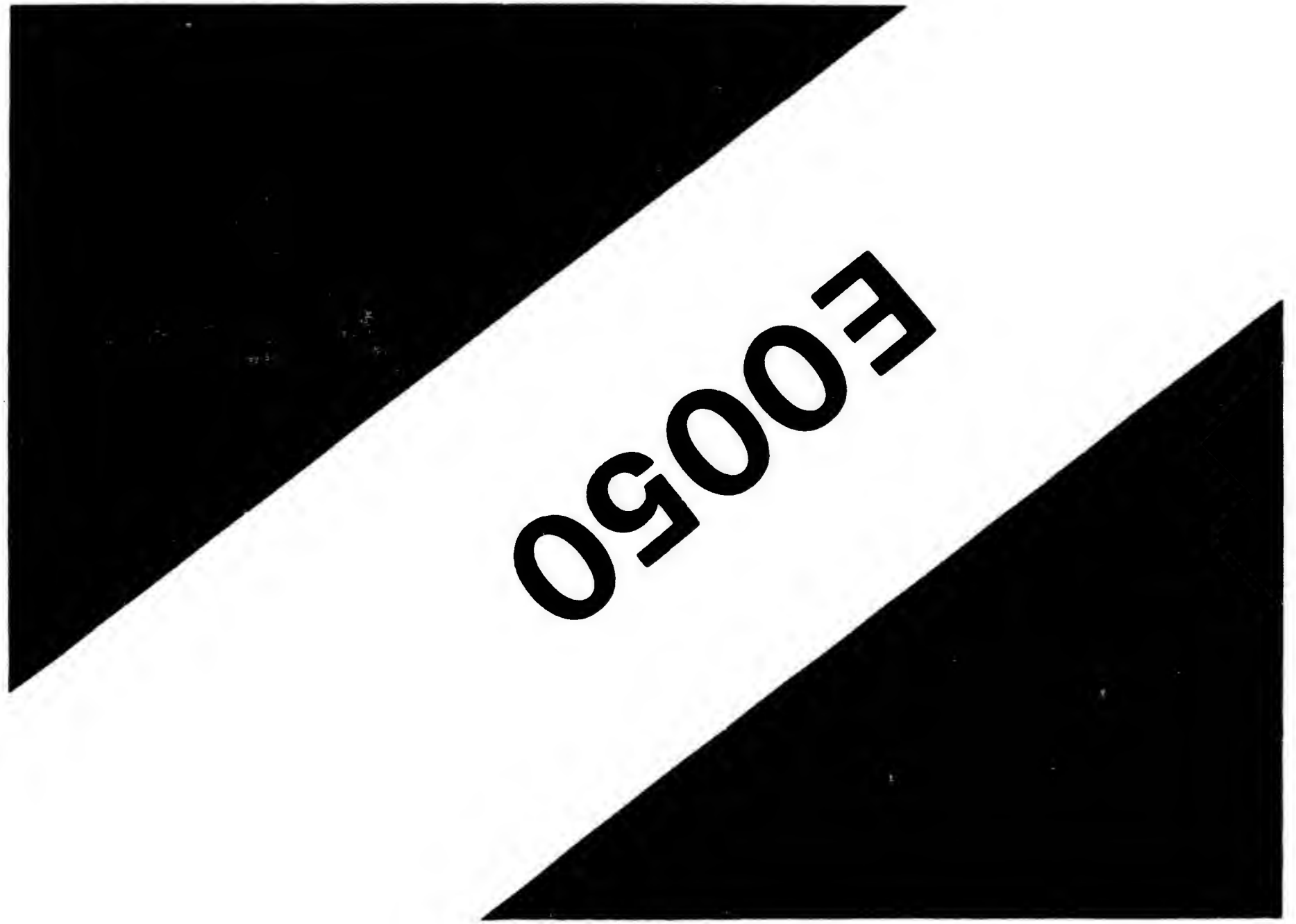


FIGURE 1


0500E

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 2/3/81

TITLE MAST PHASE III UETP

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	Initial Release	-	S. Estes	8/27/79		
B	Add to spec inst. and RSX[illegible]+ to sheet 3.	1	S. Estes	11/[illegible]/[illegible]		
C	Remove T1/78 references and LSI references. Add note about "Q-BUS" CPU's. Add RSX[illegible]+ to UETP matrix on page five.	2 M1012	T. Kenney D. Motte	6/1/80 2/2/81	David Motte	2/9/81

ENG	APPD	SIZE	CODE	NUMBER	REV
S. Estes	F. Beck	A	SB	[illegible]A-E0058-/-0	C

EN-01984 (R-9872 (3/84)

MAST PHASE III - UETP

1.0 Introduction

UETP (User Environmental Test Package) is a universal name for system test software that runs under an operating system. Currently only RSX11, RSTS/E, RT11, and RSX11M+ have some form of recognized UETP package. Since every available operating system does not have a separate UETP package, a decision matrix has been developed to aid the user in the selection of UETP packages based on the Customer's configuration. This document is not intended to instruct the user on UETP or system software build. Reference appropriate system software manuals for software and UETP build and run procedures.
Note: This document is only applicable to PDP11 family processor's.

2.0 Reference Documentation

2.1 Software Product Description (SPD)
Table of Contents.

3.0 Required Test Equipment

3.1 Minimum Hardware & Media
The minimums presented in this section may override the 'No Software Ordered' matrix in section 5.1.2.

3.1.1 UETP minimums

3.1.1.1 For RSTS/E UETP - More than 64KW of memory, memory management (KT) and at least one supported system disk. NOTE: RSTS/E UETP DOES NOT SUPPORT"Q-BUS" CPU's.

3.1.1.2 For RSX11 UETP - 32KW of memory, memory management (KT) and at least one supported system disk (with a MAGTAPE) or two supported system disks (without a MAGTAPE).

3.1.1.3 For RT11 UETP - 16KW of memory and at least two supported system disks.

3.1.1.4 For RSX11M+ - 256KW of memory and one supported system disk (with MAGTAPE) or two supported system disks (without MAGTAPE).

3.1.2 Hardware minimums

3.1.2.1 VAX 11/780 systems run VAX VMS UETP.

3.1.2.2 RX floppy disks are currently only supported as a system disk by RT11.

3.1.2.3 All systems require an appropriate console terminal.

4.0 Required Diagnostic Programs

Not Applicable

5.0 Special Instructions

5.1 The UETP decision matrix's listed in sections 5.1.1 and 5.1.2 should be used as the guide for selecting a particular operating system UETP package.

Note: Should the Customer configuration support the operating system software ordered but does not meet the UETP minimums as outlined in section 3.1.1 , Software Support will determine which UETP will be run. Software Support will either select the next level UETP (from RSTS to RSX, from RSX to RT11) or modify the Software build as deemed necesary.

5.1.1 This Matrix is to be used when Customer has specified operating system software or license. This matrix is based on the best estimate of operating system similarities with RT, RSTS/E, RSX, and RSX11M+. If Customer software is not listed below, use "No Software" Matrix in 5.1.2.

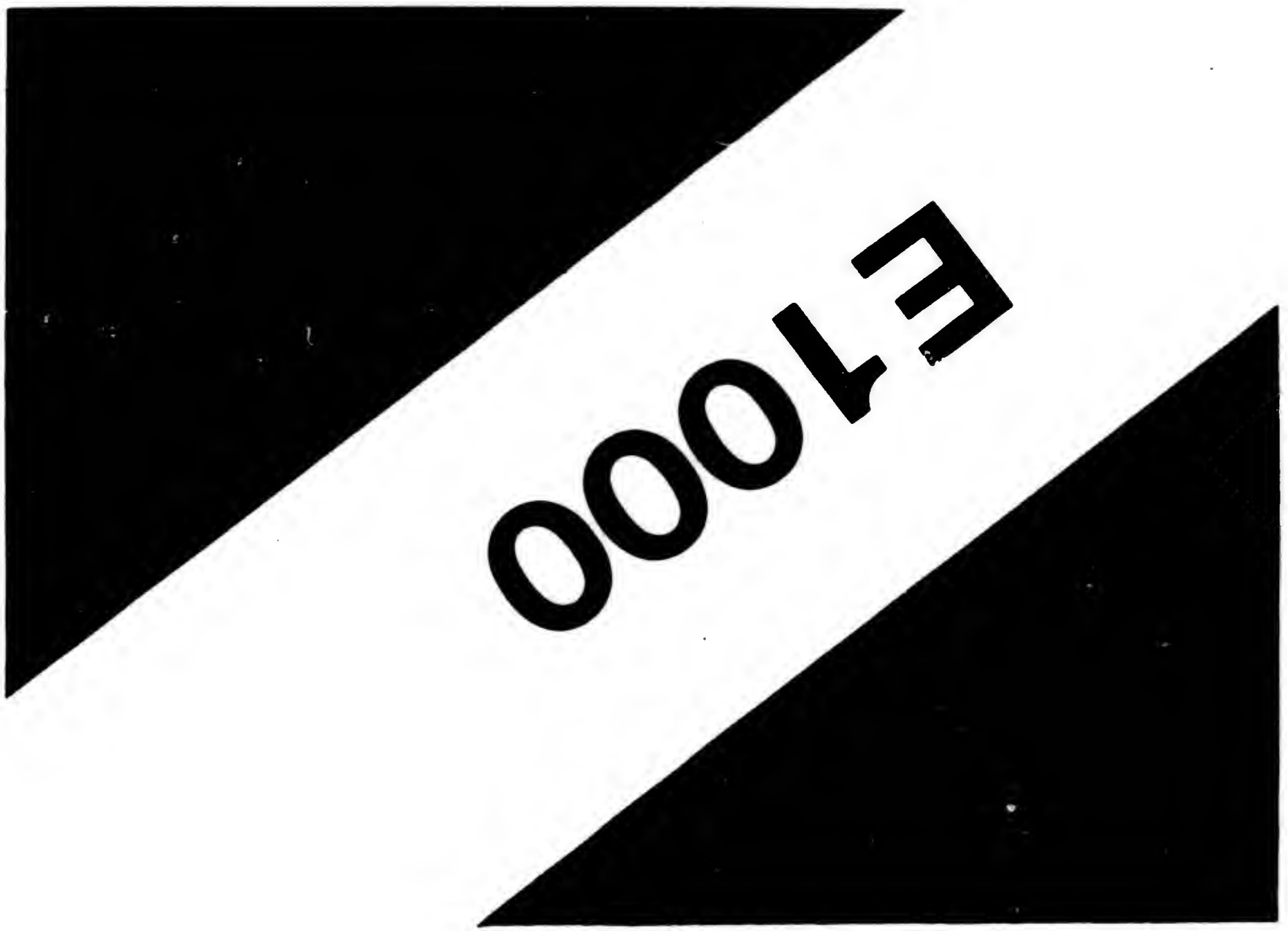
UETP MATRIX
KNOWN CUSTOMER SOFTWARE

Customer ordered this base software or license	UETP to be run				
	RSX11	RSTS	RT11	RSX11M+	
RSX11	X				
TRAX	X				
IAS	X				
TMS11	X				
RSTS/E		X			
CTS-500		X			
DSM11 (DEC STD. MUMPS)		X			
RT11			X		
CTS-300			X		
RSX11M PLUS					
RSX11M+				X	

5.1.2 Matrix to be used when Customer has not ordered an operating system software or license. This matrix is based on general RSX, RSTS/E and RT software system usage and limitations.

UETP MATRIX
NO SOFTWARE OR LICENSE ORDERED

Customer did not order any software or license	UETP to be run		
	RT11	RSX11	RSTS/E
System has ≤ 32KW of memory	X		
System has > 32KW but ≤ 64KW of memory		X	
System has > 64KW of memory			X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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE 10/6/80

TITLE PHASE III BACK UP DOCUMENTATION [illegible] (DLO)

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	NEW BACKUP	MA-40000-ML011			[illegible]	[illegible]

ENG	APPD	SIZE	CODE	NUMBER	REV
Tom Kenney	[signature]	A	SP	MA-E1000 -0-0	A

EN-01093-10-NP79 (492)

1.0 INTRODUCTION

1.1 This document details the steps necessary in generating an RSX11-M operating system and running the UETP, utilizing DYNAMIC LOADABLE DRIVERS (DLD).

1.2 Document Usage:

Section 8, Sample Sysgen, provided for those users unfamiliar with RSX11 DLD UETP.
Section 7, UETP Flow Chart, brief instructions for those users familiar with RSX11 DLD UETP.
Section 5, Special Instructions, further detail of section 7 and 8 usage.

2.0 REFERENCE DOCUMENTATION

2.1 "DLDSGN USERS GUIDE" by Ken Williams (Salem Systems Software Support Group, Real-Time Team).

2.2 RSX11-M System Generation and Management Guide, number AA-H625A-TC.

2.3 RSX11-M Utilities Manual, number AA-H268A-TC.

2.4 RSX11-M/M+ MCR Operations Manual, number AA-H263A-TC.

3.0 MINIMUM HARDWARE REQUIREMENTS

3.1 32KW of memory, memory management, and at least one supported system disk.

NOTE: RSX11-M DLD DOES NOT SUPPORT DUAL PORT DISK CONFIGURATIONS.

4.0 SOFTWARE REQUIRED

4.1 System image on magtape or disk.

4.1.1 For example: If you are using an RP06 as a system disk, you must use an RP06 image tape or an RP06 disk pack with the DLD on it.

4.2 "DSCS8" utility program on disk or magtape. "DSCS16" on magtape only.

4.2.1 You MUST use "DSCS16" if you are using a TS11, or any other tape device that uses a recording density of 1600 BPI exclusively .

NOTE: REFER TO APPENDIX "B" FOR DEVICES SUPPORTED BY EACH "DSC".

4.3 "BAD" utility program on disk or "BADSYS" utility program on magtape .

4.4 "DLD" software available from SALEM SYSTEMS SOFTWARE SUPPORT GROUP. (REAL-TIME TEAM)

5.0 SPECIAL INSTRUCTIONS

5.1 Ensure that the media used, matches the DISK type being used as the SYSTEM DISK.

NOTE: Magtape system image media is NOT BOOTABLE, therefore you must use one of the "DSC" utility programs to copy the image tape to the SYSTEM DISK.

5.2 Refer to section 7.1 pages 4 thru 8 for disk to disk sysgen flowchart.

5.3 Refer to section 7.2 pages 9 thru 14 for magtape to disk sysgen flowchart.

5.4 Refer to section 8.1 pages 16 thru 33 for disk to disk sample sysgen.

5.5 Refer to section 8.2 pages 34 thru 42 for magtape to disk sample sysgen.

6.0 SOFTWARE SET-UP INSTRUCTIONS

6.1 Ensure that the Distribution Media is protected from accidental erasure.

6.2 The system should be powered up with the CPU halted.

6.3 All turn-around connectors should be removed from any and all COMM. GEAR.

7.0 SYSGEN AND UETP FLOW CHARTS

7.1 RSX11M V3.2 DLD SYSGEN FROM DISK TO DISK

INSTALL DISTRIBUTION MEDIA IN DISK DRIVE AND BOOT

7.1.1

BADDISK
USE INDIRECT COMMAND FILE TO LOCATE BAD BLOCKS ON SYSTEM DISK. @[2,300]BADDISK

7.1.2

DSCS8/DSCS16
ASSIGN NON-STANDARD ADDRESSES AND VECTORS. COPY DISTRIBUTION MEDIA TO SYSTEM DISK. REFER TO PG.24 IN "DLD-SGN USERS GUIDE" AND APPENDIX IN THIS DOCUMENT. B00 [1,51]DSCS8 (or DSCS16)

REMOVE DISTRIBUTION MEDIA

7.1.3

BOOT SYSTEM DISK
HARDWARE BOOT THE SYSTEM DISK.

7.1.4

START DLD SYSGEN

TYPE @DLDSGN TO START SYSTEM GENERATION.

7.1.5

REBUILD DEVICE DRIVERS

REFER TO PG. 38 IN "DLDSGN USERS GUIDE" FOR PRE-BUILT DRIVER PARAMETERS. REBUILD ANY DRIVERS THAT DIFFER FROM LIST.

7.1.6

ENTER DEVICES THAT DID NOT NEED TO BE REBUILT IN 7.1.5

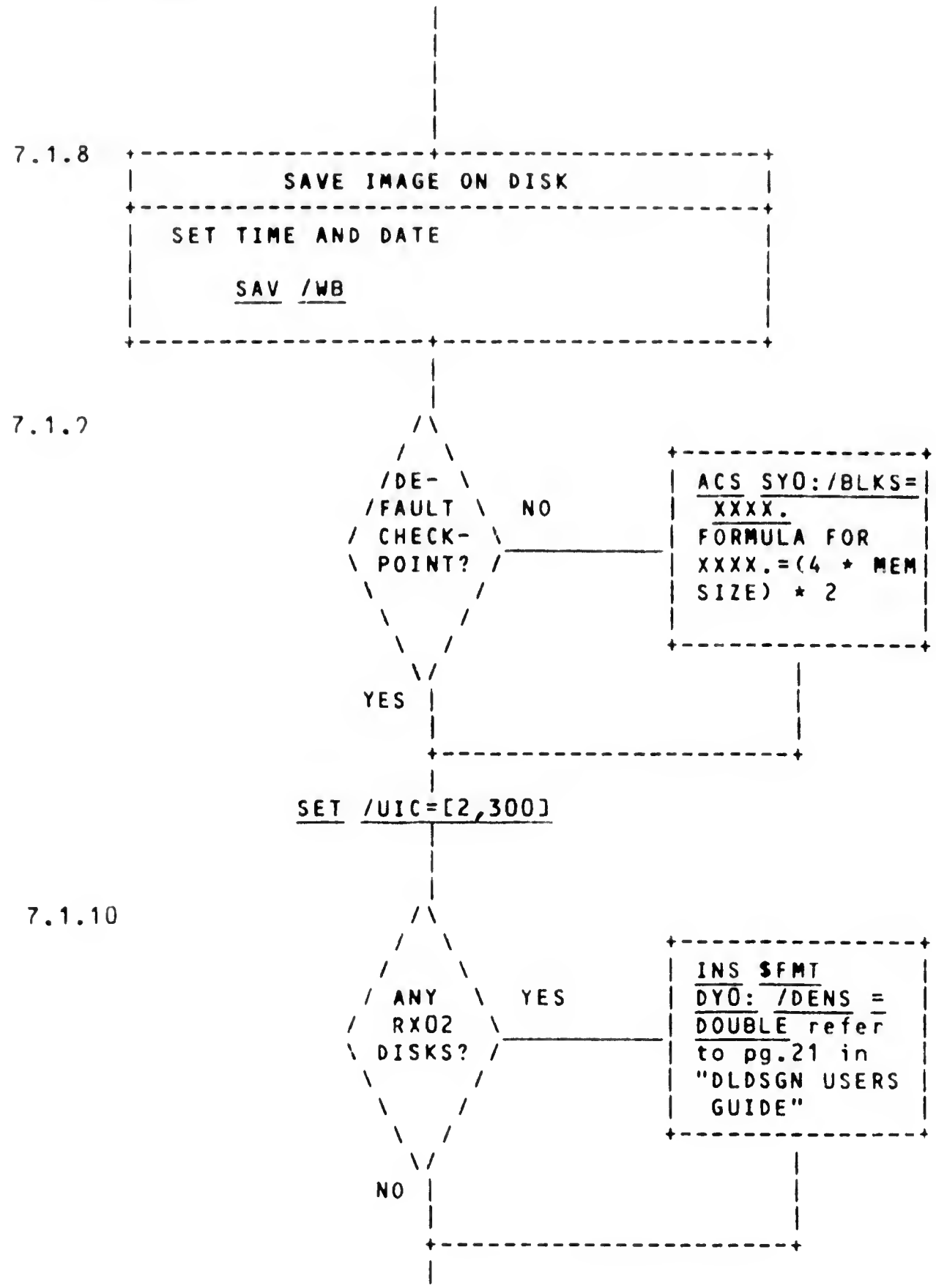
CONSULT CONFIGURATION SHEET FOR EXISTING DEVICES.

7.1.7

EDIT SYSVMR .CMD ?

YES → EDI

NO


7.1.8
SAVE IMAGE ON DISK
SET TIME AND DATE
SAV /WB
7.1.9
/DE- FAULT CHECK- POINT?
NO
ACS SYO:/BLKS=XXXX.
FORMULA FOR XXXX.=(4 * MEM SIZE) * 2
YES
SET /UIC=[2,300]
7.1.10
ANY RX02 DISKS?
YES
INS $FMT
DYO: /DENS = DOUBLE refer to pg.21 in "DLDSGN USERS GUIDE"
NO

7.1.11 ANY PUBLIC DISKS? YES → @BADDISK, @INIDISK; NO

7.1.12 **DELETE ERROR LOG**

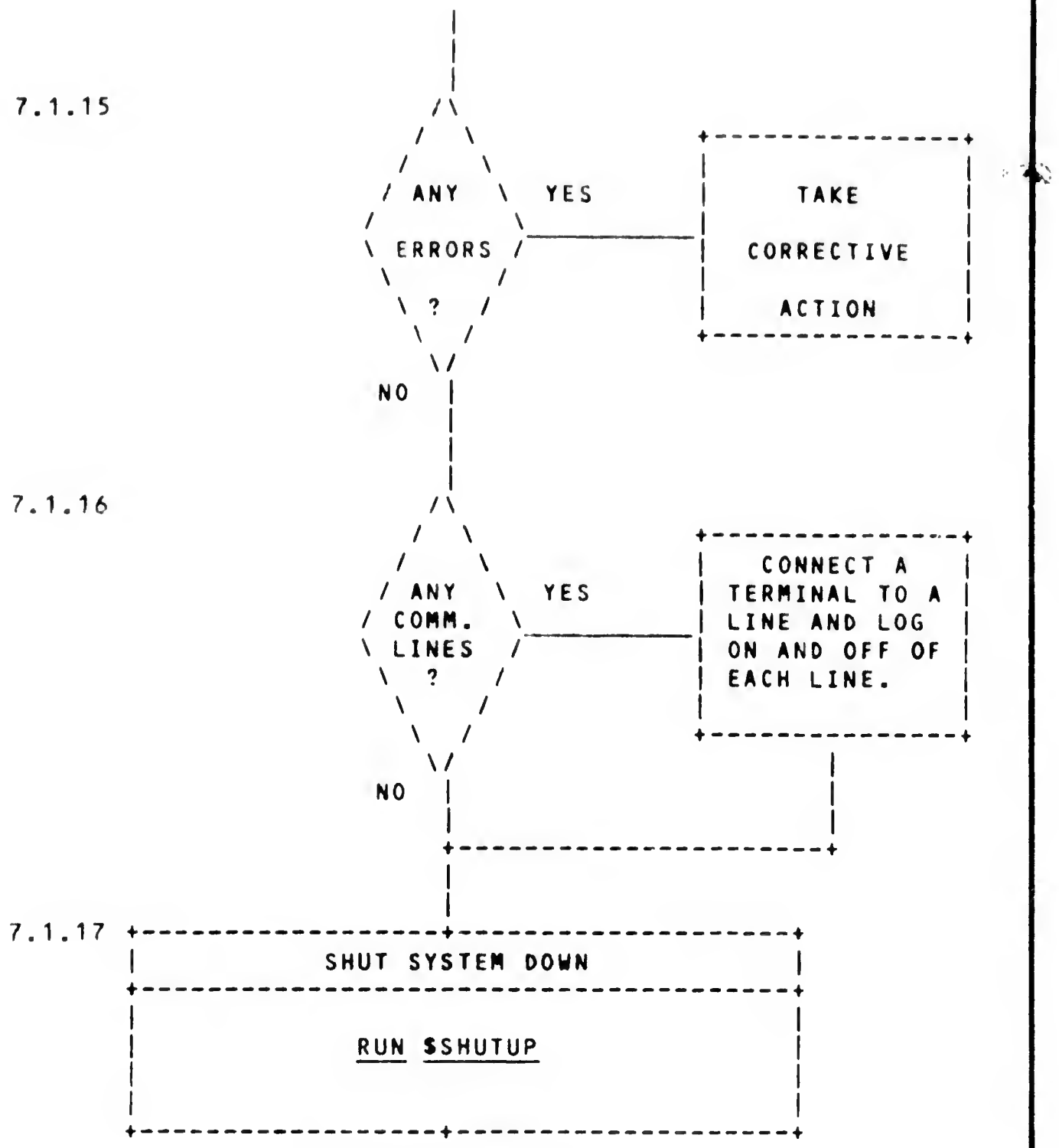
```
TYPE  ERF
 PIP TI: [1,6]*.*;*/DE
 RUN ERRLOG
```

7.1.13 **START U.E.T.P.**

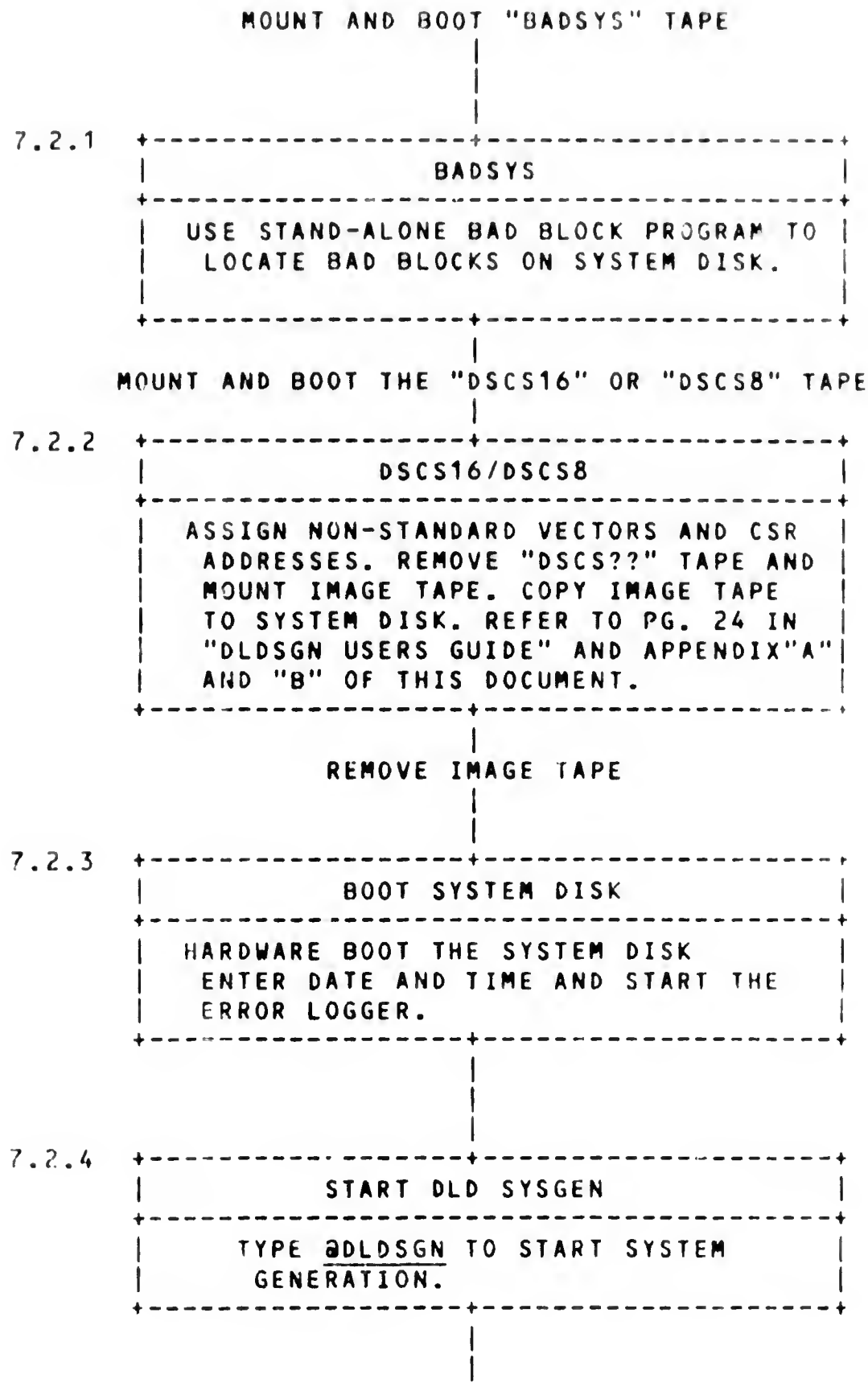
```
   TYPE @DLDUETP

 RUN U.E.T.P. FOR EIGHT HOURS OR TWO
  PASSES MINIMUM.
```

7.1.14 **CHECK FOR ERRORS**

```
IF U.E.T.P. HAS COMPLETED THE REQUEST-
 ED AMOUNT OF PASSES, TYPE :
   PIP TI:=[2,300]ERRLOG.LST
IF NOT, TYPE:
   SET /UIC=[1,6]
 THEN RUN "PSE" AND "SYE"
   refer to pg.27 in "DLDSGN USERS
 GUIDE"
```


7.1.15
ANY ERRORS ?
YES
TAKE CORRECTIVE ACTION
NO
7.1.16
ANY COMM. LINES ?
YES
CONNECT A TERMINAL TO A LINE AND LOG ON AND OFF OF EACH LINE.
NO
7.1.17
SHUT SYSTEM DOWN
RUN $SHUTUP

7.2 RSX11-M DLD V3.2 FOR TAPE TO DISK



7.2.5 REBUILD DEVICE DRIVERS

REFER TO PG. 38 IN "DLDSGN USERS GUIDE" FOR PRE-BUILT DRIVER PARAMETERS. REBUILD ANY DRIVERS THAT DIFFER FROM LIST.

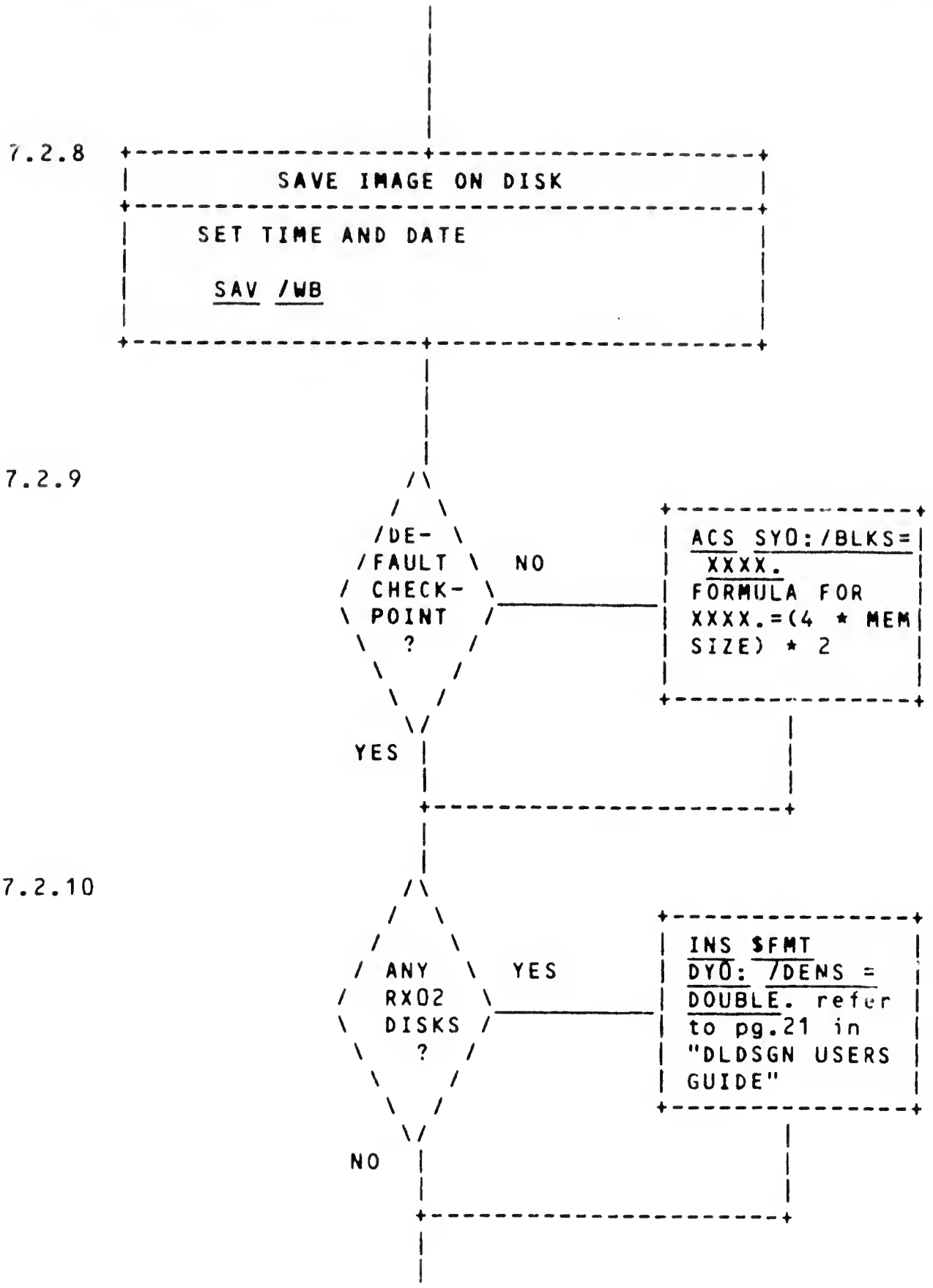
7.2.6 ENTER DEVICES THAT DID NOT NEED TO BE REBUILT IN 7.2.5

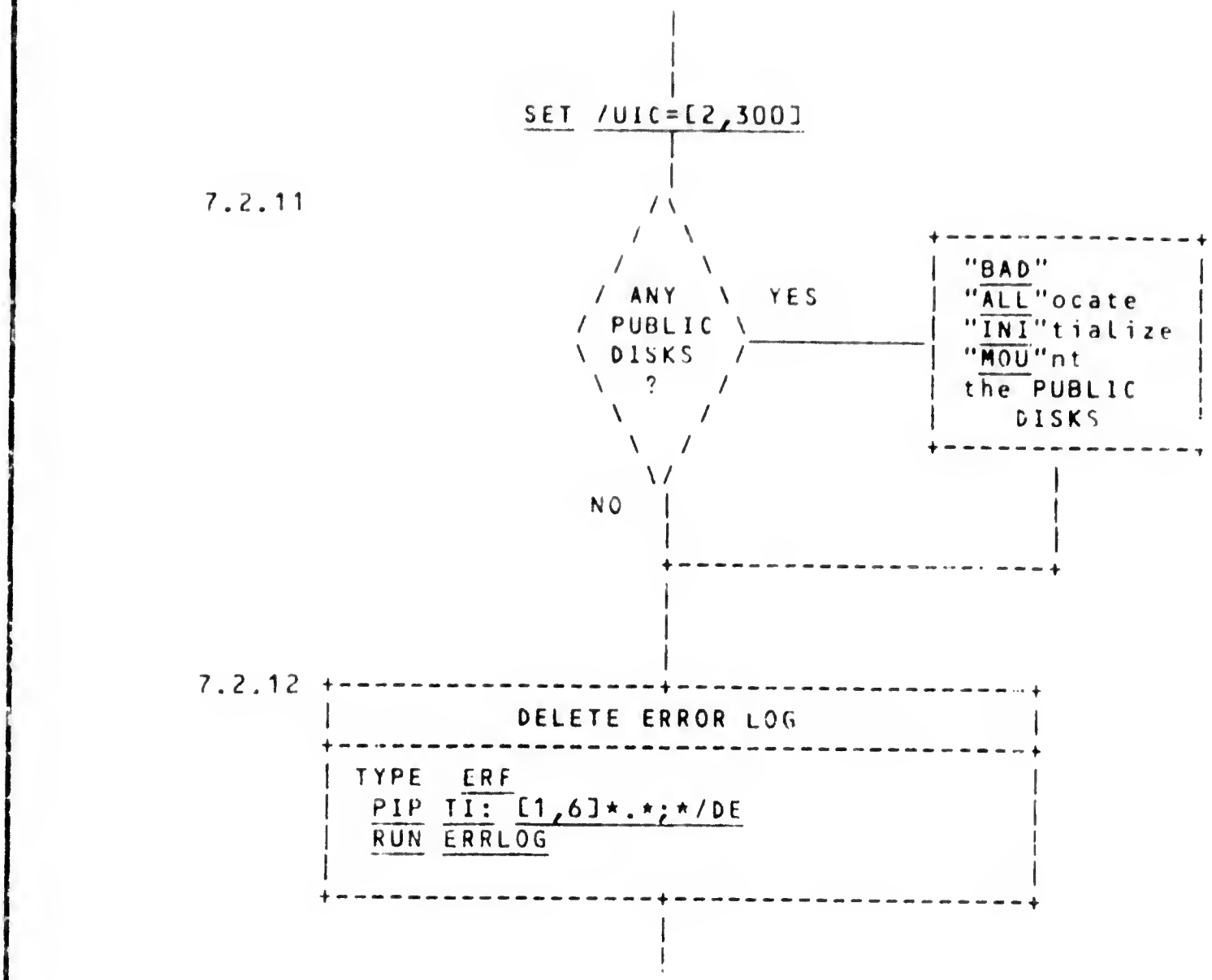
CONSULT CONFIGURATION SHEET FOR EXISTING DEVICES.

7.2.7 EDIT SYSVMR .CMD ?

YES → EDI

NO


7.2.8
SAVE IMAGE ON DISK
SET TIME AND DATE
SAV /WB
7.2.9
DE- FAULT CHECK- POINT ?
NO
ACS SY0:/BLKS= XXXX.
FORMULA FOR XXXX.=(4 * MEM SIZE) * 2
YES
7.2.10
ANY RX02 DISKS ?
YES
INS $FMT DY0: /DENS = DOUBLE. refer to pg.21 in "DLDSGN USERS GUIDE"
NO


SET /UIC=[2,300]
7.2.11
ANY PUBLIC DISKS ?
YES
"BAD"
"ALL"ocate
"INI"tialize
"MOU"nt
the PUBLIC
DISKS
NO
7.2.12
DELETE ERROR LOG
TYPE ERF
PIP TI: [1,6]*.*;*/DE
RUN ERRLOG

7.2.13 ANY DVS 11's TO TEST?

YES

MOUNT "DVS" TAPE.
FLX SY0: = MM0:*.*
@DVS
RUN U.E.T.P.

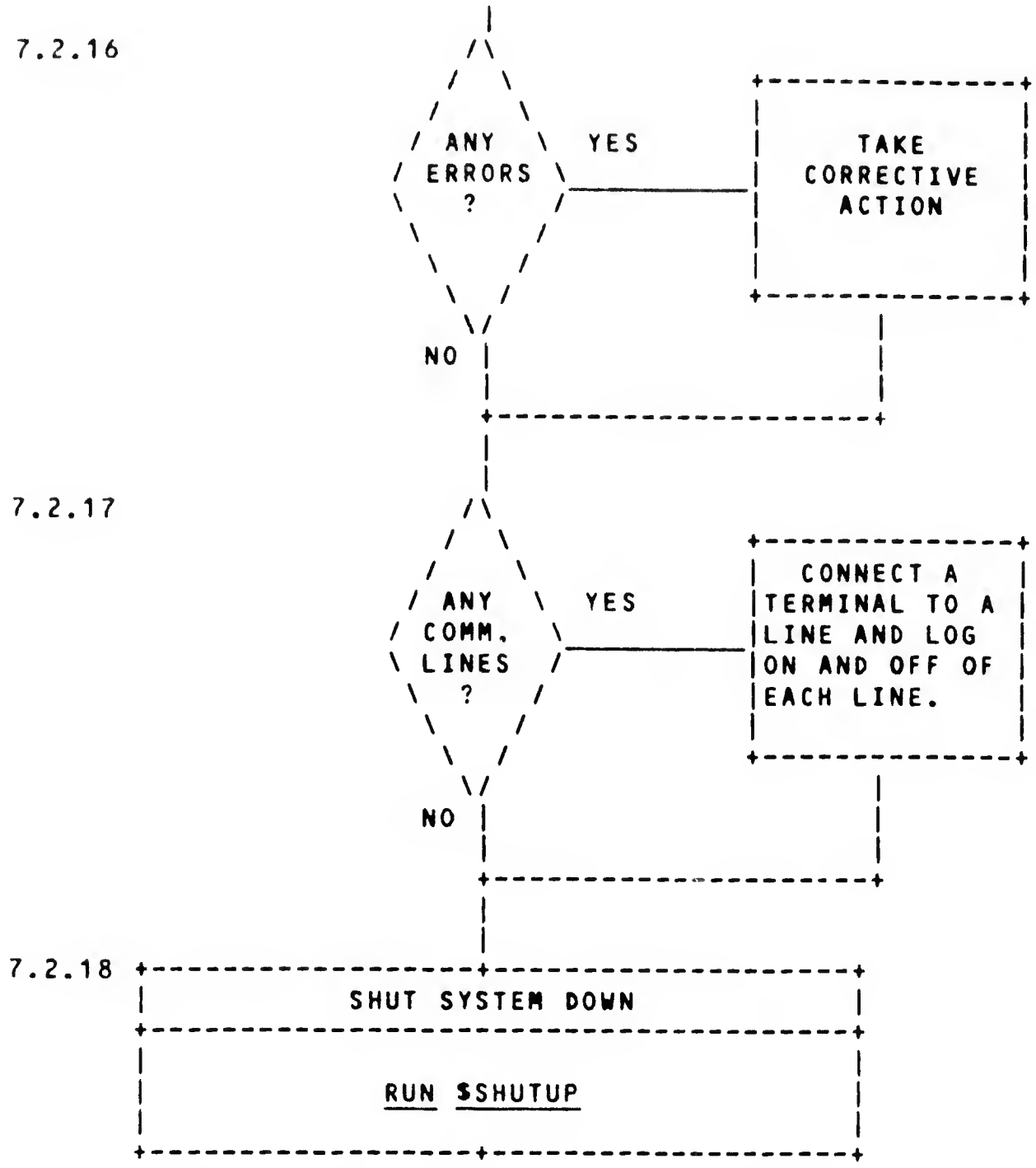
NO

7.2.14 START UETP

@DLDUETP
RUN U.E.T.P. FOR EIGHT HOURS OR TWO PASSES MINIMUM

7.2.15 CHECK FOR ERRORS

IF U.E.T.P. HAS COMPLETED THE REQUESTED AMOUNT OF PASSES, TYPE:
PIP TI:=[2,300]ERRLOG.LST
IF NOT, TYPE:
SET /UIC=[1,6]
THEN RUN "PSE" AND "SYE" refer to pg. 27 in "DLDSGN USERS GUIDE."


7.2.16
ANY ERRORS ?
YES
TAKE CORRECTIVE ACTION
NO
7.2.17
ANY COMM. LINES ?
YES
CONNECT A TERMINAL TO A LINE AND LOG ON AND OFF OF EACH LINE.
NO
7.2.18
SHUT SYSTEM DOWN
RUN $SHUTUP

8.0 SAMPLE SYSGENS AND UETP PRINTOUTS

8.1 This section starts on the next page. The text is printed with reduced character size and spacing due to space restrictions on the MANUFACTURING SPEC. paper.

8.2 These are SAMPLES ONLY, your particular SYSGEN may be different.

8.1 RSX11-M DLD SYSGEN FROM DISK TO DISK

NOTE: This example was generated for an 11/34, with 124KW of memory, 2 RL02 disk drives, 2 RX02 disk drives and 2 DZ11's. User responses are underlined. Explanatory comments are on the right hand margin.

```
@DL1 <CR>                                                    hardware boot the
                                                             distribution media

 RSX-11M V3.2 BL26    124K    MAPPED                         rsx identification
                                                             header
>RED DL1:=SY:
>RED DL1:=LB:
>MOU DL1:DLDBL26

@[1,2]DLDSTART.CMD
>* Please enter time and date (DD-MMM-YY HH:MM) [S]: <CR>    not necessary here


>TIM
08:35:52 25-MAR-80
>INS $BIGMAC/PAR=GEN
>INS $BIGTKB/PAR=GEN
>INS $ERL
>INS $ERF
>* Do you want to run the Errorlogger? [Y/N]:N <CR>         not necessary here


>@ <EOF>                                                     at this point the
                                                             operating system
                                                             waits for a response
                                                             from you
```

```
>@[2,300]BADDISK <CR>
```

[STEP 1]
this command file will allow you to check your disks for bad blocks

```
>;
>;
>* How many disks do you want to BAD [D R:1.-17. D:1.]: <CR>
>INS $BAD/TASK=...BA1
>* Disk to run BAD on [S R:3-5]: DL0 <CR>
```

disk mnemonics:
DB = RP04/05/06
DK = RK05
DL = RL01/02
DM = RK06/07
DR = RM02/03
DX = RX01
DY = RX02

```
>BA1 DL0:
>@ <EOF>
BAD — DL0: TOTAL BAD BLOCKS- 1.

>B00 [1,51]DSCS8 <CR>
```

[STEP 2]
refer to APPENDIX B for proper DSC to use. refer to APPENDIX A for device vectors and addresses. boot in the DSC program

```
RSX11S V2.2 BL26   DISK SAVE AND COMPRESS UTILITY V 3.0

DSCS8>DL0:/VEC=160 <CR>
```

assigns RL02 vector to 160

```
DSCS8>DL0:=DL1: <CR>
```

copies dist. media on DL1 to DL0

```
DSCS8>
```

refer to pg.24 in "DLDSGN USERS GUIDE" for more information on DSC.

```
@DL <CR>
```

[STEP 3]
hardware boot the system disk

```
  RSX-11M V3.2 BL26   124K   MAPPED
>RED DL:=SY:
>RED DL:=LB:
>MOU DL:DLDBL26
@[1,2]DLDSTART.CMD
```

```
>* Please enter time and date (DD-MMM-YY HH:MM) [S]: 08:37 25-MAR-80 <CR>    24 hr.  format
>TIM 08:37 25-MAR-80
>INS $BIGMAC/PAR=GEN
>INS $BIGTKB/PAR=GEN
>INS $ERL
>INS $ERF
>* Do you want to run the Errorlogger? [Y/N]:Y <CR>                          always "YES" during
                                                                             sysgen session
>RUN ERRLOG
>@ <EOF>
>
ERL -- ERROR LOG INITIALIZED



>@DLDSGN <CR>                                                               [STEP 4]
                                                                             this command starts
                                                                             the sysgen session

>TIM
08:25:51 25-MAR-80
>;
>; Dynamic Loadable Driver Sysgen.                                          Typing a <CR> in
                                                                             response to a
                                                                             question, results in
                                                                             a "NO" or the
                                                                             default answer for
                                                                             that question.
>;
>; By Ken Williams      2/29/80
>;
>; Dept:  Salem Manufacturing Product Support
>;
>SET /UIC=[1,54]
>* Is this an RL01 system? [Y/N]: <CR>
>* Does this system have the Floating Point Unit? [Y/N]: <CR>                consult sytems tech
>* Do you want long dialogue ? [Y/N]: <CR>
>PIP [11,10]RSXMC.MAC;*/DE/NM
>PIP [1,24]RSXBLD.CMD;*/DE/NM,RSX11M.OLB;*
>PIP [1,34]RSX11M.MAP;*/DE/NM
>PIP [11,10]/FO=[1,54]RSXMC.MAC
>PIP [1,24]/FO=[1,54]RSXBLD.CMD,RSX11M.OLB
>PIP [1,34]/FO=[1,54]RSX11M.MAP
>;
```

```
>;       Begin Peripheral Options.
>;
>* Expanded comments desired for peripheral options? [Y/N]: <CR>
>SET /UIC=[1,54]
>* Are you running on a system with a line printer? [Y/N]: <CR>
>* Assembly listing files desired? [Y/N]: <CR>
>* Task builder map(s) desired? [Y/N]: <CR>
>PIP [11,10]DLDMCO.MAC;*/DE/NM,DLDMC;*
>PIP [11,24]DLDASM.CMD;*/DE/NM
>PIP [1,24]DLDBLD.CMD;*/DE/NM,DLDLBR;*
>* Which device driver do you want to rebuild [S]: TT <CR>                [STEP 5]

>* Do you have any DH11's? [Y/N]: <CR>
>* Do you have any DJ11's? [Y/N]: <CR>
>* Do you have any DZ11's? [Y/N]:Y <CR>
>;
>; If you have an LA120 or LA180S, you must answer Yes to the next
>; question.
>;
>* Do you want form feeds passed directly to terminals? [Y/N]: <CR>
>;
>; Include console in the answer to the next question.
>;
>* Enter number of DL11 line interfaces [D R:1.-16. D:1.]: <CR>
>* Enter vector address of the first DL11 [O R:60-774 D:60]: <CR>
>* What is its CSR address? [O R:160000-177700 D:177560]: <CR>
>* Enter number of DZ11 asynchronous multiplexers [D R:1.-16. D:1.]: 2 <CR>
>* Do any of the lines require modem support? [Y/N]: <CR>
>* Enter vector address of the first DZ11 [O R:300-774]: 300 <CR>
>* What is its CSR address? [O R:160010-177700]: 160010 <CR>
>* How many lines does it have? [D R:1.-8. D:8.]: <CR>
>* Enter vector address of the next DZ11 [O R:300-774]: 310 <CR>
>* What is its CSR address? [O R:160010-177700]: 160020 <CR>
>* How many lines does it have? [D R:1.-8. D:8.]: <CR>
>* Which device driver do you want to rebuild [S]: <CR>
```

For an explanation of each question individually, press the <ESC> or <ALT> key in response to the question.

consult systems tech for device addresses and vectors.

type <CR> if you have no more drivers to be rebuilt.

```
>PIP [11,10]DLDMC.MAC/FO=[11,10]RSXMC.MAC,DLDMCO.MAC,RSXMCO.MAC
>SET /UIC=[11,24]
>TIM
08:27:52 25-MAR-80
>MAC @DLDASM
>TIM
08:29:20 25-MAR-80
>SET /UIC=[1,24]
>PIP [11,34]*.*/PU/NM
>TKB @[1,24]DLDBLD
>PIP [11,24]*.OBJ;*/DE/NM
>PIP [1,34]*.MAP/PU/NM
>SET /UIC=[1,54]

>* Do you have any Card Readers? [Y/N]: <CR>

>* Do you have any TA11 Cassettes? [Y/N]: <CR>
>* Do you have any RJP/RWP04/05/06's? [Y/N]: <CR>
>* Do you have any TU58's? [Y/N]: <CR>
>* Do you have any RF11's? [Y/N]: <CR>
>* Do you have any RK11/RK05's? [Y/N]: <CR>
>* Do you have any RK611/RK06/RK07's? [Y/N]: <CR>
>* Do you have any RP11/RPR02/RP03's? [Y/N]: <CR>
>* Do you have any RJ/RWM02/03's? [Y/N]: <CR>
>* Do you have any RJS/RWS03/04's? [Y/N]: <CR>
>* Do you have any TC11/TU56's? [Y/N]: <CR>
>* Do you have any RX11/RX01 Floppy's? [Y/N]: <CR>
>* Do you have any RX211/RX02 Floppy's? [Y/N]:Y <CR>
>* Do you have any LP11/LS11/LV11/LA180's? [Y/N]: <CR>
>* Do you have any TJU/TWU16/TE16/45/77's? [Y/N]: <CR>
>* Do you have any TS11/TS04'S? [Y/N]: <CR>
>* Do you have any TM11/TU10/TE10/TS03's? [Y/N]: <CR>
>* Do you have a PC11 (Paper Tape Reader/Punch)? [Y/N]: <CR>
>* Do you have a PR11 (Paper Tape Reader)? [Y/N]: <CR>
>;
>; The FCP which will be used is MIDDLE.
>;
>* Do you want to set up the terminals? [Y/N]:Y <CR>
>* Do you want to set up all the terminals the same? [Y/N]:Y <CR>
>;
>; Note: DZ11 lines must have both the receiver & the transmitter
>;       baud rates set up the same speed.
>;
>; Your first local terminal is TT1:
>; Your last local terminal is TT20:
```

[STEP 6]
if you have built a driver for each device on your system, you can hit <ESC> to bypass this section.

```
>* Do you want the default values? [Y/N]: <ESC>
>;
>; The default values are VT52, 80. characters per line,
>; 9600:9600 baud rate, and lower case enabled.
>;
>* Do you want the default values? [Y/N]:Y <CR>
>PIP [1,54]SYSVMR.CMD;*/DE/NM
>;
>; [1,54]SYSVMR.CMD will now be created.
>;
>INS $VMR
>PIP [1,54]SYSVMR.CMD=[200,200]TTY.CMD/AP
>SET /UIC=[1,54]
>* Enter size in K words for the system image? [D R:48.-124. D:48.]: <CR>
>PIP [1,54]RSX11M.SYS/NV/CO/BL:194.=[1,54]RSX11M.TSK
>* Do you wish to edit [1,54]SYSVMR.CMD? [Y/N]: <CR>
>;
>;
>; VMR is now being performed.
>;
>VMR @[1,54]SYSVMR.CMD
VMR -- INSTALLED TASKS MAY NO LONGER FIT IN PARTITION
SET /TOP=DRVPAR:-*
>;
>; The account UETP; password UETP; has been set up.
>;
>BOO RSX11M


RSX11M V3.2 BL26

>TIM 09:02 25-MAR-80 <CR>


>SAV /WB <CR>
```

type <ESC> if you want to see the default values

[STEP 7]
usual answer is "NO or <cr>. only answer "YES" if you want to change partition sizes,install additional tasks,etc..

normal warning

at this point the new executive is booted automatically,and waits for a response from you.

[STEP 8]
set the correct time and date

this command will save and boot the new system image.

```
 RSX-11M V3.2 BL26   124K   MAPPED
```

ensure memory size is correct.

```
>RED DL:=SY:
>RED DL:=LB:
>MOU DL:DLDBL26
>@[1,2]STARTUP
>* Please enter time and date (DD-MMM-YY HH:MM) [S]: <CR>
```

if you entered the correct time in step 8, it is not necessary to do so again.

```
>TIM
09:02:17 25-MAR-80
>SET /SYSUIC=[1,54]
>INS $BIGMAC /PAR=GEN
>INS $BIGTKB /PAR=GEN
>PIP SY:/FR

DL0: HAS 3773. BLOCKS FREE, 16707. BLOCKS USED OUT OF 20480.
LARGEST CONTIGUOUS SPACE = 2422. BLOCKS

>* Do you want the default checkpoint file size [992]? [Y/N]:Y
```

[STEP 9]
use default checkpoint file size, ONLY if the number of contiguous blocks is greater than the default size

```
>ACS SY:/BLKS=992.
>RUN ERRLOG
>BRO ALL:RSX11M IS NOW ON THE AIR !!!!!
ERL -- ERROR LOG INITIALIZED
>@ <EOF>
>
>SET /UIC=[2,300] <CR>
```

this is the account that U.E.T.P. resides in

```
>INS $FMT <CR>
```

[STEP 10]
this installs the format task

```
>FMT <CR>
```

this runs the format task

```
FMT>DY0:/DENS=DOUBLE <CR>

FMT>DY1:/DENS=DOUBLE <CR>
```

this tells the FMT task that you are formatting RX02's refer to pg. 21 in "DLDSGN USERS GUIDE".

```
^>^Z <CTRL Z>                                          this exits the FMT
                                                       task

>@BADDISK <CR>                                         [STEP 11]
                                                        check for bad
                                                       blocks on remaining
                                                       disks

>; Bad the Disk Command File
>;
>* How many disks do you want to BAD [D R:1.-17. D:1.]: 3 <CR>
>INS $BAD/TASK=...BA1
>INS $BAD/TASK=...BA2
>INS $BAD/TASK=...BA3
>* Device to run BAD on [S R:3-5]: DL1 <CR>
>BA1 DL1:
>* Device to run BAD on [S R:3-5]: DY0 <CR>
>BA2 DY0:
>* Device to run BAD on [S R:3-5]: DY1 <CR>
>BA3 DY1:
>@ <EOF>
BAD — DL1: TOTAL BAD BLOCKS- 0.
BAD — DY0: TOTAL BAD BLOCKS- 0.
BAD — DY1: TOTAL BAD BLOCKS- 0.

>@INIDISK <CR>                                         [STEP 12]
                                                       this command file
                                                       allows you to
                                                       initialize the
                                                       remaining disks

>; Disk Initializing Command file
>;
>; Please enter the name of the disk to be initialized
>; type a <RETURN> when all disks have been entered.
>* what disk is to be initialized [DDN:] [S]: DL1 <CR>
>ALL DL1:
>INI DL1:SCRATCH/INDX=BEG/BAD=AUTO]
>* what disk is to be initialized [DDN:] [S]: DY0 <CR>
>ALL DY0:
>INI DY0:SCRATCH/INDX=BEG/BAD=[AUTO]
>* what disk is to be initialized [DDN:] [S]: DY1 <CR>
>ALL DY1:
>INI DY1:SCRATCH/INDX=BEG/BAD=[AUTO]
>* what disk is to be initialized [DDN:] [S]: <CR>
>;
>;* Do you want to run a quick pass of IOX (the I/O exerciser)
>* on the disks that have just be initialized ? [Y/N]:Y <CR>          optional
>* How many minutes do you want it to run [0 R:0-5 D:1]: <CR>
>* Do you want to run IOX on any other devices? [Y/N]:Y <CR>
>; Please enter the name of the device to be tested;
>; type a <RETURN> when all the devices have been entered.
>* What device is to be tested [S]: DL0 <CR>
>* What device is to be tested [S]: <CR>
```

```
MOU DL1:/OVR                                                    the disks are
                                                                mounted
                                                                automatically.

>MOU DY0:/OVR
>MOU DY1:/OVR
>MOU DL0:/OVR
>IOX @DISKTEST
IOX — UNIT ALREADY CONFIGURED
IOX — UNIT ALREADY CONFIGURED

IOX — SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 08:41:01
  TIME — RUN: 1 MIN.   ELAPSED: 1 MIN.   REMAINING: 0 MIN.
  DL0: — 1,992. REQUESTS TOTALING 1,992. BLOCKS WITH NO ERRORS
  DL1: — 1,985. REQUESTS TOTALING 1,985. BLOCKS WITH NO ERRORS
  DY0: —   546. REQUESTS TOTALING   546. BLOCKS WITH NO ERRORS
  DY1: —   492. REQUESTS TOTALING   492. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 199. ITERATIONS

A C C U M U L A T E D   T O T A L S :
- - - - - - - - - - -   - - - - - - -
  TIME — RUN: 1 MIN.   ELAPSED: 1 MIN.   REMAINING: 0 MIN.
  DL0: — 1,993. REQUESTS TOTALING 1,993. BLOCKS WITH NO ERRORS
  DL1: — 1,985. REQUESTS TOTALING 1,985. BLOCKS WITH NO ERRORS
  DY0: —   546. REQUESTS TOTALING   546. BLOCKS WITH NO ERRORS
  DY1: —   492. REQUESTS TOTALING   492. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 199. ITERATIONS


>DMO DL1:                                                       the disks are
>DMO DY0:                                                       dismounted auto-
>DMO DY1:                                                       matically.
>DMO DL0:
>;
>@ <EOF>                                                        at this point the
                                                                operating system
                                                                waits for a response
                                                                from you.
```

```
>@DLDUETP                                                    [STEP 13]
                                                             this will start the
                                                             D.E.T.P. session
>;
>;      ********.**********************> ********************
>;      *                                                    *
>;      *   RSX-11M INSTALLATION VERIFICATION PACKAGE        *
>;      *                                                    *
>;      ******************************************************
>;
>SET /UIC=[2,300]
>RUN ERRLOG
>
>;
>* DO YOU WISH TO RUN RMDEMO? [Y/N]: <CR>
>;
>* ENTER VERSION OF UETP TO BE RUN (SAM, SUB, MFG, ENG) [S]: MFG <CR>    always MFG
>* ENTER UNIT NUMBER OF TERMINAL [S]: 0 <CR>
>;
>;
>* ENTER INPUT DEVICE (DDNN) OR <CR> [S]: <CR>                  press <cr> if UETP
                                                                resides on system
                                                                disk.
>;
>;
>;
>;              **** NOTE ****
>;
>; TEST MEDIA MUST BE LOADED ON ALL TAPE AND DISK DRIVES.  USE SCRATCH TAPES
>; AND FILES-11 FORMAT DISKS.
>;
>; ALL MAGTAPES BEING TESTED ARE OVER-WRITTEN.  THE DISKS ARE
>; TESTED WITH FILE-STRUCTURED I/O WITH NO NEGATIVE EFFECT ON DATA
>; OR STRUCTURE.
>;
>; BEFORE PERFORMING THE FILE-STRUCTURED I/O TEST, ALL UNMOUNTED
>; DISKS ARE MOUNTED AUTOMATICALLY.
>;
>* DO YOU NEED TO INITIALIZE ANY DISKS? [Y/N]: <CR>              if you forgot to
                                                                INIT any disks, type
                                                                "YES".
>;
>TIM
09:10:31 25-MAR-80
```

```
>;ONE COMPLETE PASS OF THIS UETP WILL TAKE 4 HOURS
>;
>* HOW MANY PASSES DO YOU WISH TO RUN [D R:1.-6. D:1.]: 2 <CR>
>;
>;THE 2 PASS(ES) YOU HAVE SELECTED, WILL TAKE 8 HOURS TO RUN.
>;
>; NEEDED UTILITIES WILL BE INSTALLED NOW.
>; **********
>; ************************************************************
>PIP TAILOR.DAT=DEVM.SAM/AP
>MAC DEFINE=LB:[11,10]DLDMC.MAC/PA:1,SY:[2,300]DEFINE
>TKB DEFINE/PR/CP=DEFINE,LB:[1,54]RSX11M.STB,[1,1]EXELIB/LB
>INS DEFINE/TASK=DEFINE
>PIP *.*/PU
>RUN DEFINE
>;
>;START OF UETP PASS #1
>;
>;
>;
>;       * CPU-BOUND LOAD TEST *
>;
>INS DUMMY/TASK=DUM00/PRI=40.
>;
>INS LOGGER/TASK=LOG00
>INS QTRUN /TASK=QTR00
>RUN DUM00
>;
>; FOR THE NEXT FEW MINUTES A NUMBER OF COMPUTE-BOUND TASKS WILL BE
>; EXERCISING THE MEMORY, THE MULTI-TASKING CAPABILITIES OF THE
>; SYSTEM AND, IF INCLUDED IN THIS SYSTEM, THE ROUND-ROBIN SCHEDULER,
>; THE SHUFFLER AND CHECKPOINTING.  THE ACTION OF THESE LAST THREE
>; FEATURES CAN BE SEEN ON THE RMDEMO SCREEN.  IF THE SYSTEM IS
>; PERFORMING PROPERLY, ALL OF THE "GEN" PARTITION IS USED AND THE "QT"
>; TASKS ARE SHARING SYSTEM RESOURCES IN A MANNER CONSISTENT
>; WITH THE FEATURES AVAILABLE.  NOTE THAT CHECKPOINTING IS DISABLED
>; FOR THE SECOND HALF OF THE TEST.
>;
>;       *** THIS TEST RUNS FOR A MAXIMUM OF 120. MINUTES ***
>;
>RUN QTR00
>
>TIM
09:11:27 25-MAR-80
>INS NUL2/TASK=QT0000
>INS NUL2/TASK=QT0100
>INS NUL2/TASK=QT0200
>INS NUL2/TASK=QT0300
```

at least 2 passes for minimum MAST requirements

AT THIS POINT THE U.E.T.P. WILL RUN UNATTENDED FOR 2 PASSES OR 8 HOURS.

```
>;      >>>>>> THE LOAD TEST IS RUNNING <<<<<<
>TIM
11:11:22 25-MAR-80
>REM QT0000
>REM QT0100
>REM QT0200
>REM QT0300
>;
>;       * TEST COMPLETED *
>;
>;
>;
>;       * SYSTEM I/O EXERCISER *
>;
>; THE FOLLOWING DEVICES HAVE BEEN GENERATED INTO YOUR SYSTEM.  THOSE
>; LISTED AS "OFFLINE" ARE NOT PHYSICALLY PRESENT AND ARE NOT
>; TESTED.  INDIVIDUAL MAG TAPE, DEC TAPE AND RK05 UNITS CAN
>; ERRRONEOUSLY BE SHOWN AS ONLINE WHEN THE CONTROLLER IS ONLINE.
>; THEY ARE TESTED AND THE TEST FAILS AFTER SEVERAL MINUTES
>; OF ERROR MESSAGES.
>;
>DEV
DL0:      PUBLIC MOUNTED LOADED LABEL=RSX11MPBL6 TYPE=RL02
DL1:      LOADED TYPE RL02
DY0:      LOADED
DY1:      LOADED
CO0:      TT0: LOADED
TT0:      LOADED
TT1:      LOADED
TT2:      LOADED
TT3:      LOADED
TT4:      LOADED
TT5:      LOADED
TT6:      LOADED
TT7:      LOADED
TT10:     LOADED
TT11:     LOADED
TT12:     LOADED
TT13:     LOADED
TT14:     LOADED
TT15:     LOADED
TT16:     LOADED
TT17:     LOADED
TT20:     LOADED
NL0:      LOADED
RD0:      LOADED
TI0:
CL0:      TT0:
LB0:      DL0:
SY0:      DL0:
>;
```

```
>;
>; IF ANY DRIVERS ARE UNLOADED, THEY WILL BE LOADED NOW.
>;
>; **********
>; ************************************************************
>INS $IOX/TASK=...SIO
>;
>MOU DL1:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DL1:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = □
ACP NAME   = F11ACP
>MOU DY0:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DY0:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = □
ACP NAME   = F11ACP
>MOU DY1:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DY1:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = □
ACP NAME   = F11ACP
>;
```

```
>;  THE SYSTEM I/O EXERCISER WILL RUN FOR 120 MINUTES
>;
>TIM
11:12:12 25-MAR-80
>SIO @IOXCNF

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 11:42:14
  TIME -- RUN: 30 MIN.   ELAPSED: 30 MIN.   REMAINING: 90 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 12:12:16
  TIME -- RUN: 30 MIN.   ELAPSED: 60 MIN.   REMAINING: 60 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 12:42:18
  TIME -- RUN: 30 MIN.   ELAPSED: 90 MIN.   REMAINING:30 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 13:12:20
  TIME -- RUN: 30 MIN.   ELAPSED: 120 MIN.   REMAINING: 0 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

A C C U M U L A T E D   T O T A L S :
- - - - - - - - - - - -   - - - - - - -
  TIME -- RUN: 120 MIN.   ELAPSED: 120 MIN.   REMAINING: 0 MIN.
  DL0: -- 103,692. REQUESTS TOTALING 103,692. BLOCKS WITH NO ERRORS
  DL1: -- 100,136. REQUESTS TOTALING 100,136. BLOCKS WITH NO ERRORS
  DY0: -- 41,016. REQUESTS TOTALING 41,016. BLOCKS WITH NO ERRORS
  DY1: -- 41,016. REQUESTS TOTALING 41,016. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 26,680. ITERATIONS
```

```
>REM SIO
>TIM
13:12:54 25-MAR-80
>;
>;        * TEST COMPLETED *
>;
>;
>;END OF UETP PASS #1
>;
>;
>;
>;START OF UETP PASS #2
>;
>;
>;
>;        * CPU-BOUND LOAD TEST *
>;
>RUN DUM00
>;
>;        *** THIS TEST RUNS FOR A MAXIMUM OF 120. MINUTES ***
>;
>RUN QTR00
>
>TIM
13:13:11 25-MAR-80
>INS NUL2/TASK=QT0000
>INS NUL2/TASK=QT0100
>INS NUL2/TASK=QT0200
>INS NUL2/TASK=QT0300
>;       >>>>>> THE LOAD TEST IS RUNNING <<<<<<
>TIM
15:13:22 25-MAR-80
>REM QT0000
>REM QT0100
>REM QT0200
>REM QT0300
>;
>;        * TEST COMPLETED *
>;
```

```
>;       * SYSTEM I/O EXERCISER *
>;
>; IF ANY DRIVERS ARE UNLOADED, THEY WILL BE LOADED NOW.
>;
>; **********
>; ************************************************************
>INS $IOX/TASK=...SIO
>;
>MOU DL1:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DL1:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = []
ACP NAME   = F11ACP
>MOU DY0:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DY0:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = []
ACP NAME   = F11ACP
>MOU DY1:/OVR/VI
MOUNT -- VOLUME INFORMATION --
CLASS      = FILES 11
DEVICE     = DY1:
LABEL      = SCRATCH
UIC        = [1,1]
VOL PRO    = [RWED,RWED,RWED,RWED]
FILE PRO   = [RWED,RWED,RWED,R]
CHAR       = []
ACP NAME   = F11ACP
>;
>;  THE SYSTEM I/O EXERCISER WILL RUN FOR 120 MINUTES
>;
>TIM
15:13:57 25-MAR-80
>SIO @IOXCNF
SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 15:43:59
  TIME -- RUN: 30 MIN.   ELAPSED: 30 MIN.   REMAINING: 90 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS
```

```
SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 16:14:01
  TIME -- RUN: 30 MIN.   ELAPSED: 60 MIN.   REMAINING: 60 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 16:44:03
  TIME -- RUN: 30 MIN.   ELAPSED: 90 MIN.   REMAINING: 30 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

SIO -- SUMMARY OF EXERCISER ACTIVITY AT 25-MAR-80 17:14:05
  TIME -- RUN: 30 MIN.   ELAPSED: 120 MIN.   REMAINING: 0 MIN.
  DL0: -- 25,923. REQUESTS TOTALING 25,923. BLOCKS WITH NO ERRORS
  DL1: -- 25,034. REQUESTS TOTALING 25,034. BLOCKS WITH NO ERRORS
  DY0: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  DY1: -- 10,254. REQUESTS TOTALING 10,254. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 5,920. ITERATIONS

A C C U M U L A T E D   T O T A L S :
- - - - - - - - - - -   - - - - - - -
  TIME -- RUN: 120 MIN.   ELAPSED: 120 MIN.   REMAINING: 0 MIN.
  DL0: -- 103,692. REQUESTS TOTALING 103,692. BLOCKS WITH NO ERRORS
  DL1: -- 100,136. REQUESTS TOTALING 100,136. BLOCKS WITH NO ERRORS
  DY0: -- 41,016. REQUESTS TOTALING 41,016. BLOCKS WITH NO ERRORS
  DY1: -- 41,016. REQUESTS TOTALING 41,016. BLOCKS WITH NO ERRORS
  IDLE-LOOP COUNT: 26,680. ITERATIONS


>REM SIO
>TIM
17:14:23 25-MAR-80

>;
>;        * TEST COMPLETED *
>;
>;
>;END OF UETP PASS #2
>;
>;>;
```

```
>;
>PIP *.DAT;*/DE
>;
>; IF ANY ERRORS HAVE BEEN LOGGED BY ERROR LOGGER, WHEN THE COMMAND FILE
>; EXITS YOU SHOULD PRINT [2,300]ERRLOG.LST AND INVESTIGATE THE ERRORS.
>;
>ERF
ERF -- REQUESTED "ERRLOG" TO STOP LOGGING
>PSE SY:=SY:
ERL -- LOGGING ENDED AFTER 0 ERRORS
>SYE SY:=SY:/-SP
SYE -- 1. PAGES IN REPORT
>;
>RUN ERRLOG
ERL -- ERROR LOG INITIALIZED
>
>;
>;
>;
>; *'**********************************************************************
>;
>TIM
17:14:53 25-MAR-80
>;
>;                          *** END OF RSX-11M   INSTALLATION VERIFICATION ***
>;
>; **********************************************************************
>
>@ <EOF>
>
>PIP TI:=[2,300]ERRLOG.LST <CR>
```

[STEP 14]
type this to see any errors that have been logged. further information on the ERROR LOGGER can be found on page 27 of the "DLDSGN USERS GUIDE".

8.2 RSX11-M DLD SYSGEN - MAGTAPE TO DISK

NOTE:
This example was generated on an 11/70, with Floating Point, 640K words of MEMORY, a TE16 magtape, an RP06 disk drive and no comm. devices.
User responses are underlined. Explanatory comments on right margin.

```
RSX11S V2.1 BL22     BAD BLOCK LOCATOR
```

[STEP 1]
mount and boot "BADSYS" tape

```
BAD>DB0:/LI/CSR=176700/VEC=254/WCHK <CR>
```

refer to pg. 23 in "DLDSGN USERS GUIDE" for more info. on "BAD".

```
BAD -- BAD BLOCK FOUND - LBN= 1292.

BAD -- TOTAL NO. OF BAD BLOCKS = 1.

BAD>
```

remove "BADSYS" tape.

```
RSX11S V2.2 BL26D DISK SAVE AND COMPRESS UTILITY V 3.0
```

[STEP 2]
refer to APPENDIX B for proper "DSC" to use. refer to APPENDIX A for device addresses and vectors.
mount and boot a "DSC" tape.

```
DSCS16>MM0: /VEC=224 <CR>
DSCS16>DB0: /VEC=254 <CR>
```

assigns vector add. to devices

```
DSCS16>DB0:=MM0: <CR>
```

copies image tape to disk

```
DSC -- *WARNING* 59-DB0:
```

refer to pg. 24 in "DLDSGN USERS GUIDE" for more info. on "DSC".

```
DSCS16>
```

```
 RSX11M V3.2 BL26   124K   MAPPED
```

[STEP 3]
hardware boot the system disk.

```
>RED DB:=SY:
>RED DB:=LB:
>MOU DB:DLDBL26
>@DB:[1,2]STARTUP
>* Please enter time and date ( DD-MMM-YY HH:MM ) [S]: 9-JUN-80 11:06<CR>  24 hr. time format
>TIM 9-JUN-80 11:06
>INS $CDA
>INS $BIGMAC/PAR=GEN
>INS $BIGTKB/PAR=GEN
>INS $ERL
>INS $ERF
>RUN ERRLOG
>@ <EOF>
ERL -- ERROR LOG INITIALIZED


>@DLDSGN <CR>
```

[STEP 4]
this command starts the sysgen session.

```
>TIM
11:06:13 09-JUN-80
>;
>; Dynamic Loadable Driver Sysgen.
```

typing a <CR> in response to a query, results in a "NO " or the default answer for that query.

```
>;
>; By Ken Williams      9/10/79
>;
>; Dept:  Salem Manufacturing Product Support
>;
>SET /UIC=[1,54]
>* Is this an 11/70 system? [Y/N]: Y <CR>
>* Does this system have the Floating Point Unit? [Y/N]: Y <CR>
```

consult systems tech.

```
>INS $LBR
>INS $PIP
>INS $EDI
>* Do you want long dialogue ? [Y/N]: <CR>
```

for an explanation of each question individually, press the <esc> or <alt> key in response to the question.

```
>PIP [11,10]RSXMC.MAC;*/DE/NM
>PIP [1,24]RSXBLD.CMD;*/DE/NM,RSX11M.OLB;*
>PIP [1,34]RSX11M.MAP;*/DE/NM
>PIP [11,10]/FO=[1,57]RSXMC.MAC
>PIP [1,24]/FO=[1,57]RSXBLD.CMD,RSX11M.OLB
>PIP [1,34]/FO=[1,57]RSX11M.MAP
PIP -- NO SUCH FILE(S)
SY0:[1,57]RSX11M.MAP
>;
>;       Begin Peripheral Options
>;
>* Expanded comments desired for peripheral options? [Y/N]: <CR>
>SET /UIC=[1,54]
>* Are you running on a system with a line printer? [Y/N]: <CR>
>* Assembly listing files desired? [Y/N]: <CR>
>* Task builder map(s) desired? [Y/N]: <CR>
>PIP [11,10]DLDMC0.MAC;*/DE/NM,DLDMC;*
>PIP [11,24]DLDASM.CMD;*/DE/NM                                  [STEP 5]
                                                                consult systems tech
                                                                for vectors and
                                                                addresses.

>PIP [1,24]DLDBLD.CMD;*/DE/NM,DLDBDR;*
>* Which device driver do you want to rebuild [S]: DB <CR>
>* How many RJ/RWP04/5/6 disk pack cont. have you [D R:0.-16. D:1.]: <CR>
>* Enter vector address of the first RJ/RWP04-05-06 [O R:60-774 D:254]: <CR>
>* What is its CSR address? [o R:160000-177700 D:176700]: <CR>
>* How many drives does it have? [D R:1.-8. D:1.]: <CR>
>* Enter physical unit number of the first drive [O D:0]: <CR>
>* Is contr. 0 unit 0 an RP04 or RP05? [Y/N]: <CR>
>* Which device driver do want to rebuild [S]: MM <CR>
>* How many TJ/TWU16-45 magtape cont. do you have [D R:0.-16. D:1.]: <CR>
>* Enter vector address of the first TJ/TWU16-45 [O R:60-774 D:224]: <CR>
>* What is its CSR address? [O R:160000-177700 D:172440]: <CR>
>* How many drives does it have? [D R:1.-8. D:1.]: 2 <CR>
>* Enter physical unit number of the TM03 formatter [O D:0]: <CR>
>* Which device driver do you want to rebuild [S]: <CR>          press <CR> if there
                                                                are no more drivers
                                                                to be rebuilt

>PIP [11,10]DLDMC.MAC/FO=[11,10]RSXMC.MAC,DLDMC0.MAC,RSXMC0.MAC
>PIP [1,24]DLDLBR.CMD=[1,24]*.LBR
>PIP [1,24]*.LBR;*/DE/NM
>SET /UIC=[11,24]
```

```
>TIM
11:09:02 09-JUN-80
>MAC @DLDASM
>TIM
11:09:28 09-JUN-80
>SET /UIC=[1,24]
>PIP [11,34]*.*/PU/NM
>LBR @[1,24]DLDLBR
MODULE "DBTAB " REPLACED

MODULE "MMTAB " REPLACED

>TKB @[1,24]DLDBLD
>PIP [11,24]*.OBJ;*/DE/NM
>PIP [1,34]*.MAP/PU/NM
>SET /UIC=[1,54]
>SET /UIC=[1,57]
>* Do you have any Card Readers? [Y/N]: <esc>
```

[STEP 6]
if you have built a driver for each device on your system, you can press <esc> to bypass this section.

```
>;
>; The FCP which will be used is MIDDLE.
>;
>PIP [1,57]SYSVMR.CMD;*/DE/NM
>;
>; [1,57]SYSVMR.CMD will now be created.
>;
>INS $VMR
>SET /UIC=[1,57]
>*  Enter size in K words for the system image [D R:48.-124. D:48.]: <CR>
>PIP [1,57]RSX11M.SYS/NV/CO/BL:498.=[1,57]RSX11M.TSK
>* Do you wish to edit [1,57]SYSVMR.CMD? [Y/N]: <CR>
```

[STEP 7]
usual answer is "NO "or <CR>. only answer "YES" if you have to change partition sizes, install additional tasks, etc.

```
;>
>; VMR is now being performed.
>;
>VMR @[1,57]SYSVMR.CMD
VMR -- INSTALLED TASKS MAY NO LONGER FIT IN PARTITION
```

normal warning - disregard at this time.

```
SET /TOP=DRVPAR:-*
>;
>; Don't forget to create an account file with $ACNT.
>;
>TIM
11:12:21 09-JUN-80
>;
>;
>BOO RSX11M
```

at this point, the new executive is booted automatically and waits for a response from you.

```
RSX11M V3.2 BL26
```

```
>TIM 11:14 09-JUN-80 <CR>
```

[STEP 8] set the correct time and date

```
>SAV . SY <CR>
```

this command will save and boot the new system image.

```
  RSX-11M V3.2 BL26   640K   MAPPED
```

ensure that memory size is correct.

```
>RED DB:=SY:
>RED DB:=LB:
>MOU DB:DLDBL26
>@DB:[1,2]STARTUP
>* Please enter time and date (DD-MMM-YY HH:MM) [S]: <CR>
```

if you have set the correct time and date in step 8, it is not necessary to do so again.

```
>TIM
11:14:19 09-JUN-80
```

```
 SET /SYSUIC=[1,57]
>INS $CDA
>INS $BIGMAC /PAR=GEN
>INS $BIGTKB /PAR=GEN
>INS $FLX
>PIP SY:/FR
```

[STEP 9]

```
DB0: HAS 101793. BLOCKS FREE, 29887. BLOCKS USED OUT OF 131680.
LARGEST CONTIGUOUS SPACE = 74786. BLOCKS
```

use default checkpoint file size, ONLY if the number of contiguous blocks is greater than the default size.

```
>* Do you want the default checkpoint file size [5120]? [Y/N]: <Y> <CR>
> ACS SY:/BLKS=5120.
>RUN ERRLOG
>BRO ALL:RSX11M IS NOW ON THE AIR !!!!!
ERL -- ERROR LOG INITIALIZED
>@ <EOF>
```

```
>SET /UIC=[2,300] <CR>                                          [STEP 10]

>@DLDUETP <CR>                                                  this command will
                                                                start the UETP
                                                                session.
>;
>;      ************************************************************
>;      *                                                          *
>;      *   RSX-11M V3.2 INSTALLATION VERIFICATION PACKAGE         *
>;      *                                                          *
>;      ************************************************************
>;
>SET /UIC=[2,300]
>RUN ERRLOG
>;
>* DO YOU WISH TO RUN RMDEMO? [Y/N]: <CR>
>;
>* ENTER VERSION OF UETP TO BE RUN (SAM, SUB, MFG, ENG) [S]: MFG <CR>    always "MFG"
>* ENTER UNIT NUMBER OF TERMINAL [S]: 0 <CR>
>;
>;
>* ENTER INPUT DEVICE (DDNN) OR <cr>  [S]: <CR>                   press <cr> if UETP
                                                                resides on system
                                                                disk, if not, then
                                                                enter device it
                                                                resides on.
>;
>;
>;
>;              **** NOTE ****
>;
>; TEST MEDIA MUST BE LOADED ON ALL TAPE AND DISK DRIVES. USE SCRATCH TAPES
>; AND FILES-11 FORMAT DISKS.
>;
>; ALL MAGTAPES BEING TESTED ARE OVER-WRITTEN. THE DISKS ARE
>; TESTED WITH FILE-STRUCTURED I/O WITH NO NEGATIVE EFFECT ON DATA
>; OR STRUCTURE.
>;
>; BEFORE PERFORMING THE FILE-STRUCTURED I/O TEST, ALL UNMOUNTED
>; DISKS ARE MOUNTED AUTOMATICALLY.
>;
>* DO YOU NEED TO INITIALIZE ANY DISKS? [Y/N]: <CR>               if you forgot to
                                                                "init" any disks,
                                                                type "YES"
```

```
>;
>TIM
11:21:14 09-JUN-80
>;
>;
>; ONE COMPLETE PASS OF THIS UETP WILL TAKE 4 HOURS
>;
>* HOW MANY PASSES DO YOU WISH TO RUN [D R:1.-6. D:1.]: 2 <CR>


>;
>;
>;THE 2 PASS(ES) YOU HAVE SELECTED, WILL TAKE 8 HOURS TO RUN.
>;
>; NEEDED UTILITIES WILL BE INSTALLED NOW.
>; ************************************************************
>INS LB:$CMP
>; ************************************************************
>PIP TAILOR.DAT=DEVM.SAM/AP
>MAC DEFINE=LB:[11,10]DLDMC.MAC/PA:1,SY:[2,300]DEFINE
>TKB DEFINE/PR/CP=DEFINE,LB:[1,57]RSX11M.STB,[1,1]EXELIB/LB
>INS DEFINE/TASK=DEFINE
>PIP *.*/PU
>RUN DEFINE
>;
>;START OF UETP PASS #1
>;
>;
>;
>;       * CPU-BOUND LOAD TEST *
>;
>INS DUMMY/TASK=DUM00/PRI=40.
>INS LOGGER/TASK=LOG00
>INS QTRUN /TASK=QTR00
>RUN DUM00
>;
>; FOR THE NEXT FEW MINUTES A NUMBER.....ETC.   At this point the
    U.E.T.P. will run for the selected amount of time.
    The CPU tests are run first, for 2 HOURS, followed by 2 HOURS of
    IO EXERCISER, and then repeated until the pass count is satisfied.
```

at least 2 passes to meet minimum MAST requirements.

```
>REM SIO
>TIM
19:21:25 09-JUN-80

>;
>;      *TEST COMPLETED*
>;
>;
>;END OF UETP PASS #2
>;
>;
>PIP *.DAT;*/DE
>;
>; IF ANY ERRORS HAVE BEEN LOGGED BY ERROR LOGGER, WHEN THE COMMAND FILE
>; EXITS YOU SHOULD PRINT [2,300]ERRLOG.LST AND INVESTIGATE THE ERRORS.
>;
>ERF
ERF -- REQUESTED "ERRLOG" TO STOP LOGGING
>PSE SY:=SY:
ERL -- LOGGING ENDED AFTER 0 ERRORS
>SYE SY:=SY:/-SP
SYE -- 1. PAGES IN REPORT
>;
>RUN ERRLOG
ERL -- ERROR LOG INITIALIZED
>
>;
>;
>;
>; ********************************************************************************
>;
>TIM
17:14:53 25-MAR-80
>;
>;       *** END OF RSX-11M   INSTALLATION VERIFICATION ***
>;
>; ********************************************************************************
>/
>@ <EOF>
>
>PIP TI:=[2,300]ERRLOG.LST <CR>
```

[STEP 11]
type this to see any errors that have been logged. further information on the ERROR LOGGER can be found on page 27 of the "DLDSGN USERS GUIDE".

9.0 APPENDIX

9.1 APPENDIX A

CSR and VECTOR addresses supported
by stand-alone DSC

System-Generated CSR and Vector Addresses

DEVICE TYPE	CSR	VECTOR
DB:	176700	254
DK:	177404	220
DL:	174400	160
DM:	177440	210
DP:	176714	300 *
DR:	176700	320 *
MM:	172440	224
MT:	172522	320 *
MS:	172522	224

* Indicates nonstandard vector address

9.2 APPENDIX B

DEVICES SUPPORTED BY "DSC" VARIATIONS

DSCS8	DSCS16
RP04/05/06	RP04/05/06
RK05	RK05
RL01/02	RL01/02
RK06/07	RK06/07
RP02/03	RM02/03
RM02/03	TE16
TE10/16	TS11/TS04
TU45/77	TU45/77

F1050

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE

TITLE M.A.S.T. NPS-8/211 PHASE II [illegible]

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	[illegible]	MA-A0000-M1011				

ENG	APPD	SIZE	CODE	NUMBER	REV
Dominic Pischetola	Kevin Reichel	A	3P	MA-[illegible]	A

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1.0 SCOPE

This document is an attempt to provide WORD PROCESSING operators and technicians direction in running PHASE III on the WS211 Series systems. It does not try to explain how to run Word Processing Software in any environment other than F.A.& T.

The WPS-8/211 Phase III is a software/hardware system verification test designed to simulate the environment in which Word Processing Systems are used. This WPS-8/211 Phase III Package is written to provide an easy to use, consistent method of exercising WS211 Series Systems.

1.1 HARDWARE REQUIREMENTS

- 32K of memory
- A console terminal (VT100)
- RX02 Dual Floppy Drive

The Optional Hardware supported by this test package is as follows:

- Communication Lines (KL8-A IOT 46,47)

1.2 SOFTWARE REQUIREMENTS

- WPS-8/211 Phase III Test Package
  This Test package can be obtained by contacting the Salem Systems Manufacturing Engineering Group.

2.0 REFERENCE DOCUMENTATION

MP00780	WS211 Field Maintenance Print Set
QF711-HZ	WPS Documentation Kit

3.0 RESPONSIBILITY

The SALEM SYSTEMS MANUFACTURING ENGINEERING GROUP is responsible for maintaining this document.

4.0 SPECIAL INSTRUCTIONS

4.1 This Test Package is designed to exercise the following only:

- RX02 dual floppy drive
- Memory
- KL8-A Communication Lines (KL8-A IOT 46,47)

4.2 If system has an H326 panel, move all switches to the "OFF" position.

4.3 Connect a VT100 to the console terminal port located on the static filter bracket.

4.4 Throughout this document the user responses are underlined. Preceding the underlined response are the words Press or Type. Example: Press -> GOLD MENU (in respone to this example the user must press the GOLD key, located on the top left hand side of the mini-keypad, then the letter M). Example: Type -> E 2 <CR> (in respone to this example the user must type the letter E, space, number 2, carriage return).

5.0 GENERAL OVERVIEW

5.1 WPS-8/211 EXERCISER PROGRAM CONTENTS

The WPS-8/211 Phase III Exerciser Program consists of the following files:

Doc #	Name	
2	ABBREV....	File that contains stored text that will be called from an abbreviation code.
3	LIST.....	Used to perform List Processing.
4	SPEC.....	Used as the Selection Specification File during List Processing.
5	FORM.....	Output format of List Processing.
6	UDK1.....	139 block document. Used to exercise the RX floppy drives.
7	COMM TEST.	Document that is sent to the Host Terminal during the communication line test.

The WPS-8/211 Phase III Exerciser Program was designed to minimize operator intervention time. This was done by using the Software's "User Define Keys" (UDK's). The UDK's that are used are numbered from 1 thru 9. The following section includes a summary and a listing of each UDK.

UDK 1 - will initialize the diskette in Drive 1 as a document diskette and create a file named PASS on Drive 1. The PASS file is used to log the software features as they are performed to the hardware. The user will then be asked to type the System's DEC number.

M C RETURN D RETURN RETURN GOLD:M C SPACE P A S S RETURN GOLD:=ST

UDK 2 - will run the complete WPS-8/21. Phase III Test Package without operator intervention. This UDK will perform UDK 3 thru UDK 7 and UDK 9 for the required two (2) passes.

GOLD:3 GOLD:3 GOLD:9

UDK 3 - will perform one pass, instead of the required two(2) passes one would get by pressing UDK 2.

GOLD:4 GOLD:5 GOLD:6 GOLD:7

UDK 4 - will exercise the RX Drive 1. It will perform a GET document of 139 blocks from Drive 0 to Drive 1, it will then find the beginning of the document, then find the end of the document. When it finds the end of the document it will read the document backwards on the screen. Successful completion of this function will be logged into the Pass file.

C SPACE U D K 1 RETURN GOLD:G 0 . U D K 1 RETURN GOLD:T GOLD:B G-BACK GOLD:F D SPACE U D K 1 RETURN Y E S RETURN E SPACE 2 RETURN G-ADV GOLD:=DF GOLD:\ RETURN GOLD:F

UDK 5 - will perform a Diskette Verification check on Drive 1. Successful completion of this function will be logged into the Pass file.

M C RETURN V RETURN RETURN RETURN GOLD:M E SPACE 2 RETURN G-ADV GOLD:=DV GOLD:\ RETURN GOLD:F

UDK 6 - will perform a large List Processing function of selecting 49 records. The objective is to exercise memory. Successful completion of this function will be logged into the Pass file.

L P RETURN D RETURN 0 . 3 RETURN 0 . 4 RETURN 0 . 5 RETURN R RETURN G 0 RETURN GOLD:M E SPACE 2 RETURN G-ADV GOLD:=LP GOLD:\ RETURN GOLD:F D SPACE R RETURN YES RETURN

UDK 7 - will copy an index into a file. Successful completion of this function will be logged into the Pass file.

C I RETURN 1 SPACE X RETURN C I RETURN 0 SPACE X RETURN A RETURN E SPACE ? RETURN G-ADV GOLD:=CI GOLD:\ RETURN GOLD:=EN GOLD:\ GOLD:F D SPACE X RETURN YES RETURN

UDK 8 - see section 5.2.

UDK 9 - if UDK 2 is used, UDK 8 will then log an END OF TEST into the Pass file.

E SPACE 2 RETURN G-ADV GOLD:=FF GOLD:F

5.2 UDK 8 COMMUNICATION TEST

The WPS-8/211 Phase III Communication Line Test was designed to minimize operator intervention time. This was done by using the Software's User Define Keys. This UDK 8 will perform the following functions:

-- Set User terminal in communication mode.

-- Transmit a document called COMM TEST to the Host terminal.

-- User terminal will receive characters from the Host terminal by operator intervention.

C X RETURN RUBWRD H S SPACE D H RETURN 8 . 7 RETURN GOLD:M

6.0 WPS-8/211 OPERATING PROCEDURES

6.1 PREREQUISITES

Before one attempts to run this procedure it is assumed that all diagnostics and DEC-X/8 have been successfully run to completion.

6.2 RUNNING THE WPS-8/211 PHASE III TEST

To begin the WPS-8/211 Phase III Test, the user must first:

6.2.1 Apply power to the equipment in the main cabinet. This is done by depressing the switch at the top of the cabinet marked "1".

6.2.2 Apply power to the console terminal.

6.2.3 Insert the WPS-8/211 Phase III Test Disk in Drive 0.

6.2.4 Depress the "BOOT" switch located at the top of the cabinet. The following message is displayed at the console terminal indicating that the boot floppy has successfully loaded into the system;

```
Digital Equipment Corporation

Version x.x

Make sure your system diskette is in drive 0

And press RETURN
```

6.2.5 Insert a single density scratch diskette in Drive 1.

6.2.6 Press the **RETURN** key on your console keyboard.

6.2.7 At this point the DATE/TIME MENU is displayed at the console terminal. The user must enter a valid date and time followed by a **RETURN.**

6.3 RUNNING WPS-8/211 EXERCISER PROGRAM

6.3.1 Press -> GOLD 1 -- Initialization of RX drive 1 will now take place.

6.3.2 Type -> DEC number of system that is being tested.

6.3.3 Press -> GOLD F

6.3.4 Press -> GOLD 2
this test will now exercise the system for approximately 30 mins. Upon completion the Main Menu will be displayed.

6.3.5 Type -> E 2 <CR>

6.3.6 Press -> PARA -- key until your VT100 sounds a beep. This will enable you to check the pass file to determine if there were any errors. See Appendix A.

6.3.7 Press -> GOLD F -- will file document.

6.4 TESTING COMMUNICATION LINES

6.4.1 Attach a VT100 to P6 (P6 is located on the Communication H326 Panel. This VT100 will be referenced as Host VT100. Set Host VT100 up to 1200 baud by:

a) Press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 Keyboard.

b) Press the number 5 to enter SET-UP B.

c) Press the Transmit (Key 7) and Receive (Key 8) Keys until the display reads 1200. Your Host VT100 should look like this on the screen:

1 ØlØØ 2 ØlØl 3 ØØØØ 4 ØØlØ T SPEED 1200 R SPEED 1200

d) To exit SET-UP B press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 keyboard.

e) Return to the console terminal and

6.4.2 Type -> SO <CR>

6.4.3 Type -> CL 1 <CR>

6.4.4 Press -> GOLD MENU

6.4.5 Press -> GOLD 8
now looking at the Host VT100 that is connected to P6, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal

6.4.6 Type -> THIS IS A TEST
The above message will then be displayed on the Console Terminal.

6.4.7 Type -> \R -- on the Console Terminal to exit.

6.4.8 Move P6 to P7. Set Host VT100 up to 300 baud, Data Bits = 7, Parity Sense = Even, and Parity = On by:

a) Press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 Keyboard.
b) Press the number 5 to enter SET-UP B.
c) Position the cursor above the feature switch to be changed by using the space bar. Change the feature settings by pressing the 6 key on the keyboard. Each time the key is pressed the feature will change to the opposite state.
d) Press the Transmit (Key 7) and Receive (Key 8) Keys until the display reads 300.

Your Host VT 100 Set-Up B should look like this:

1 0100 2 0101 3 0000 4 1100 T SPEED 300 R SPEED 300

e) To exit SET-UP B press the SET UP key on your Host VT100.

f) Return to the console terminal and

6.4.9 Type -> SO <CR>

6.4.10 Type -> CL 2 <CR>

6.4.11 Press -> GOLD MENU

6.4.12 Press -> GOLD 8
now looking at the Host VT100 that is connected to P7, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal

6.4.13 Type -> THIS IS A TEST
The above message will then be displayed on the Console Terminal.

6.4.14 Hit -> \R -- on the Console Terminal to exit.

6.4.15 Move P7 to P8. Host VT 100 should still be at 300 baud. Change your Host VT 100 Set-Up B, Word 4, (follow steps a thru f in Section 6.4.8) to the following:

4 0010

6.4.16 Type -> SO <CR>

6.4.17 Type -> CL 3 <CR>

6.4.18 Press -> GOLD MENU

6.4.19 Press -> GOLD 8
now looking at the VT100 that is connected to P8, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal:

6.4.20 Type - > THIS IS A TEST
The above message will then be displayed on your Console Terminal.

6.4.21 Type -> \R -- on your Console Terminal to exit.

7.0 WPS-8/211 RUN SUMMARY

The WPS-8/211 Phase III Test was designed to report to the Pass file the name of the specific function it just completed. If one of the functions did not report to the Pass file, we then have an error.

Check the Run Summary Checklist (Appendix A) to determine if you have an error. If you found an error, perform the specific function separately. This is done by typing the following User Define Keys: GOLD n (n = either 1,4,5,6,7).

Error	Action
INITIALIZATION OF DRIVE 1	Press -> GOLD 1
COPY FROM DRIVE Ø TO DRIVE 1 EDIT HAS BEEN TESTED DELETE HAS BEEN TESTED	Press -> GOLD 4
DISKETTE VERIFICATION	Press -> GOLD 5
LIST PROCESSING	Press -> GOLD 6
CREATE INDEX	Press -> GOLD 7

If error persists advise the Manufacturing Engineering Group for technical assistance.

APPENDIX A

RUN SUMMARY CHECKLIST

In order to determine a successful completion of the Phase III Test, the following page contains an example of a successful run of Phase III testing. Your summary which is located in a file called PASS, must be exactly the same as the example on the next page. If not refer to section 7.0 WPS-8/211 Run Summary.

SALEM SYSTEMS MANUFACTURING WPS-8/211 PHASE III TEST

VERSION 1.0

THIS IS THE START OF TESTING FOR
DEC # (The DEC # you originally typed in)

INITIALIZATION OF DRIVE 1 - PASS
COPY FROM DRIVE 0 TO DRIVE 1 - PASS
EDIT HAS BEEN TESTED - PASS
DELETE HAS BEEN TESTED - PASS (DATE,TIME)

DISKETTE VERIFICATION HAS BEEN TESTED - PASS (DATE,TIME)

LIST PROCESSING HAS BEEN TESTED - PASS (DATE, TIME)

CREATE INDEX TESTED - PASS (DATE, TIME)

---------- P A S S C O M P L E T E D (DATE, TIME)

INITIALIZATION OF DRIVE 1 - PASS
COPY FROM DRIVE 0 TO DRIVE 1 - PASS
EDIT HAS BEEN TEST - PASS
DELETE HAS BEEN TESTED - PASS (DATE,TIME)

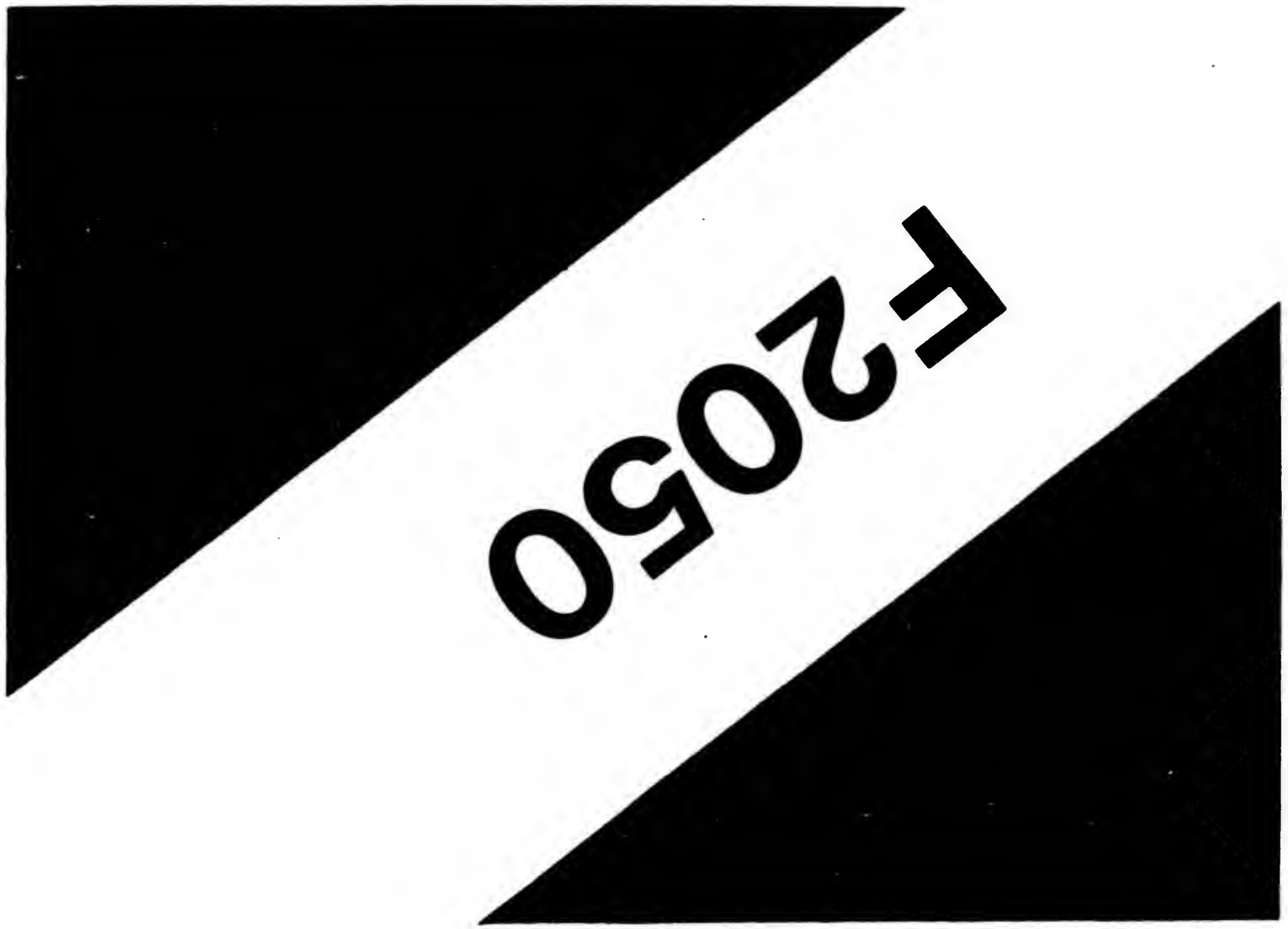
DISKETTE VERIFICATION HAS BEEN TESTED - PASS (DATE,TIME)

LIST PROCESSING HAS BEEN TESTED - PASS (DATE, TIME)

CREATE INDEX TESTED - PASS (DATE, TIME)

---------- P A S S C O M P L E T E D (DATE, TIME)
IF SYSTEM HAS TWO (2) COMPLETED PASSES THEN

THIS IS THE END OF THE TEST


2021
0505

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION

DATE [illegible]

TITLE M.A.S.T. MPS-8/312 PHASE II WCLR'S CH.M.

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	New release	MA-A0000-ML011			[illegible]	[illegible]

ENG	APPD	SIZE	CODE	NUMBER	REV
Dominic Vischetola	[illegible]	A	[illegible]	[illegible]	A

EN-01402-10-M672-(392)

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1.0 SCOPE

This document is an attempt to provide WORD PROCESSING operators and technicians direction in running PHASE III on the WPS212 Series systems. It does not try to explain how to run Word Processing Software in any environment other than F.A.& T.

The WPS-8/212 Phase III is a software/hardware system verification test designed to simulate the environment in which Word Processing Systems are used. This WPS-8/212 Phase III Package is written to provide an easy to use, consistent method of exercising WS212 Series Systems.

1.1 HARDWARE REQUIREMENTS

- 32K of memory
- A console terminal (VT100)
- Two (2) Dual RX02 Floppy Drives

The Optional Hardware supported by this test package is as follows:

- Communication Lines (KL8-A IOT 46,47)
- User Lines (KL8-A 40,41)

1.2 SOFTWARE REQUIREMENTS

- WPS-8/212 Phase III Test Package
  This Test package can be obtained by contacting the Salem Systems Manufacturing Engineering Group.

2.0 REFERENCE DOCUMENTATION

MP00780	WS211 Field Maintenance Print Set
QF711-GZ	WPS Documentation Kit

3.0 RESPONSIBILITY

The SALEM SYSTEMS MANUFACTURING ENGINEERING GROUP is responsible for maintaining this document.

4.0 SPECIAL INSTRUCTIONS

4.1 This Test Package is designed to exercise the following devices:

- Two (2) Dual RX FLOPPY DRIVES
- Memory
- KL8-A Communication Lines (IOT 46,47)
- KL8-A User Lines (IOT 40,41)

4.2 If the system has an H325 Panel, move all switches to the "OFF" position.

4.3 Connect a VT100 to the console terminal port located on the static filter bracket.

4.4 Throughout this document the user responses are underlined. Preceding the underlined response are the words Press or Type. Example: Press -> GOLD MENU (in respone to this example the user must press the GOLD key, located on the top left hand side of the mini-keypad, then the letter M). Example: Type -> E 2 <CR> (in respone to this example the user must type the letter E, space, number 2, carriage return).

5.0 GENERAL OVERVIEW

5.1 WPS-8/212 EXERCISER PROGRAM CONTENTS

The WPS-8/212 Phase III EXERCISER PROGRAM CONSISTS OF THE Following files:

DOC #	NAME	
2	ABBREV....	File that contains stored text that will be called from an abbreviation code.
3	LIST.....	Used to perform List Processing.
4	SPEC.....	Used as the Selection Specification File during List Processing.
5	FORM.....	Output format of List Processing.
6	UDK1.....	128 Block document. Used to exercise the RX floppy drives.
7	COMM TEST.	Document that is sent to the Host Terminal during the Communication Line test.
8	MESS1.....	Will display a procedure for initializing diskettes.
9	START.....	File that logs the System DEC number.

The WPS-8/22 Phase III Exerciser Program was designed to minimize operator intervention time. This was done by using the Software's "User Define Keys" (UDK's). The UDK's that are used are numbered from 1 thru 9. The following section includes a summary and a listing of each UDK.

UDK 1 - will edit the start file to delete the previous System's DEC number. The user will then be asked to type the System's DEC number.

E SPACE 0 . 9 RETURN GOLD:, GOLD:. ADVANC DELWRD

UDK 2 - will inform the user to hit GOLD 9 to initialize scratch diskettes.

E SPACE 0.8 RETURN GOLD:B

UDK 3 - will create a file named PASS on Drive 1. The START file on Drive 0 will be copied into the PASS file on Drive 1 by the GET document command. The PASS file is used to log the software features as they are performed to the hardware.

This UDK will then proceed to exercise RX Drive 0 and 1 by performing a GET document of 120 blocks from Drive 0 to Drive 1, it will then find the beginning of the document, then find the end of the document. When it finds the end of the document it will read the document backwards on the screen. Successful completion of this function will be logged into the PASS file.

This UDK will then perform the above exerciser to RX Drive 2 from RX Drive 1, then to RX Drive 3 from RX Drive 0.

C SPACE P A S S RETURN GOLD:G 0 . 9 RETURN GOLD:F C SPACE F RETURN GOLD:G 0 . 6 RETURN GOLD:T GOLD:B G-BACK GOLD:F E SPACE 2 RETURN G-ADV GOLD:AA GOLD:\ RETURN GOLD:F C SPACE 2 . F RETURN GOLD:G F RETURN GOLD:T GOLD:B G-BACK GOLD:F E SPACE 2 RETURN G-ADV GOLD:BB GOLD:\ RETURN GOLD:F C SPACE 3 . F RETURN GOLD:G 0 . 6 RETURN GOLD:T GOLD:B G-BACK GOLD:F E SPACE 2 RETURN G-ADV GOLD:CC GOLD:\ RETURN GOLD:F GOLD:4

UDK 4 - will perform a diskette verification check on Drive 1. Successful completion of this function will be logged into the PASS file.

M C RETURN V RETURN RETURN RETURN GOLD:M E SPACE 2 RETURN G-ADV GOLD:DV GOLD:\ RETURN GOLD:F GOLD:5

UDK 5 - will perform a large List Processing function of selecting 49 records. A GET Document will copy, FORM from Drive 0 to Drive 2, SPEC from Drive 0 to Drive 3. List Processing will then merge the documents LIST on Drive 0, FORM on Drive 2, and SPEC on Drive 3 into a document named R on Drive 1. Successful completion of this function will be logged into the Pass file.

C SPACE 3 . S RETURN GOLD:G 0 . 4 RETURN GOLD:F C SPACE 2 . M RETURN GOLD:G 0 . 5 RETURN GOLD:F L P RETURN D RETURN 0 . 3 RETURN 3 . S RETURN 2 . M RETURN R RETURN G O RETURN GOLD:M E SPACE 2 RETURN G-ADV GOLD:LP GOLD:\ RETURN GOLD:F GOLD:6

UDK 6 - will log an END OF TEST into the PASS file.

UDK 7 - reserved for future use.

UDK 8 - see Section 5.2.

UDK 9 - will initialize diskettes as document diskettes. After initialization this UDK will go back to UDK #2.

M C RETURN D RETURN RETURN GOLD:M GOLD:2

5.2 UDK 8 COMMUNICATION TEST

The WPS-8/212 Phase III Communication Line Test was designed to minimize operator intervention time. This was done by using the Software's User Define Keys. This UDK 8 will perform the following functions:

-- Set User terminal in communication mode.

-- Transmit a document called COMM TEST to the Host terminal.

-- User terminal will receive characters from the Host terminal by operator intervention.

C X RETURN RUBWRD H S SPACE D H RETURN 0 . 7 RETURN GOLD:M

6.0 WPS-8/212 OPERATING PROCEDURES

6.1 PREREQUISITES

Before one attempts to run this procedure it is assumed that all diagnostics and DEC X/8 have been successfully run to completion.

6.2 RUNNING THE WPS-8/212 PHASE III TEST

To begin the WPS-8/212 Phase III Test, the user must first:

6.2.1 Apply power to the equipment in the main cabinet. This is done by depressing the switch at the top of the cabinet marked "1".

6.2.2 Apply power to the console terminal.

6.2.3 Insert the WPS-8/212 Phase III Test Disk in Drive 0.

6.2.4 Depress the "BOOT" switch located at the top of the cabinet. The following message is displayed at the console terminal indicating that the boot floppy has successfully loaded into the system;

```
Digital Equipment Corporation

Version x.x

Make sure your system diskette is in drive 0

And press RETURN
```

6.2.5 Press the **RETURN** key on your console keyboard.

6.2.6 At this point the DATE/TIME MENU is displayed at the console terminal. The user must enter a valid date and time followed by a **RETURN.**

6.3 RUNNING WPS-8/212 EXERCISER PROGRAM

6.3.1 Press -> **GOLD** 1

6.3.2 Type -> the **DEC** number of system that is being tested.

6.3.3 Press -> **GOLD** F

6.3.4 Press -> **GOLD** 2

6.3.5 ->INSERT A SINGLE DENSITY SCRATCH DISKETTE IN DRIVE 1.

6.3.6 Press -> **GOLD** F

6.3.7 Press -> **GOLD** 9

6.3.8 -> REMOVE DISKETTE FROM DRIVE 1 AND INSERT IT IN DRIVE 3.

6.3.9 -> INSERT ANOTHER SINGLE DENSITY SCRATCH DISKETTE IN DRIVE 1.

6.3.10 Press -> **GOLD** F

6.3.11 Press -> **GOLD** 9

6.3.12 -> REMOVE DISKETTE FROM DRIVE 1 AND INSERT IT IN DRIVE 2.

6.3.13 -> INSERT ANOTHER SINGLE DENSITY SCRATCH DISKETTE IN DRIVE 1.

6.3.14 Press -> **GOLD** F

6.3.15 Press -> **GOLD** 9

6.3.16 Press -> **GOLD** F

6.3.17 Press -> **GOLD** 3
this test will now exercise the system for approximately 30 mins. Upon completion the Main Menu will be displayed.

6.3.18 Type -> **E** 2 **<CR>**

6.3.19 Press -> **PARA** -- key until your VT100 sounds a beep. This will enable you to check the pass file to determine if there were any errors. See Appendix A.

6.3.20 Type -> **GOLD** F -- will file document.

6.4 TESTING COMMUNICATION LINES

6.4.1 Attach a VT100 to P6 (P6 is located on the communication H326 panel). This VT100 will be referenced as Host VT100. Set Host VT100 up to 1200 baud by:

a) Press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 Keyboard.

b) Press the number 5 to enter SET-UP B.

c) Press the Transmit (Key 7) and Receive (Key 8) Keys until the display reads 1200. Your Host VT100 should look like this on the screen:

1 0100 2 0101 3 0000 4 0010 T SPEED 1200 R SPEED 1200

d) To exit SET-UP B press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 keyboard.

e) Return to the console terminal and

6.4.2 Type -> **SO** <CR>

6.4.3 Type -> **CL 1** <CR>

6.4.4 Press -> **GOLD MENU**

6.4.5 Press -> **GOLD 8**
now looking at the Host VT100 that is connected to P6, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal

6.4.6 Type -> **THIS IS A TEST**
The above message will then be displayed on the Console Terminal.

6.4.7 Type -> **\R** -- on the Console Terminal to exit.

6.4.8 Move P6 to P7. Set Host VT100 up to 300 baud, Data Bits = 7, Parity Sense = Even, and Parity = On by:

a) Press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 Keyboard.
b) Press the number 5 to enter SET-UP B.
c) Position the cursor above the feature switch to be changed by using the space bar. Change the feature settings by pressing the 6 key on the keyboard. Each time the key is pressed the feature will change to the opposite state.
d) Press the Transmit (Key 7) and Receive (Key 8) Keys until the display reads 300.

Your Host VT 100 Set-Up B should look like this:

1 0100 2 0101 3 0000 4 1100 T SPEED 300 R SPEED 300

e) To exit SET-UP B press the Host VT100 SET-UP KEY located on the upper left hand corner of your Host VT100 keyboard.

f) Return to the console terminal and

6.4.9 Type -> **SO** <CR>

6.4.10 Type -> **CL 2** <CR>

6.4.11 Press -> **GOLD MENU**

6.4.12 Press -> **GOLD 8**
now looking at the Host VT100 that is connected to P7, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal

6.4.13 Type -> **THIS IS A TEST**
The above message will then be displayed on the Console Terminal.

6.4.14 Type -> **\R** -- on the Console Terminal to exit.

6.4.15 Move P7 to P8. Host VT100 should still be at 300 baud. Change your Host VT 100 Set-Up B, Word 4,(follow steps a thru f in Section 6.4.8) to the following:

4 0010

6.4.16 Type -> **SO** <CR>

6.4.17 Type -> **CL 3** <CR>

6.4.18 Press -> **GOLD MENU**

6.4.19 Press -> **GOLD 8**
now looking at the VT100 that is connected to P8, you should see the following flashing:

COMMUNICATION LINE TEST - WORKING.....

The last line you will see on your Host VT100 will state:

ECHO CHARACTERS FROM HOST TO TERMINAL - \R ON USER TERMINAL TO EXIT

Type the following on your Host VT100 Terminal:

6.4.20 Type -> **THIS IS A TEST**
The above message will then be displayed on your Console Terminal.

6.4.21 Type -> **\R** -- on your User Terminal to exit.

7.0 TESTING USER LINES

7.1 If your system has a KL8-A at IOT 40,41 or IOT 46,47 connect a VT100 to P5 (L0) on the H326 Panel. This VT100 is hereafter know as VT100 #2.

NOTE: If your system is configured for two (2) KL8-A's and two (2) H326 Distribution Panels -- IOT 40,41 and IOT 46,47, the KL8-A at IOT 40,41 is inoperative. In this situation, IOT 46,47 H326 Panel P5 (L0) is reserved for VT100 #2, and P6 - P8 are reserved for communications. In order to test out P5 (L0) your VT100 #2 must be set up for 9600 baud.

7.2 Remove scratch diskette from Drive 2.

7.3 Insert another WPS-8/212 PHASE III Test Disk in Drive 2.

7.4 Depress the "BOOT" switch located at the top of the cabinet. The following message should now appear on your VT100 #2:

```
Digital Equipment Corporation

Version x.x

Make sure your system diskette is in drive 2

And press RETURN
```

7.5 Press -> <CR> -- on VT100 #2

7.6 At this point the DATE/TIME MENU is displayed on the VT100 #2 terminal. The user must enter a valid date and time followed by a **RETURN.**

7.7 The MAIN MENU should now be displayed on the VT100 #2 terminal. Visually check that the date and time you typed into the DATE/TIME MENU now appears in the upper right-hand corner.

7.8 Type -> F <CR> - to log off system.

NOTE: If you have another KL8-A at IOT 40,41 power down system, unseat KL8-A IOT 46,47, plug VT100 #2 into P5 (L0) of the distribution panel (IOT 40,41). Power up system and follow the steps 7.4 though 7.8. After successful completion reseat KL8-A IOT 46,47.

8.0 WPS-8/212 RUN SUMMARY

The WPS-8/212 Phase III Test was designed to report to the Pass file the name of the specific function it just completed. If one of the functions did not report to the Pass file, we then have an error.

Check the Run Summary Checklist (Appendix A) to determine if you have an error. If you found an error, perform the specific function separately. This is done by typing the following User Define Keys: GOLD n (n = either 3,4,5).

Error	Action
COPY FROM DRIVE Ø TO DRIVE 1 COPY FROM DRIVE 1 TO DRIVE 2 COPY FROM DRIVE Ø TO DRIVE 3	Hit>GOLD 3
DISKETTE VERIFICATION	Hit>GOLD 4
LIST PROCESSING	Hit>GOLD 5

If error persists advise the Manufacturing Engineering Group for technical assistance.

APPENDIX A

RUN SUMMARY CHECKLIST

In order to determine a successful completion of the Phase III Test, the following page contains an example of a successful run of Phase III testing. Your summary which is located in a file called PASS, must be exactly the same as the example on the next page. If not refer to section 8.0 WPS-8/212 Run Summary.

SALEM SYSTEMS MANUFACTURING WPS-8/212 PHASE III TEST

VERSION 1.0

THIS IS THE START OF TESTING FOR
DEC # (The DEC # you originally typed in)

COPY FROM DRIVE Ø TO DRIVE 1 - PASS (DATE,TIME)

COPY FROM DRIVE 1 TO DRIVE 2 - PASS (DATE,TIME)

COPY FROM DRIVE Ø TO DRIVE 3 - PASS (DATE,TIME)

DRIVE 1 DISKETTE VERIFICATION - PASS (DATE,TIME)

LIST PROCESSING HAS BEEN TESTED - PASS (DATE,TIME)

---------- P A S S C O M P L E T E D (DATE, TIME)

THIS IS THE END OF THE TEST


V2K100

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION M.A.S.T. DATE

TITLE MODULAR APPROACH TO SYSTEMS TEST

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A						
B	VAX 11780 CPU Procedure Update and rewrite	ML013	Al Gauthier	3/24/83		

ENG	APPD	SIZE	CODE	NUMBER	REV
Al Gauthier	Bob Beck	A	SP	MAV2100-0-0	B

VAX 11780 CPU

1.0 INTRODUCTION

The VAX 11/780 CPU is a high-speed, microprogrammed 32-bit hexadecimal computer. The 11/780 executes VAX-11 variable length instructions in native mode, and non-privileged PDP-11 instructions in compatibility mode. The processor can directly address 4 gigabytes of virtual address space, and provides a complete and powerful instruction set that includes integral decimal, character string, and floating point instructions. The 11/780 CPU includes an 8KB memory cache, integral memory management, translation buffer, 8B instruction buffer, 16 general registers, 32 interrupt priority levels, and an intelligent console. (LSI-11)

2.0 REFERENCE DOCUMENTATION

2.1 Manuals

2.1.1	Micro Computer Handbook	EB-07948
2.1.2	PDP-11/03 Users Manual	EK-LSI11-TM
2.1.3	RXV11 Users Manual	EK-RXV11-OP
2.1.4	Floppy Disk System Maint. Man.	EK-RX01-MM
2.1.5	RX01 Floppy IPB	EK-RX01-IP
2.1.6	PDP 11/03 System Manual	EK-11V03-TM
2.1.7	CPU Processor Manual	EK-KA780-TD
2.1.8	TB/CACHE/SBI Control Manual	EK-MM780-TD
2.1.9	Console Manual	EK-KC780-TD
2.1.10	Power System Overview	EK-PS780-TD
2.1.11	Diagnostic System Manual	EK-DS780-TD
2.1.12	Hardware Users Guide	EK-UG780-UG
2.1.13	System Maint. Guide	EK-11780-PG

2.2 Reference Listings

2.2.1	Wirelist & Pin Sort	7013628-0-0
2.2.2	Micro Code Listing (Fiche)	EP-VAX-PCS
2.2.3	WCS Code Listing (Fiche)	EP-VAX-WCS
2.2.4	LSI-11 Programming Ref. Card	EJ-S2000
2.2.5	VAX Instruction Card	EJ-S2000
2.2.6	VAX 11780 Architecture Hndbk	EB-07466
2.2.7	VAX 11 Software Handbook	EB-08136

2.3 Maintenance Print Sets

2.3.1	KA780 Maint. Print Set	MP00496
2.3.2	MS780 Maint. Print Set	MP00498
2.3.3	DW780 Maint. Print Set (OPT)	MP00497
2.3.4	RH780 Maint. Print Set (OPT)	MP00499
2.3.5	FP780 Maint. Print Set (OPT)	MP00565

3.0 REQUIRED TEST EQUIPMENT

3.1 Diagnostic Diskettes

3.1.1	RX1 Floppy Diskette	AS-E633?-YE
3.1.2	RX2 Floppy Diskette	AS-E158?-DE
3.1.3	RX3 Floppy Diskette	AS-E159?-DE
3.1.4	RX7 Floppy Diskette	AS-E160?-YE
3.1.5	RX8 Floppy Diskette	AS-E161?-YE
3.1.6	RX25 Floppy Diskette	AS-F748?-YE

3.2 W9025 extender board

3.2 Assorted chip clips

3.3 Oscilloscope Tektronix 465 or equivalent

3.4 Voltmeter Tektronix DM44 or equivalent

3.5 Console Terminal

4.0 REQUIRED DIAGNOSTIC PROGRAMS

4.1 LEVEL 4 -The following Diagnostics do not require Diagnostic Supervisor.

ESKAH ---Microdiagnostic Test #1
ESKAJ ---Microdiagnostic Test #2

4.2 EVKAA ---This Diagnostic needs to be run only if operator experiences trouble with Diagnostic Supervisor.

4.3 LEVEL 3 -These Diagnostics run standalone under Diagnostic Supervisor.

EVKAB ---Basic Instruction Exerciser
EVKAC ---Floating Point Inst. Exerciser. Run this test whether Floating Point is installed or not
EVKAD ---Compatability Mode Instruction
EVKAE ---Privileged Architecture

4.4 LEVEL 2 -These Diagnostics run standalone under Diagnostic Supervisor or with Diagnostic Supervisor running under VMS.

4.5 LEVEL 1 -VMS must be running for these Diagnostics.

5.0 SPECIAL INSTRUCTIONS

5.1 CAUTION: No metallic jewelry should be worn while servicing this equipment, due to the high current capabilities of the power supplies.

5.2 Jumper conversion used is:

I = Jumper IN, O = Jumper Out, X = Unimportant

Jumper configurations are explicit or standard configuration is shown by an arow (-------->).

5.3 To run floppy ZZ-ESZAC-X.X without the SBI connected to the CPU, jumper the following: (KA780 backplane)

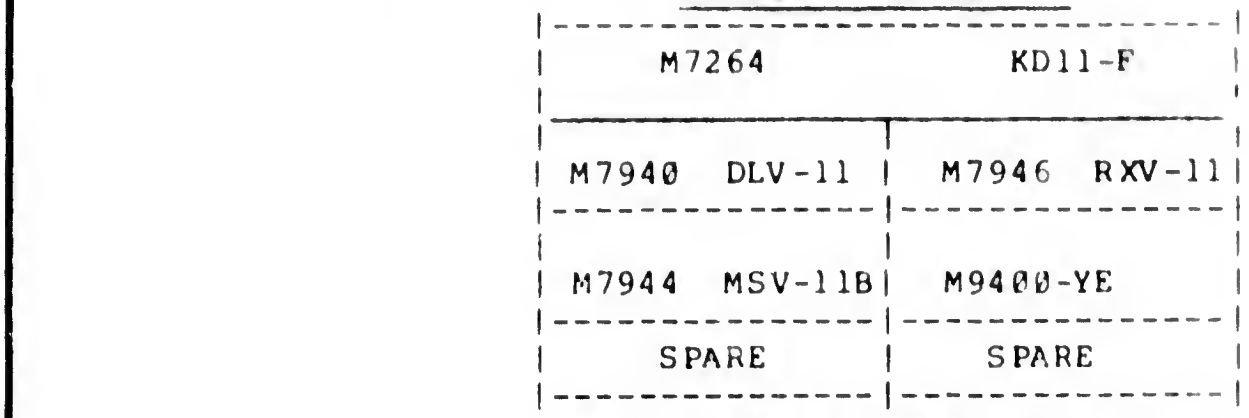
FROM	TO
E01F1	J5-T
E01F2	J5-J
E01H2	J5-R
E01J1	J5-Z
E01J2	J5-X
E01K2	J5 BB

5.4 In section 8.0, the user's response is underlined.

6.0 INSTALLATION AND TEST SET-UP INSTRUCTION

6.1 KC780 (11/03 Subsystem)

Module Utilization



(Front View-Module Handle Side)

6.2 Jumper Configuration KD11-F (M7264) Refer to Figure 1

JUMPER	IN/OUT	RESULT
W1	O	Resident memory at bank 0
W2	I	Resident memory at bank 0
W3	O	LTC Interrupt enabled
W4	O	Memory Refresh enabled
W5	O	Power up at 173000
W6	I	Power up at 173000
W7	*	Preconfigured
W8	*	Preconfigured
W9	O	Disables resident memory
W10	O	BRPLYL
W11	I	Enables on board memory select

6.3 M9400-YE Cable Connection. Refer to Figure 2 Cables are BC05L-10

From M9400-YE	To Backpanel
(Stripe Left, Smooth side UP)	(Stripe Down, Ribbed side to backpanel)
J1	J8
J2	J7

6.4 Configuration of RXV-11 (M7946). Refer to Figure 3 Address Jumpers are set to: 177170-177172

ADDRESS	JUMPER	IN/OUT
A12	W17	O
A11	W16	O
A10	W15	O
A9	W14	O
A8	W13	I
A7	W12	I
A6	W11	O
A5	W10	O
A4	W9	O
A3	W8	O
A2	W7	I

Vector Jumpers are set: 264

VECTOR	JUMPER	IN/OUT
V7	W6	O
V6	W5	I
V5	W4	O
V4	W3	O
V3	W2	I
V2	W1	O

6.5 Configuration of DLV11 (M7940). Refer to Figure 4.

JUMPER	IN/OUT	RESULT
NP	O	No Parity
2SB	I	1 Stop Bit
NB2	O	8 Data Bits
NB1	O	8 Data Bits
PEV	X	Unimportant whether parity odd/even
FEH	O	No halt on framming error
EIA	O	EIA operation
FR3	O	Selects 300 Baud
FR2	O	Selects 300 Baud
FR1	I	Selects 300 Baud
FR0	O	Selects 300 Baud
CL4-CL0	I	20MA Active Xmit and Receive

NOTE: When using an LA120 the Baud is set for 1200. Refer to table below.

JUMPER	IN/OUT
EIA	I
FR2	I
FR1	O

6.5.1 Vector Jumpers set to 60-64

Vector	In/Out
V7	I
V6	I
V5	O
V4	O
V3	I

6.5.2 Address Jumpers set to 177560-177566

Address	In/Out
A12	O
A11	O
A10	O
A9	O
A8	O
A7	I
A6	O
A5	O
A4	O
A3	I

6.6 Configuration of MSV-11B (M7944). Refer to Figure 5

JUMPER	IN/OUT	RESULT
W1	I	Memory Bank select
W2	I	" " "
W3	O	" " "
W4	O	Enables BRPLY during refresh

6.7 KA780 Module Utilization Chart. Refer to Figure 6

6.8 Control Store Jumpers

6.8.1 PCS, M8234 - Backplane Slot 22 Bank Address, Select. For location and pinning of J12 refer to Figures 7 and 8, and to table below.

Bank Adds.	J12-L	J	F	D	B
Ø-4K	I	O	O	O	O
	J5	J4	J3	J2	J1

NOTE: J1-5 for cross ref. to module schematic only.

6.8.2 Update System I.D. Register to proper Rev level by installing/removing Jumpers on J12 & J13. Refer to Figure 8.

6.8.3 Optional WCS (M8233) or PCS (M8234). Slot 18 Bank Address Select. For location and pinning of J11, refer to Figures 7, 8 and table below.

NOTE: W23 and W24 needs to be installed in the M8232 Module for optional WCS/PCS.

Refer to Figure 9.

Bank Adds.	J11-FF Board J5 CV2	DD J4 CM1	BB J3 CL2	Z J2 CL1	X J1 CB1
1K	I	I	I	I	O
2K	I	I	I	O	I
3K	I	I	O	I	I
4K	I	O	I	I	I
5K	O	I	I	I	O
6K	O	I	I	O	I
7K	O	I	O	I	I
8K	O	O	I	I	I
	J5	J4	J3	J2	J1

NOTE: J1-5 for cross ref. to module schematic only.

6.8.4 Console Signals at 11/780 CPU backplane.

SIGNAL	J9 PIN	BACKPL
SCPA Boot SW H	B	A29A1
SCPA AUTO Restart H	D	A29B2
SCPA LOCK H	F	A29F1
SCPA REMOTE H	E	A29K1
CIBN Run H	K	A29D1
CIBN ATTN H	L	A29E1

6.9 TR Arbitration Level Selection. For locating and pinning of J10, refer to table below as well as Figures 7 and 8.

J10 -- J F D B	Backplane Wire F02M2 to ----	BUS TR Level
I I I I	----------	16
I I I O	F02U2	15
I I O I	F02U1	14
I I O O	F02T2	13
I O I I	F02S2	12
I O I O	F02P2	11
I O O I	F02P1	10
I O O O	F02N1	09
O I I I	F02M1	08
O I I O	F02J2	07
O I O I	F02J1	06
O I O O	F02H2	05
O O I I	F02F2	04
O O I O	F02E1	03
O O O I	F02D1	02
O O O O	F02C1	01

6.10 Perform visual inspection for obvious discrepancies, damage, or potential power problems.

6.11 Check to see that modules are in the proper slots. Refer to Figure 6.

6.12 Diskette Load

6.12.1 Release drive lock and swing out floppy drive assembly.

6.12.2 Insert Diskette RX1 Floppy, MAINDEC-11-DZQAA-PB, into RX01 drive assembly.

6.12.3 Close diskette slot cover.

6.13 Power on/Bootstrap

6.13.1 With Main Breaker OFF, plug power cord into proper power outlet.

6.13.2 Turn 869 Power Controller Function Switch to REMOTE position.

6.13.3 With the H7111 Time Of Day Power Supply, LSI-11 DC, and all H7100 CKT Breakers OFF, apply power to 869 Power Controller.

6.13.4 Middle blower should be ON, with air exiting from center exhaust.

6.13.5 Turn on H7111 Time Of Day Power Supply. Power ON indicator should light.

6.13.6 Power On System by Key Switch, and verify operation and air flow direction of the other two blowers.

6.13.7 Power on LSI-11, by placing DC ON/OFF Switch to ON. DC and LED should light. Place HALT/ENABLE Switch to ENABLE.

NOTE: If DC on LED is not lit, check power switch on rear of LSI-11 for on position.

6.13.8 Set CPU Control Panel AUTO/RESTART Switch to OFF.

6.13.9 Turn on H7100 CKT Breakers one at a time observing Power Indicator LED's. Should get green power normal indicators.

6.13.10 With Key in LOCAL position, Console program will boot.

6.13.11 Console Terminal will output message. CPU should now be ready to run diagnostics. Message is shown at 8.1.1 of this procedure.

7.0 POWER CHECK

7.1 Check D.C. voltages, observing safety rules, as follows

CAUTION: Remove rings and watches which could short across voltage points, resulting in severe burns.

VOLTAGE/SIGNAL	PIN	FROM-------TO
+5A (PS#1)	C24A2	4.9V ----- 5.2V
+5B (PS#2)	C01A2	4.9V ----- 5.2V
+5C (PS#3)	C04A2	4.9V ----- 5.2V
+5 T.O.D. CLK	J20-1	4.75V ---- 5.25V
-5 (PS#2)	J18-1 J18-2	-5.0V ----- 5.3V
-10 VOLT	J14-1	-8.0 ----- -11.0V
A	J14-2	-8.0 ----- -11.0V
C	J15-1	-8.0 ----- -11.0V
D	J15-2	-8.0 ----- -11.0V
C	J16-1	-8.0 ----- -11.0V
L	J16-2	-8.0 ----- -11.0V
O	J17-1	-8.0 ----- -11.0V
W	J17-2	-8.0 ----- -11.0V

NOTE: H7100 POWER Supplies are not adjustable and must be repaired or replaced if out of spec.

7.2 If there are no problems, CPU should boot. M8235 will display a UPC of FF. If a UBA is present, the M8271 will display an MPC of 3.

8.0 DIAGNOSTIC TEST PROCEDURE

For the specific sequence of diagnostics to be run in any particular situation, or for the current MAST minimun test criteria, e.g.: pass counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are detailed step-by-step instructions for executing each individual diagnostic contained in the CHECKLIST.

8.1 Console terminal will display the following message upon completion of boot.

8.1.1
```
CPU HALTED,SOMM CLEAR,STEP=NONE,
CLOCK=NORM,
RAD=HEX,ADD=PHYS,DAT=LONG,FILL=00,
REL=000000
INIT SEQ DONE
HALTED AT 00000000

RELOADING WCS)
LOAD DONE, 00003200 BYTES LOADED
VER:  PCS=01  WCS=0D-12 FPLA=0D CON=V05-01-L

>>>
```

8.1.2 Remove RX1 Diskette in drive, and insert RX2 Diskette.

T<CR>

```
ZZ-ESKAB V12.0
01,02,03,04
NO. OF WCS MODULES = 0001
05,06,07,08,09,0A,0B<0C<0D<0E>0F<10,11,12,
13,1
,15,16,17,18,19,1A,1B,1C,1D,1E,1F,20,
SYS ID REG= 01200996
21,22,23,24,25,26,27,28,29,2A,2B,2C,2D,2E,
2F,
3,31,32,33,34,35,36,37,38,39,3A,3B,3C,3D,
END PASS 0001

MOUNT FLOPPY ZZ-ESSZAD & TYPE "DI"

MIC>
```

8.1.3 Remove RX2 Diskette in drive, and insert RX3 Diskette.

DI <CR>

```
3E,
CPU TR= 00000010
MS780 16K CHIP AT TR 01
MAX ADR+1= 00100000
DW780 AT TR 03
RH780 AT TR 08
RH780 AT TR 09
3F,40,41,42,43,44,45,46,47,48,49,4A,4B,4C,
4D,4E
MS780 16K CHIP AT TR 01
 ARRAY #: 00000000
 # SINGLE BIT ERRORS:                    00000000
 ARRAY #: 00000001
 # SINGLE BIT ERRORS:                    00000000
 ARRAY #: 00000002
 # SINGLE BIT ERRORS:                    00000000
 ARRAY #: 00000003
 # SINGLE BIT ERRORS:                    00000000
4F,
MS780 16K CHIP AT TR 01
  M8213 ROMS OK
50,51,52
MP FPA

END PASS 0001

     CPU HALTED,SOMM CLEAR,STEP=NONE,CLOCK=
     NORM
     RAD=HEX,ADD=PHYS,DAT=LONG,FILL=00,
     REL=00000000
     INIT SEQ DONE
     HALTED AT 00000000

     (RELOADING WCS)
     LOAD DONE, 00003200 BYTES LOADED
     VER: PCS=01 WCS=0D-12 FPLA=0D
     CON=V05-01-L


     >>>
```

8.1.4 Remove RX3 Diskette and mount VAX Instruction Diagnostic #1 RX8.

BOOT<CR>

```
                CPU HALTED
                INIT SEQ DONE
                LOAD DONE, 0001420 BYTES LOADED
DIAGNOSTIC SUPERVISOR, ZZ-ESSAA-6.1-370
7-AUG-1980 04:57:54

DS> ATT KA780 SBI KAO NO NO 0 0 <CR>
DS> SEL KA0 <CR>
DS> SET HA <CR>
DS> RUN EVAKB <CR>

..    PROGRAM:    VAX   Basic    Instructions
Exerciser,ZZ-EVKAB,  REV  2.2,  10  TESTS,  AT
05:03:52.76.  TESTING: KA0
.. END OF RUN. 0 ERRORS DETECTED. PASS
COUNT:1
TIME: 5-AUG-1980  11:52:41.98

DS>
```

8.1.5 Remove RX8 Diskette and mount VAX INST. DIAG. Diskette #2, RX25.

RUN EVKAC <CR>

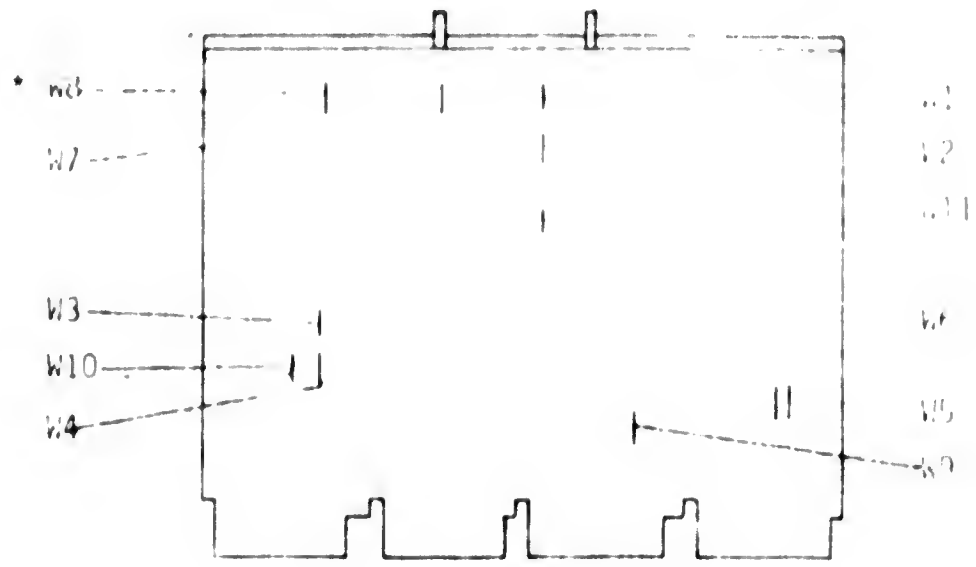
```
..PROGRAM: VAX Floating Point Instruction
Exerciser,  ZZ-EVKAC,  REV  2.0,  3  TESTS,  AT
05:06:34.89

TESTING:  _KA0

..  END  OF  RUN.  0  ERRORS  DETECTED.  PASS  COUNT:
1. TIME: 7-AUG-1980 05:08:55.78.
DS> RUN EVKAD <CR>

..PROGRAM: VAX Compatibility Mode Instructions
Exerciser,  EVKAD,  REV  1.2  4  TESTS,  AT  TESTING:
-KA0

..END OF RUN. 0 ERRORS DETECTED. PASS  COUNT:1
TIME: 1-JAN-1980 01:43:55.53.
```

```
DS> RUN EVKAE <CR>
..PROGRAM:   VAX   Privileged   Architecture
Exerciser, EVKAE, REV 1.2, 9 TESTS, AT TESTING:
_KA0
..END OF RUN. 0 ERRORS DETECTED. PASS COUNT: 1.
TIME: 5-AUG-1980 11:34:56.40

DS>
```

8.1.6 Remove RX25 Diskette from the drive and mount VAX CHANNEL DIAG. RX7.

```
      ATT DW780 SBI DW0 3 4  <CR>
DS> SEL DW0 <CR>
DS> RUN ESCBA <CR>
..PROGRAM: ZZ - ESCBA - 7.1 DW780 REPAIR
DIAGNOSTIC, REV 7.1, 54 TESTS, AT   11:38:11.71

TESTING: _DW0

UBA UNIT UNDER TEST IS _DW0

..END OF RUN. 0 ERRORS DETECTED. PASS COUNT: 1.
TIME: 5 AUG-1980 11:39:14.58

DS> ATT RH780 SBI RH0 8 5 <CR>
DS> ATT RH780 SBI RH1 9 5 <CR>
DS> SEL RH0 <CR>
DS> SEL RH1 <CR>
DS> RUN ESCAA <CR>

..PROGRAM:  ESCAA-REV,6.2  RH780  DIAGNOSTIC,REV
6.2, 20 TESTS, AT 11:40:37.22.
TESTING: _RH0 _RH1

RH0 BASE ADDRESS IS: 20010000
DRIVE [0] RESPONDED
*******NO MBE PRESENT ON MASSBUS*******
RH1 BASE ADDRESS IS: 20012000
DRIVE [1] RESPONDED
..  END OF RUN. 0 ERRORS DETECTED. PASS COUNT:
1. TIME: 5-AUG-1980 11:42:02.54

DS>
```

[END OF TEST]



M7264

FIGURE 1

*PRECONFIGURED

DO NOT CHANGE (W7 & W8)

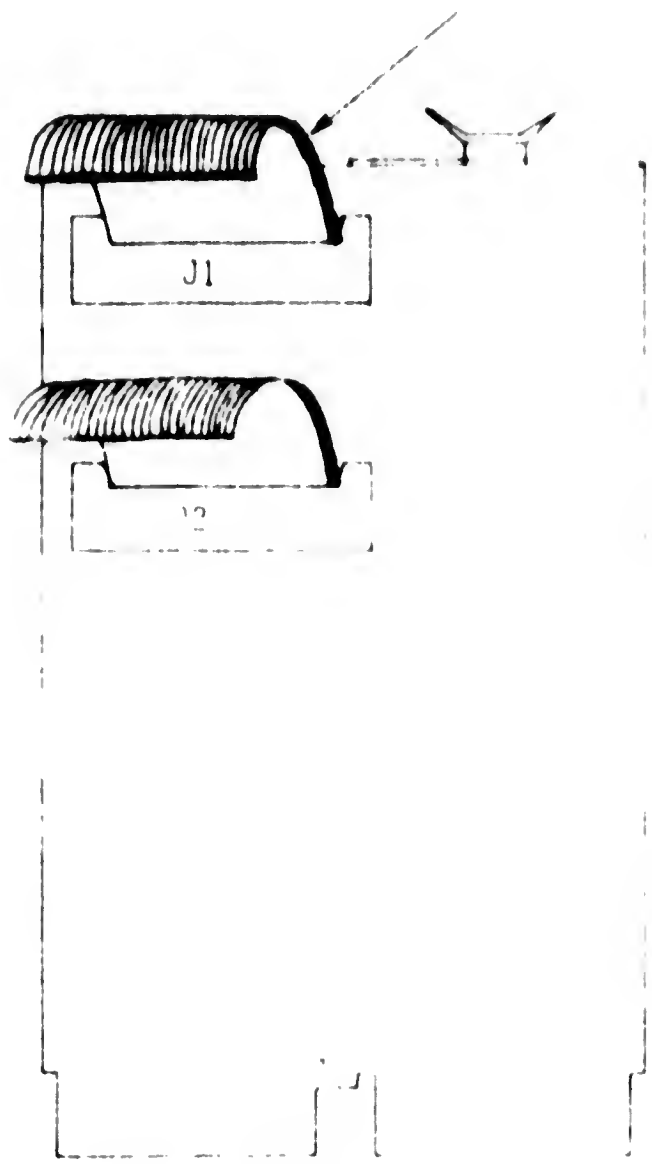


FIGURE 2

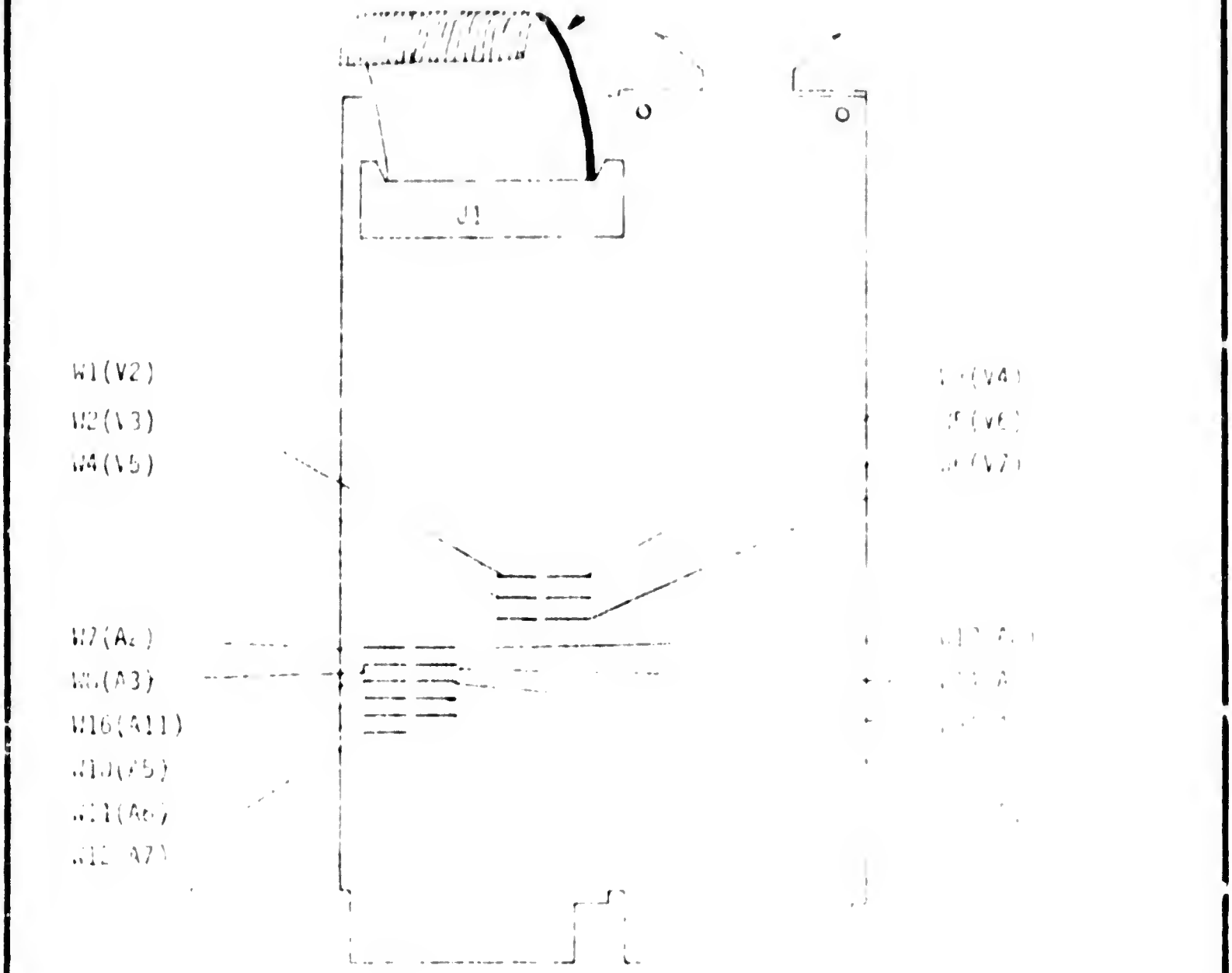
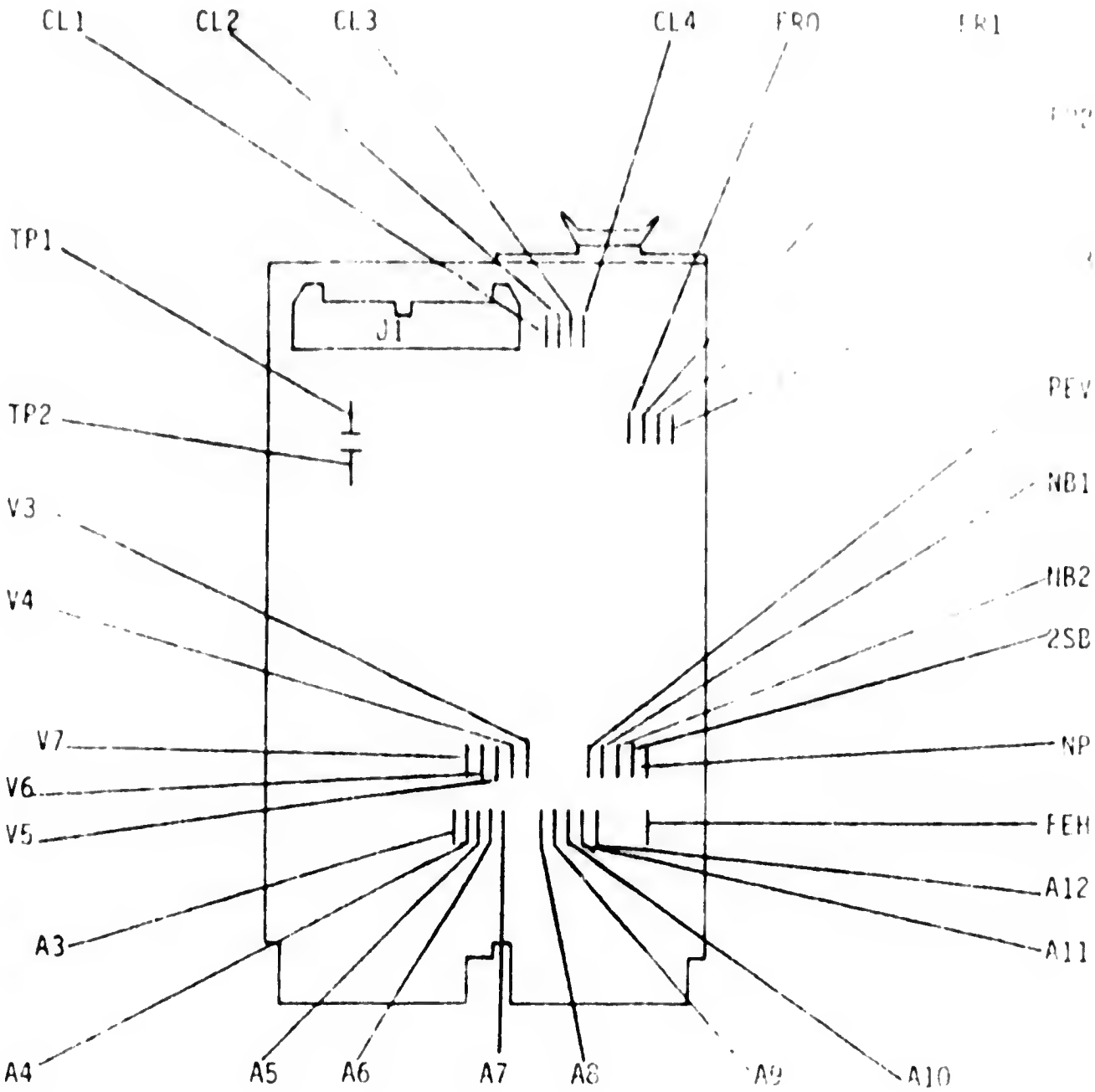
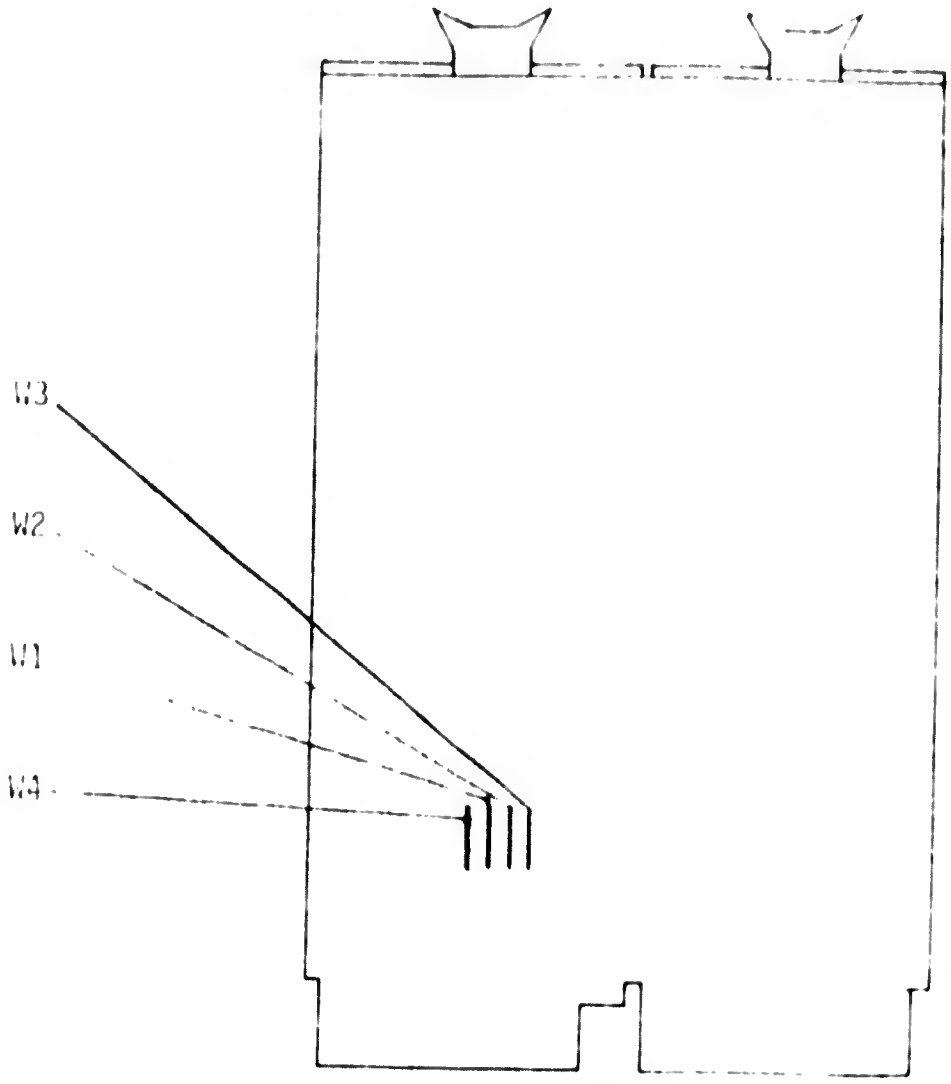


FIGURE 3



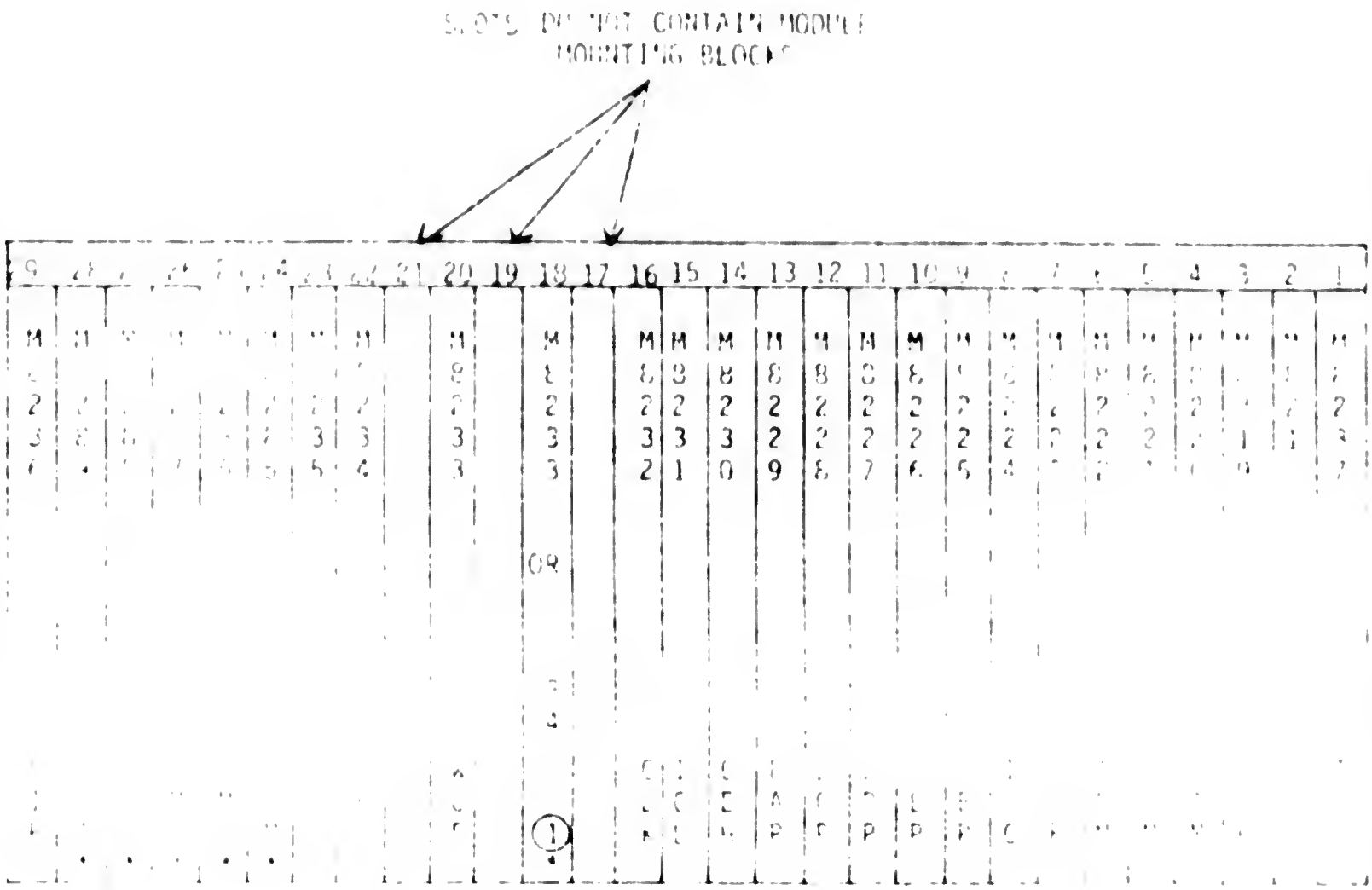
M7940

FIGURE 4



M7944

FIGURE 5



VIEW FROM MODULE SIDE

FIGURE 6

PINNING USED ON J10, J11, and J12.

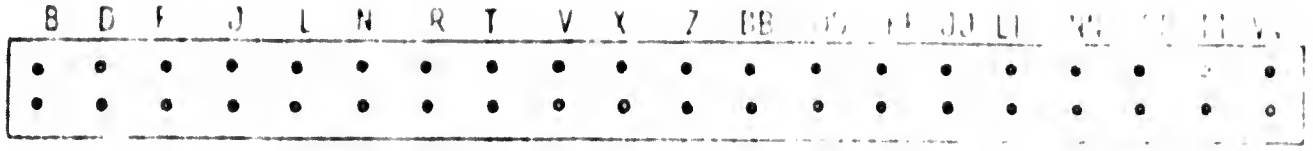


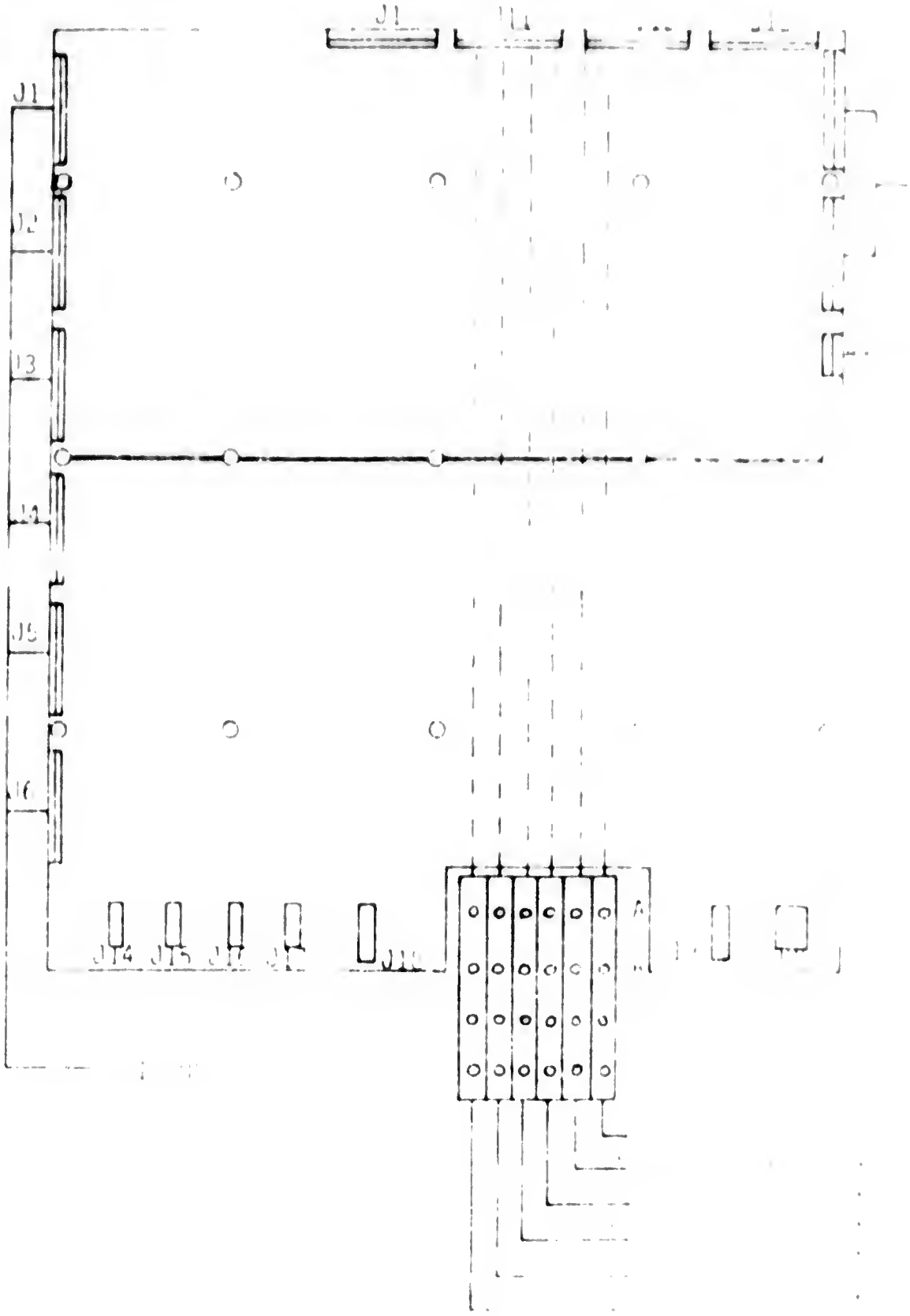
FIGURE 7

TR Select Pin

TITLE

MODULAR APPROACH TO SYSTEMS TEST

KZ50 Backpanel view



	SIZE	CODE	NUMBER	REV
	A	S?	MAV?100-0-0	B

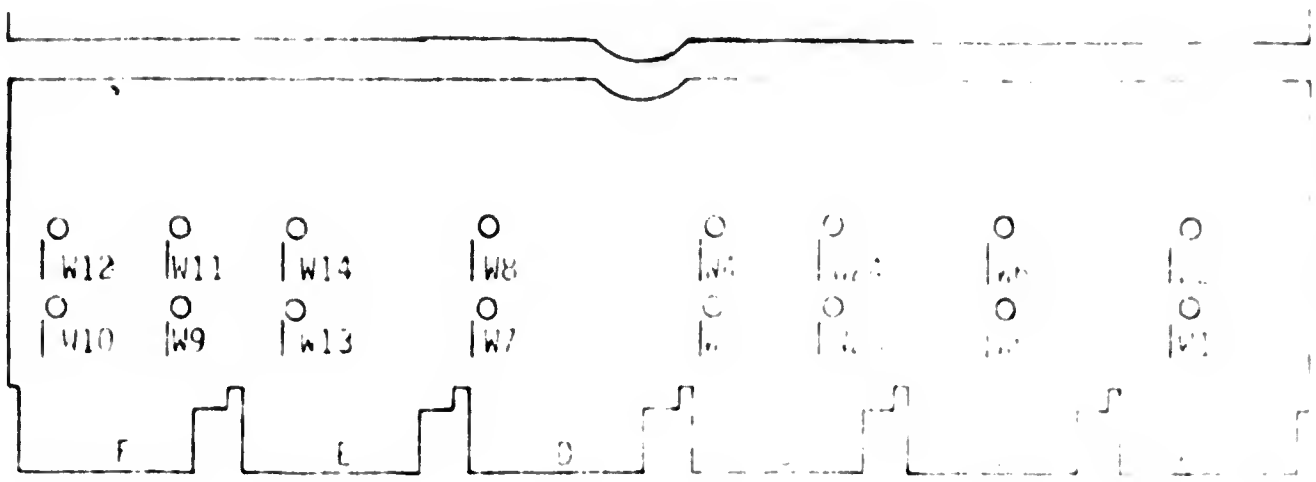
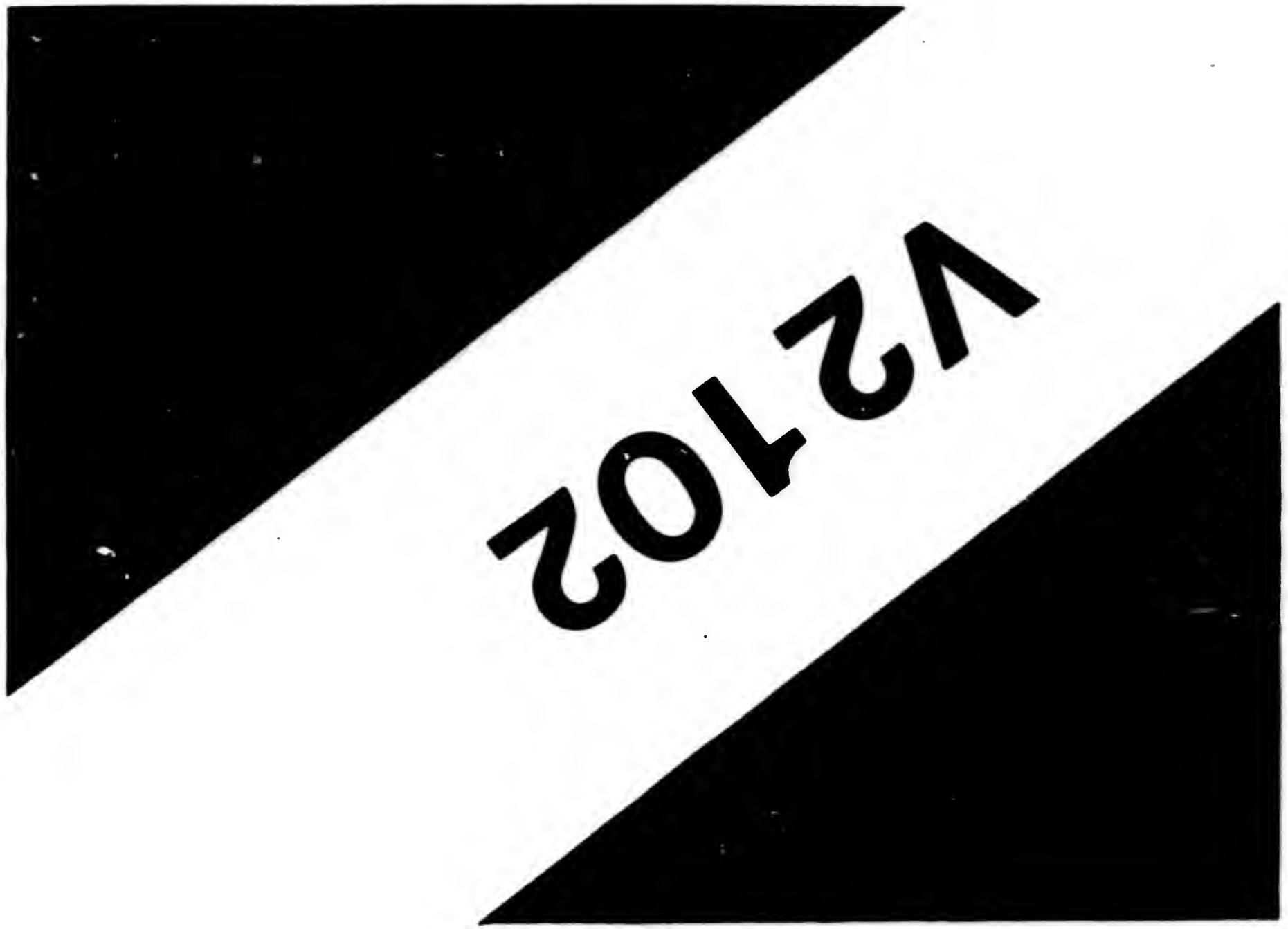


FIGURE [illegible]

NOTE: W1 through W14=In for FPA
W23 and W24=In for WCS


V2102

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION DATE 12/10

TITLE 11/750 MAST 1

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	NEW RELEASE	ML012	D. MONACO	8/19/81	Gerard Lyotte	8/19/81

ENG	APPD	SIZE	CODE	NUMBER	REV
Don Monaco		A		MAV 2102	A

1.0 INTRODUCTION:

1.1 The VAX-11/750 is the mid-range enhancement of the VAX-11 family. It carries with it all the architectural strengths of the VAX family including virtual addressing, both native mode and non-privileged PDP-11 compatibility mode instructions, and the VAX virtual memory operating system. The use of Gate Array Technology gives all this performance in a reliable compact 4 module CPU. The basic 11/750 is housed in a system cabinet 40in.H x 30in.D x 29in.W which includes the KA750, 256KB of memory, DD11-DK, DZ11 and TU-58 cassette tape drive.

1.2 The intent of this procedure is to establish the minimum test requirements necessary to test a VAX 11/750 CPU.

2.0 REFERENCE DOCUMENTATION:

2.1 Manuals

1.	750 Diagnostic System Overview	EK-VYD75-UG
2.	DZ11 User's Guide	EK-DZ110-UG
3.	TU58 User's Guide	EK-OTU58-UG
4.	Hardware Handbook	EB-17291-20
5.	VAX11 Architecture Handbook	EB-17580-18
6.	VAX11 Software Handbook	EB-18057-20
7.	VAX11 Technical Summary	EB-18816-20
8.	VAX Instruction Card	AV-D627A-TE
9.	750 Technical Description	EK-KA750-TD
10.	UBI Technical Description	EK-UB750-TD
11.	Memory System Tech. Des.	EK-MS750-TD
12.	Power System Tech. Des.	EK-PS750-TD
13.	750 Install. & Accept. Man.	EK-SI750-IA
14.	KC750 Microdiagnostic Tech. Man.	EK-KC750-TM
15.	Remote Diagnostics Users Guide	EK-KC750-UG

2.2 Prints

1.	11750	Field Maintenance Print Set MP-00838
2.	KA750	Field Maintenance Print Set MP-01024
3.	L0011	Field Maintenance Print Set MP-00858
4.	M8728	Field Maintenance Print Set MP-00857
5.	875	Field Maintenance Print Set MP-01022
6.	H7104C	Field Maintenance Print Set MP-01020
7.	H7104D	Field Maintenance Print Set MP-01021
8.	DZ11	Field Maintenance Print Set MP-00132

3.0 REQUIRED TEST EQUIPMENT:

3.1 VAX 11/750 with 256KB of memory.
3.2 Console terminal with E.I.A. such as an LA36 or LA120 or equivalent.
3.3 Appropriate load media.
3.4 H325 Test Connector
3.5 H3271 or H327 Test Connector
3.6 Optional test equipment

1. Oscilloscope Tektronix 465 or equivalent
2. D.V.M. accurate to .1 Vdc. at 15 Vdc..
3. KC750 (RDM module).
4. L9101 Comet Extender Module
5. H9048 Hex Extender Module

4.0 REQUIRED DIAGNOSTICS

4.1	VAX11 Hardcore Diagnostic	EVKAA.EXE
4.2	VAX11 Basic Instruction Exerciser	EVKAB.EXE
4.3	VAX11 Floating Point Instruction Exerciser	EVKAC.EXE
4.4	VAX11 Compatibility Mode Instruction Exe.	EVKAD.EXE
4.5	VAX11 Privileged Architecture CPU Cluster	EVKAE.EXE
4.6	11750 Specific CPU Cluster Exerciser	ECKAX.EXE
4.7	KA750 Cache T.P. Test	ECKAL.EXE
4.8	MS750 Memory Diagnostic	ECKAM.EXE
4.9	DW750 Diagnostic	ECCBA.EXE
4.10	Configuration Command File	CONFIG.COM
4.11	Diagnostic Supervisor	ECSAA.EXE
4.12	DZ11 8 Line Async Mux Test	EVDAA.EXE

4.13 Optional Microdiagnostics

VAX 11/750 Microdiagnostic Monitor	ECKAA.EXE
KC750 Microdiagnostic Test	ECKAB.EXE
VAX 11/750 Data Paths Microdiagnostic	ECKAH.EXE
VAX 11/750 Memory Interconnect Microdiag.	ECKAC.EXE
VAX 11/750 Memory Controller Microdiag.	ECKAD.EXE

5.0 SPECIAL INSTRUCTIONS:

5.1 Throughout this procedure, it is assumed that the user is familiar with DEC hardware, and the VAX 11/750.

5.2 Caution, no metallic jewelry should be worn while servicing this equipment, due to the high current capabilities of the power supply.

5.3 With battery backup installed, only loss of input power will invoke battery backup (turning off main breaker).

6.0 INSTALLATION & TEST SET-UP INSTRUCTIONS:

6.1 Unpacking instructions as received from High-Volume.

6.1.1 Save all boxes and packing material if it is needed to re-package a unit for shipment.

6.2 Visual checks:

6.2.1 With CPU unboxed check for problems such as (ref DEC standard 116):

A. Structural damage to cab and panels.

B. Bent or damaged backplane pins.

C. Loose power connections and broken wires.

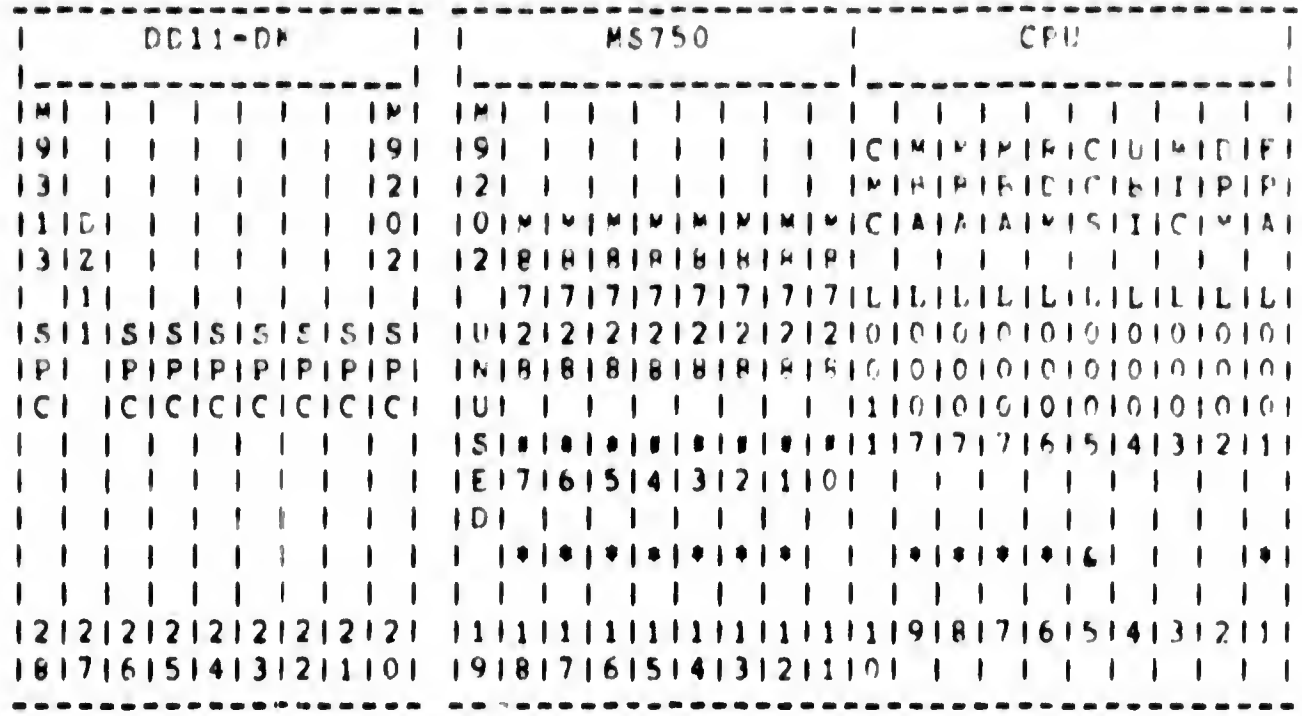
D. Loose hardware (e.g. mounting screws, cable hold downs, etc).

6.3 Hardware set up

6.3.1 KA750 Set Up

6.3.1.1 Module Utilization

11/750 MODULE UTILIZATION (module side)



* = OPTIONAL
& = WCS MOUNTS ON CCS MODULE (ref. figure 3)

NOTE: There are three methods of pin numbering and placement used in 11/750 CPU's.

PIN NUMBERING EXAMPLES:

DD11-DK	MS750	11/750
A01A1. . A01A2	A01A1. .A01A2	A0101. .A0102
A01B1 . .A01B2	A01B1. .A01B2	A0103. .A0104
A01C1. . A01C2	A01C1. .A01C2	A0105. .A0106
A01D1 . .A01D2	A01D1. .A01D2	A0107. .A0108.
|	|	|
A01V1. . A01V2	A01V1. .A01V2	A0193. .A0194

6.3.2 BAUD RATE SELECTION JUMPERS (ref. figure 1)

RATE	A	B	C	D
* 300	0	0	1	0
600	0	1	1	0
1200	1	1	1	0
2400	0	0	0	1
3600	1	0	0	1
4800	1	1	0	1
9600	1	0	1	1
19200	0	1	1	1
38400	1	1	1	1
PIN #	C00645	C00646	C00649	C00650
JUMPER TO GND	C00643	C00644	C00651	C00652

jumper in = 1

* Denotes standard console baud rate of 11/750 as shipped from manufacturing.

6.3.3 OPTION SLOT BUS GRANT JUMPERS (ref. figure 1)

TO SELECT	REMOVE JUMPER
BG4	A00X 67
BG5	A00X 69
BG6	A00X 73
BG7	A00X 77

X=SLOT 7,8,OR 9

6.3.4 HARDWARE REVISION LEVEL OF SYSTEM ID

(Undefined, for future reference)

BIT	PIN
0	B00456
1	B00455
2	B00454
3	B00453
4	B00450
5	B00449
6	B00448
7	B00446

6.3.5 Verify that the TOY (Time of Year) Clock battery backup is connected to of CPU backplane. (ref. figure 6)

6.3.6 L0011 CMC Module contains 4 IC sockets for the 11/750 boot roms.(ref. figure 7)

LOCATION	DEVICE	DEVICE SELECT
* E81	TU58	A
* F82	RK07	B
* F83	RL02	C
E84	XXXX	D

*Denotes installed in High Volume.

6.3.7 DZ11 Installation (ref. figure 4 and M.A.S.T. MAV 5145).

M7819 Switch Settings

E81 Address = 160100

1	2	3	4	5	6	7	8	9	10
off	off	off	on	off	off	off	off	off	off

E11 Vector = 300

1	2	3	4	5	6	7	8
on	on	on	on	off	off	on	or

6.4 Power Conversions (ref. figure 6)

All 11/750's will be shipped from High Volume as a 11/750-AA 120 volt 50/60 HZ. Because of this the following procedure is needed to convert the 11/750-AA to a 11/750-AB 230 volt 50/60 HZ.

NOTE:
HYPOT TESTING IS REQUIRED ON UNITS THAT ARE CONVERTED. Removal of the 11/750 side panel will make access to power plugs easier.

6.4.1 Required Material

70-16707-03	Power Conversion Kit
90-07A80-00	Tie Wrap (x3)
36-15180-00	Blank Serial Tag (x2)
36-15946-00	Product Variation Tag (x2)

6.4.2 Required Tools

#2 Phillips Screwdriver
Allen Wrench Set
Nut Driver or Socket Set
Tie wrap Tool

6.4.3 Work Steps For Conversion

Caution:
Due to high current capability of the power supplies, disconnect from power source before proceeding.

1. Open rear door on 11/750.
2. Remove rear power supply cover.
3. Remove rear access panel.
4. Remove left side panel on 11/750.
5. Disconnect P1, P2, P3 on the top of the Power Controller, and P1 , P2 on the rear of the Power Controller, then disconnect the 2.5 volt sense cable and unplug the 70-16908-00 (115 Volt)Blower Cord.
6. Cut the Line Cord free of shipping tie wraps.
7. Remove screws securing the 70-15929-00 (115 Volt) Power Controller.
8. Remove controller by sliding it out of the rear of the cab.
7. Install the 70-15929-01 (230 Volt) Power Controller with the hardware removed in the previous steps.

8. Disconnect the 70-16908-00 (115 Volt) Blower Cord from J1 of the Blower Assembly.
9. Connect the 70-16908-01 (220 Volt) Blower Cord to J1 of the blower assembly.
10. Connect P1, P2, P3 on the top of the Power Controller, and P1 , P2 on the rear of the Power Controller, then connect the 2.5 volt sense cable and plug in the 70-16908-01 (220 Volt)Blower Cord.
11. Tie wrap Line Cord in place for shipment.
12. Replace rear power supply cover.
13. Replace 11/750 side panel.
14. Replace Rear Access Cover.
15. Change Serial Tags and install Product Variation Tags (rear door and front rail) to reflect the new version.
16. Change 11/750 ECO Status Sheet to reflect new version.

7.0 POWER CHECKS (ref. figures 5 and 7)

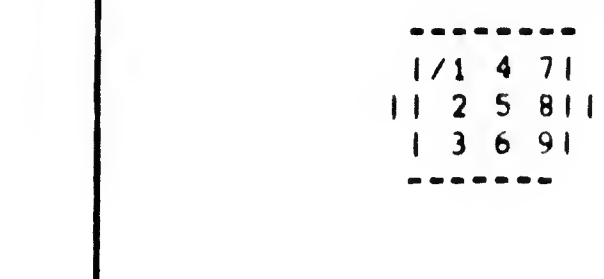
7.1 With power applied and the Rotary Key Switch on LOCAL. the following power indicators should be lit.

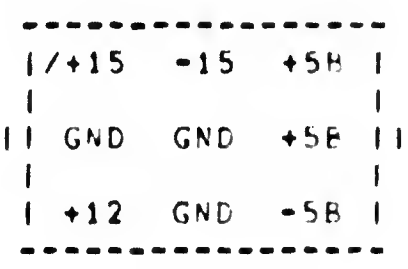
1. Green Power On located on Console Panel.
2. Orange power indicator on power controller.
3. Green DC OK indicator on power controller.
4. Green power indicator on memory arrays.
5. Green power indicator on memory controller.

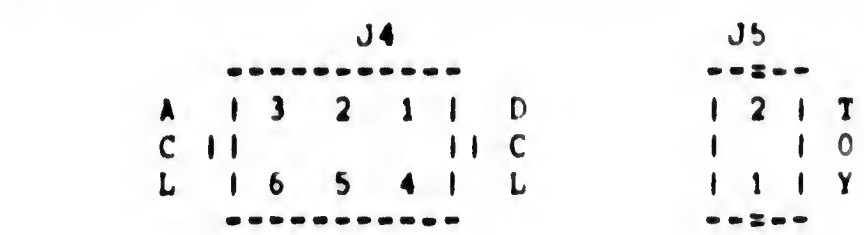
7.2 Voltages Supplied by H7104 Power Supply. (Non adjustable self monitored)

+2.5	V.D.C.	at	85.0 amps.
+5.0	V.D.C.	at	135.0 amps.
+5.0	V.D.C.	at	10.0 amps.
+12.0	V.D.C.	at	10.0 amps.
+15.0	V.D.C.	at	2.0 amps.
-5.0	V.D.C.	at	1.5 amps.
-15.0	V.D.C.	at	3.5 amps.

POWER REF. FOR J1,J2,J3







7.3 Optional Battery Backup (if applicable) (ref. figure 7)

7.3.1 Optional Battery Backup is installed as shown in figure 7.

1. Mount H7112 Battery Backup on volume installed brackets in lower left of CPU cab, as viewed from the front of the CPU.
2. Connect Battery Backup cable harness to J1 (battery backup harness plate).
3. Connect P4 of Harness assembly to J11 of H7112.
4. Connect H7112 line cord to J16 (unswitched) socket of power controller.

7.3.2 There are no indicators showing the state of the Battery Backup.
The only quick check is to deposit data into memory and then shut off the main breaker (CB1), wait 60 sec then apply power and check memory contents. During the power down, power indicators on memory arrays should be lit.

7.3.3 See section 8.10 of this document for more detail testing of Battery Backup.

8.0 DIAGNOSTIC TEST PROCEDURES:

NOTE:
Reference KC750 Microdiagnostics and Technical Manual EK-KC750-TM and the Microdiagnostic listings, for detail information on installation and use of KC750 and Microdiagnostics.

For the specific sequence of diagnostics to be run in any situation, or for the current MAST minimum test criteria, e.g.: pass-counts, etc., refer to the appropriate MAST CHECKLIST. Listed below are the detailed step-by-step instructions for executing individual diagnostics contained in the CHECKLIST.

NO ERRORS allowed on diagnostics.

Operator inputs will be underlined.

8.1 Stand alone diagnostic cassette load (ref. figure 5)

NOTE:

It is assumed that the CPU is in a power down state.

8.1.1 Set Boot Device Selection Switch to position A (Selects TU58)

8.1.2 Set Power On Action Switch to Boot on power up.

8.1.3 Insert cassette with EVKAA.EXE HARDCORE into the TU58 located in the 11/750 console panel.

8.1.4 Set Rotary Key Switch to LOCAL.

System powers up, Power light is on Console should print %%. The first % indicates beginning the micro verify routine. The second % indicates successful completion of the micro verify. Tape motion light on TU58 comes on

8.1.5 EVKAA.EXE will load and begin running, if successfully run, console will print.

EVKAA-5.0 done!

8.1.6 Insert cassette containing ECKAL.EXE Cache TB into TU58.

8.1.7 Press the Reset Button located on the 11/750 console panel.

Console should print %% tape motion light on TU58 will turn on and tape will begin loading.

8.1.8 ECKAL.EXE will load and begin running, if successfully run, console will print.

ECKAL-2.0 DONE!

8.2 Cassette Load of Diagnostic Supervisor

8.2.1 Insert cassette containing ECSAA.EXE Diagnostic Supervisor, into the TU58.

8.2.2 Press the Reset button located on the 11/750 console panel.

When boot is complete console will respond with the following.

```
DIAGNOSTIC SUPERVISOR, ZZ-ECSAA-5.4-121  DD-MMM-YYY
DS>
```

8.3 System Disk Load of Diagnostic Supervisor

8.3.1 Place correct media in system disk and spin disk up.

8.3.2 Set the Console Power on Action Switch to the Halt position.

8.3.3 Set the Device Select to A, B, C or D, whichever is your system device.

8.3.4 Depress the Console Reset Button, and wait for the console prompt.

8.3.5 Now type "B/10 DDCU" <CR>

Example:

```
>>>B/10 DMA0 <CR>
   --------------
```

When boot is complete console will print the following message.

```
DIAGNOSTIC SUPERVISOR, ZZ-ECSAA-5.4-121 DD-MMM-YYYY
DS>
```

8.4 Running The Diagnostic Supervisor

8.4.1 Before running any diagnostic the Diagnostic Supervisor must be configured. Following is an example of a dual RK07 11/750 system.

```
DS> ATTACH KA750 CMI KA0 NO NO YES 0 0 <CR>
    ---------------------------------------
DS> ATTACH DW750 CMI DW0 <CR>
    ------------------------
DS> ATTACH RK611 DW0 DMA 777440 210 5 <CR>
    -------------------------------------
DS> ATTACH RK07 DMA DMA0 <CR>
    ------------------------
DS> ATTACH RK07 DMA DMA1 <CR>
    ------------------------
DS> ATTACH DZ11 DW0 TTA 760100 300 5 FIA <CR>
    -----------------------------------------
DS> ATTACH VT100 TTA TTA0 <CR>
    -------------------------

NOTE:
      These ATTACH Commands may be located
      in a config command procedure.
      To run the command procedure input
      the following to attach devices.

DS> @CONFIG <CR>
    -----------

8.4.2 With devices to be tested configured
      into the system, type the following
      to select all devices for test.

DS> SEL ALL <CR>
    ------------

NOTE:
      It is assumed that the proper diagnostics
      are located on the load media being used.
      The following format will be used to
      illustrate running diagnostics under the
      Diagnostic Supervisor.

8.X Diagnostic name

DS> RUN XXXX <CR>          (how to start diagnostic.)
    -------------          (operator input indicator)
XXXXXXXXXXX                (beginning of run print out)
XXXXXXXXXXX                (special instructions)
XXXXXXXXXXX                (end of run print out)
```

8.5 EVKAB.EXE VAX Basic Instruction Exerciser.

```
DS> RUN EVKAB <CR>
    --------------
..PROGRAM: VAX Basic Instruction Exerciser, ZZ-EVKAB,
rev 2.0, 10 tests, at HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.6 EVKAC.EXE VAX Floating Point Instruction Exerciser.

```
DS> RUN EVKAC <CR>
    --------------
..PROGRAM: VAX Floating Point Instruction Exerciser,
ZZ-EVKAC, REV 1.0, 2 TESTS, AT HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.7 EVKAD.EXE VAX Compatibility Mode Instruction Exerciser.

```
DS> RUN EVKAD <CR>
    --------------
..PROGRAM: VAX Compatibility Mode Instruction Exerciser,
ZZ-EVKAD, REV 1.2, 4 TESTS, AT HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.8 EVKAE.EXE VAX Privileged Architecture Exerciser.

```
DS> RUN EVKAE <CR>
    --------------
..PROGRAM: VAX Privileged Architecture Exerciser,
ZZ-EVKAE, REV 1.0, 9 TESTS, AT HH:MM:SS
TESTING: _KA0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.9 ECCBA.EXE VAX 11/750(UBI), Dw750 Diagnostic

```
DS> RUN ECCBA <CR>
    --------------
..PROGRAM: ECCBA-REV 1.0 VAX 11/750(UBI), Dw750 Diagnostic
REV 1.0 32 TE... AT HH:MM:SS.
TESTING: _DW0
NO UBES SELECTED. SKIPPING TEST
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.10 ECKAX.EXE VAX 11/750 Specific CPU Cluster Exercicer.

NOTE:
Install a write enabled scratch tape into TU58
afte ECKAX is loaded into memory.

```
DS> LOAD ECKAX <CR>
    --------------
DS> ST/SE:ALL <CR>
    -------------

..PROGRAM: VAX 11/750 Specific CPU Cluster Exerciser - ZZ-ECKAX-1
REV 1.0 9 TESTS, AT HH:MM:SS
TESTING: _KA0

Before continuing, set the front panel switch to HALT/RESTART

Good Restart Parameter Block Subtest - This subtest
will restart itself if the RPB is properly interpreted.
Push the init switch to power fail...
%%

Bad Checksum Subtest - This subtest will halt the processor
with a halt code of 11. After this has happened the subtest
is restarted by typing S 100 <CR> on the console terminal.
Push the init switch to power fail...

%%

00000000  11
>>>S 100 <CR>
   ---------

Search for Good RPB - This subtest will restart itself
if the good RPB is found and interpreted properly.
Push the init switch to power fail...
%%

Warm start Flag Subtest - This subtest will halt the processor
with a halt code of 12. After this has happened the subtest
is restarted by typing S 100 <CR> on the console terminal.
Push the init switch to power fail...

%%

00000000  12
>>>S 100 <CR>
   ----------
```

```
Is this system equipped with battery back-up?
(if no, then set the front panel switch to the Halt position)
[(NO),YES]
WARNING: The front panel switch must be in HALT
         for this test to operate properly.

HALT expected with following printout:
00006136  06
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>

00006136
>>>D/G F 100 <CR>
   --------------
>>>C <CR>
   ------

HALT expected with following printout:
0000633F  04
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
0000633F  04

>>>D/G F 100 <CR>
   --------------

>>>C <CR>
   -----
HALT expected with following printout:
0000650C  04
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
0000650C 04

>>>D/G F 100 <CR>
   --------------
>>>C <CR>
   ------

HALT expected with following printout:
00006688 0A
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
00006688  0A

>>>D/G F 100 <CR>
   --------------
>>>C <CR>
   ------
```

```
HALT expected with following printout:
00006808  0A
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
00006808  0A

>>>D/G F 100 <CR>
   --------------
>>>C <CR>
   ------

HALT expected with following printout:
00006988  0A
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
0006988  0A

>>>D/G F 100 <CR>
   --------------
>>>C <CR>
   ------

HALT expected with following printout:
00006B08
To continue from console mode do the following:
D/G F 100 <CR> and then C <CR>
00006B08

>>>D/G F 100 <CR>
   --------------
>>>C <CR>
   ------
Exiting WCS test, WCS last address = 0.

Exiting WCS test, WCS last address = 0.


..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.11 ECKAM.EXE MS750 Memory Diagnostic.

NOTE:
First memory array is not tested, must have 512KB for test to run.

```
DS> RUN ECKAM <CR>
    --------------
.. PROGRAM: ECKAM-REV. 1.0 MS750 MEMORY DIAGNOSTIC, REV 1.0
11 TESTS, AT HH:MM:SS

HIGHEST LONG WORD ADDRESS IS :
MEMORY MAP VALID: 00003FFF (X)
SLOT(0) IS FULLY POPULATED (256KB)
SLOT(1) IS FULLY POPULATED (256KB)
SLOT(3) IS EMPTY
SLOT(4) IS EMPTY
SLOT(5) IS EMPTY
SLOT(6) IS EMPTY
SLOT(7) IS EMPTY
ROM NUMBER: A DEVICE TYPE: DD
ROM NUMBER: B DEVICE TYPE: DM
ROM NUMBER: C DEVICE TYPE: DL
ARRAY(1) SINGLE BIT ERRORS:
     ROW 0  -  0
     ROW 1  -  0
     ROW 2  -  0
     ROW 3  -  0
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

8.12 EVDAA.EXE DZ11 8 Line Async Mux Test

NOTE: This is an example of running internal wrap around mode (reference M.A.S.T. SP-MAV-5145 for detail testing).

```
DS> RUN EVDAA <CR>
    --------------

..PROGRAM: DZ11 8 LINE ASYNC MUX TEST,REV 2.1 21 TESTS
TESTING: _TTA

DEVICE _TTA IS BEING TESTED AS A M7819  (EIA) MODULE
..END OF RUN. 0 ERRORS DETECTED PASS COUNT: 1. TIME:
```

9.0 Console Routines

9.1 Console Commands

The console prompt is the same as the VAX 11/780 ">>>" and appears at the beginning of every line.

"^P" Enter 11/750 Console mode.

"^R" Enter RDM console mode.
RDM> (with RDM installed)

>>>E Examine command

>>>D Deposit command

>>>I<CR> Init command, invalidates TB, Cache, and does Processor Init and Unibus Init.

>>>T<CR> Test command, runs micro verify microroutine explained later.

>>>S ADR<CR> Start command, The command may have
>>>S <CR> an address argument following, or a carriage return if the PC is used. The start command does an init sequence before going to IRD1 of the macro instruction pointed to by the PC.

>>>C The continue command is the same as the Start command and starts macro execution at the address in the PC.

>>>N Next command is used to single step the macro instruction after the PC is loaded.

>>>B The Boot command in this example will boot the device selected by the front panel DEVICE switch.

>>>X ART load and dump command.

9.2 Command switches for examine and deposit commands.

Size Switches

/B	sets the data size to byte
/W	sets the data size to word
/L	sets the data size to long

Function Switches

/G	GPR
/I	IPR
/P	Physcial Memory
/V	Virtual Memory
<SP>P	PSL

9.3 Command Switches for Boot Console Command.

>>>B/X<CR>	Boot device selected by front panel DEVICE SELECT switch and inhibit Micro Verify Test.
>>>B/nnnn<CR>	Boot device selected by front panel DEVICE SELECT switch and pass a four digit number as software control flags to VMB.EXE in R5.
>>>B DDCU<CR>	Boot device specified by operator.

Examples:

>>>D/G/L F 1000<CR>	Put 1000 in PC.
>>>D/P 1000 00525:D0	Put code in address 1000.
>>>E/I 25<CR>	Examine cache disable register.
>>>I<CR>	Do an Init secuence.
>>>B/10/X DMA0<CR>	Boot Diagnostic Supervisor without micro verify from DMA0.

9.4 Console Command Error Codes.

9.4.1 If an illegal console command is attempted or command is aborted because of a microtrap or or some other condition a two digit error code is typed out and the console waits for new input.

Example:

>>>E P<CR>	Examine PSL
>>>E<CR>	Implies examine next location (illegal)
?11	Error Code typed by console.
>>>	Ready for input

Error Codes:

20 = Deposit or examine of memory failed.
(access violation, translation not valid,
bus error, TB or CS parity error.)
11 = Illegal access of an IPR or PSL.
29 = Binary transfer checksum error.
33 = Attempt to boot from unknown device type.
34 = Boot device not "A", "B", C", or "D".

9.5 Console Halt Error Codes

00 = Halt command typed at console.
02 = ^p halt or single macro instruction mode.
04 = Interrupt stack not valid.
06 = Halt instruction executed.
07 = Vector Bits <1:0>=3, Halt at vector
08 = Vector Bits <1:0>=2, WCS disabled or missing
0A = Change Mode Instruction executed on
Interrupt Stack.
0B = Change Mode Instruction executed and
Vector Bits <1:0> not = 0.
0F = Double Bus write Error Halt.
11 = Power up and can't find RPB, FPS1 at
RESTART/HALT.
12 = Power up warm start flag false FPS1 at
RESTART/HALT.
13 = Power up can't find good 64k of memory.
14 = Power up and booting, but bad Boot ROM.
15 = Power up and cold start flag set during
boot subroutine.
16 = Power up halt FPS1 at HALT position.
FF = Micro Verify Test failure.

9.6 Micro Verify

9.6.1 The Micro Verify Routine is run at power up and during Init sequences to the 11/750. At the beginning of Micro Verify a % will be outputed to the console. A successful completion will yield another % . A failure will output one of the following failure codes.

NOTE:
Reference KC750 Microdiagnostics and Technical Manual EK-KC750-TM and the Microdiagnostic listings for detail information on installation and use of KC750 if microdiagnostics are to be run.

Test Number	Test Name	Failure Code
1	R-Bus, W-Bus, D Reg Tests	@
2	M-Bus, O-Reg Test	C
3	Scratchpad Test	E
4	Explicit Addr.Test Mtemp	F
5	Explicit Addr.Test Rtemp	I
6	Explicit Addr.Test IPRs	J
7	Explicit Addr.Test GPRs	E
8	XB, IR, and OSP Test	O
9	XB, PC, and PC+Isize Test	Q
10	RNUM/D-Size Tests	P
11	RNUM/D-Size Tests	T
12	Cache Parity Error Test	X
13	TB Parity Error Test	[
14	Control Store Parity Error Test	]
15	Cache Test	^

EXAMPLE: Micro Verify Failure

```
%F       This indicates a failure of Mtemp Scratchpad
00000XXX FF  PC contains loop count or point at which
>>>          test failed and FF indicates micro
             verify failure.
```

9.7 VAX 11/750 BOOT58 Console Emulator

9.7.1 General

<location> = <value> or <register>

<value> = <number> or <shorthand>

<number> = Any nonnegative HEXADECIMAL number.

<register> = 0...F

<shorthand> = Any of the following:
"*" = Use last <location> specified.
"+" = Use last <location> +1.
"-" = Use last <location> -1.
"@" = Use contents of last <location>.

<loc_qual> = Any of the following:
"/P" = Physical Memory Address.
"/G" = General Register.
"/I" = Internal Processor Register.

<size_qual> = Any of the following:
"/L" = Longword
"/W" = Word
"/B" = Byte

<devspec> = A device spec of the form DDCU
DD = Generic device type (eg. DB)
C = Controller designator (A or B)
U = Unit number 0...9

<filespec> = A legal RT-11 filename NAME.TYPE
NAME = Any alphanumeric string of not more than 6 chars.
TYPE = Any alphanumeric string of not more than 3 chars a null is acceptable.

9.7.2 BOOTSR COMMANDS

BOOT [<devspec>]
Boot from the device specified. If no device is specified boot from default boot device. This command cannot be in an indirect command file.

DEPOSIT [<loc_qual><size_qual>] <location> <value>
Deposit <value> at location specified by <location>. The <location> is interpreted according to the qualifiers.

EXAMINE [<loc_qual><size_qual>] <location>
Displays the contents of <location> according to the qualifiers.

HELP
Displays BOOTSR HELP FILE.

LOAD <filespec>[/START:<value>]
Load a file from the boot device into memory starting at the address specified <number>. If no starting location is specified, load the file beginning at the first free location in memory.

START <value>

JMP <value>

NOTE:

All BOOT5B commands may be abbreviated to the least amount of significant characters. Since the first character of each command is unique this means all commands may be abbreviated to one character. (BOOT may be entered as "B").

Some processor registers are either read or write only. Attempting the wrong operation on such a register will yield unpredictable results.

9.8 VMB Primary Boot

9.8.1 BOOT is the program name for VMB.EXE, which is used for booting of system devices for VMS and the Diagnostic Supervisor. Following is a list of VMB errors.

%BOOT-F- Unknown processor	This indicates that the CPU is not a 11/750 or 11/780 check SID register for proper jumper configuration in the CPU type field on the backplane.
%BOOT-F-Unexpected Exception	This indicates that one of the following exceptions occurred. 1 Access Violation 2 Breakpoint Opcode 3 Reserved Operand 4 Thit Trap 5 Page Fault (TNV)
%BOOT-F-Unexpected Machine Check	This indicates some sort of Machine Check occurred. Check all adapters using console examine and deposit commands. Probably a timeout occurred.
%BOOT-F-Nonexistant Drive	Self explanatory.

%BOOT-F-Unable to locate Boot file	VMB can't find [SYSEXE] SYSBOOT.EXE or if bit 4 in R5 is set, VMB can't find [SYSMAINT]DIAGBOOT .EXE .
%BOOT-F-Bootfile not contiguous	Indicates that [SYSEXE] SYSBOOT.EXE or if bit 4 in R5 is set, [SYSMAINT] DIAGBOOT.EXE is not contiguous on system disk.
%BOOT-F-I/O error reading boot file	Indicates problem reading boot file from disk by SDID service.

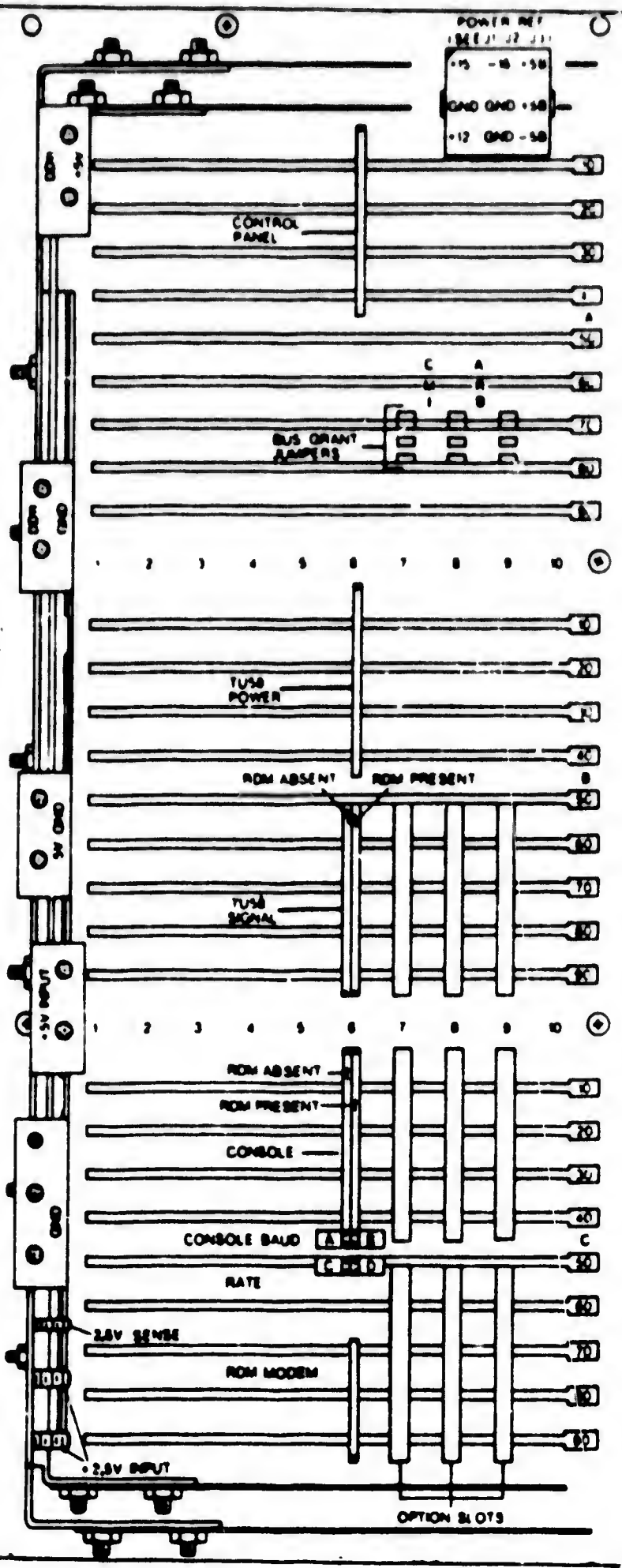


FIGURE 1
11/750 Backplane

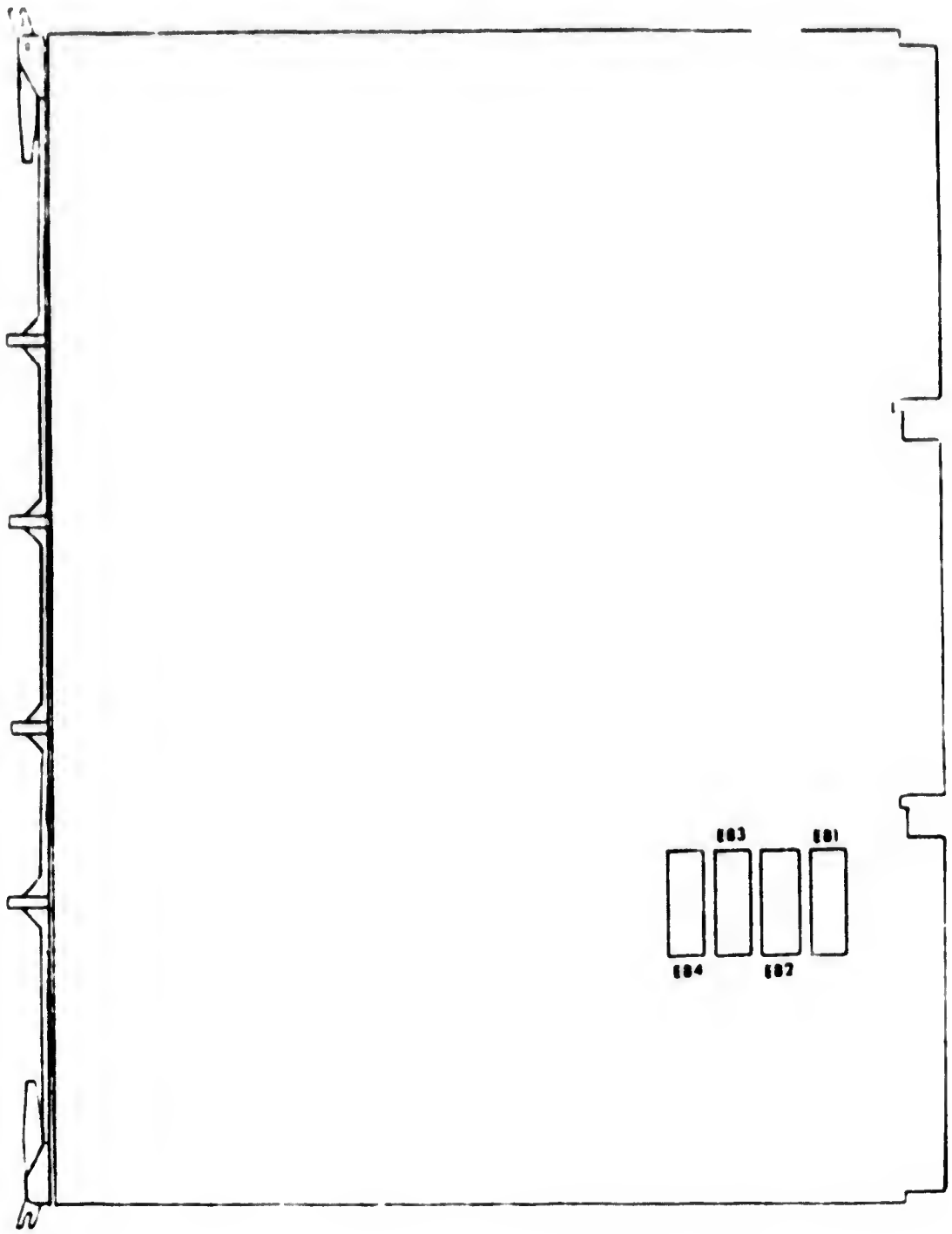


FIGURE 2
Comet Memory
Controller

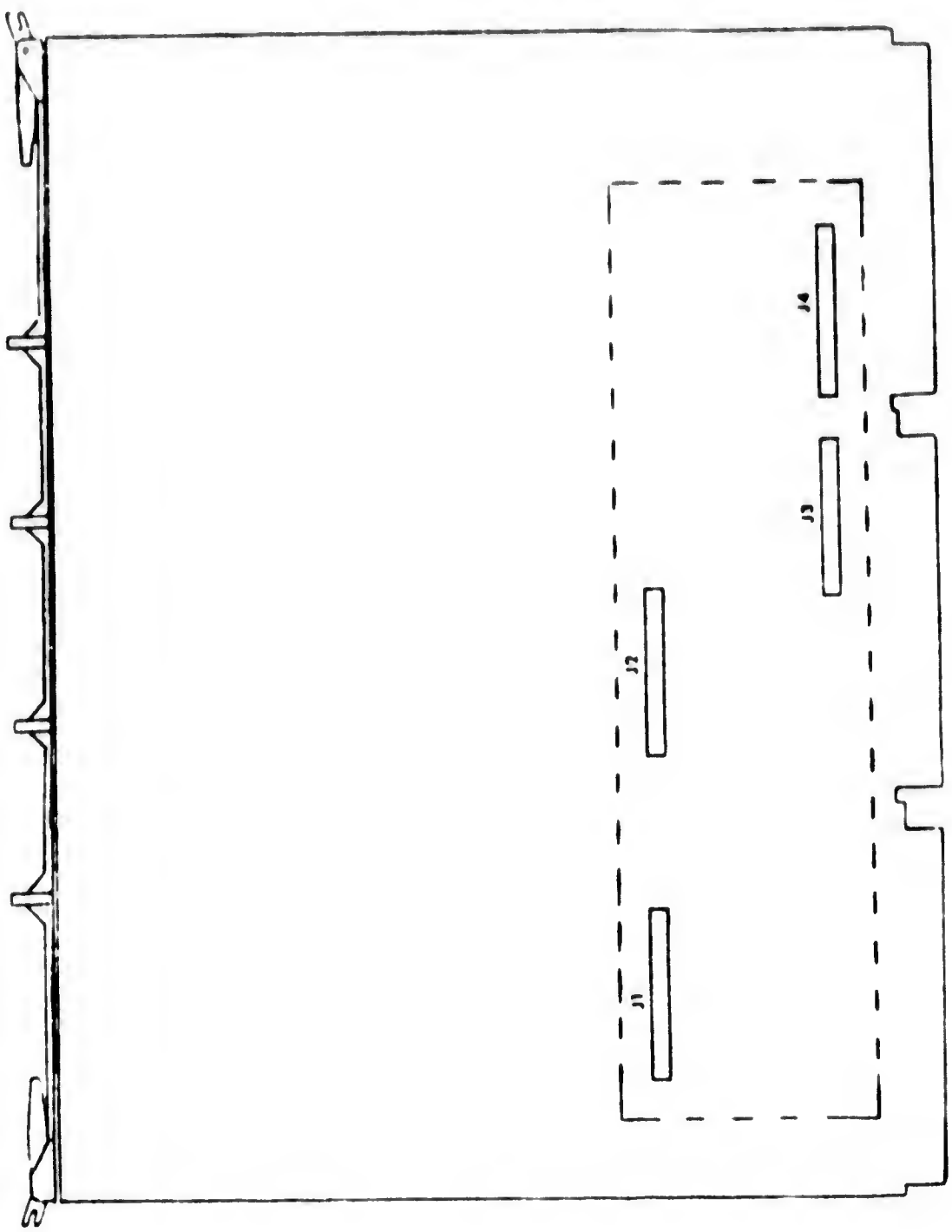


FIGURE 3
Comet Control Store
(WCS Mounted)

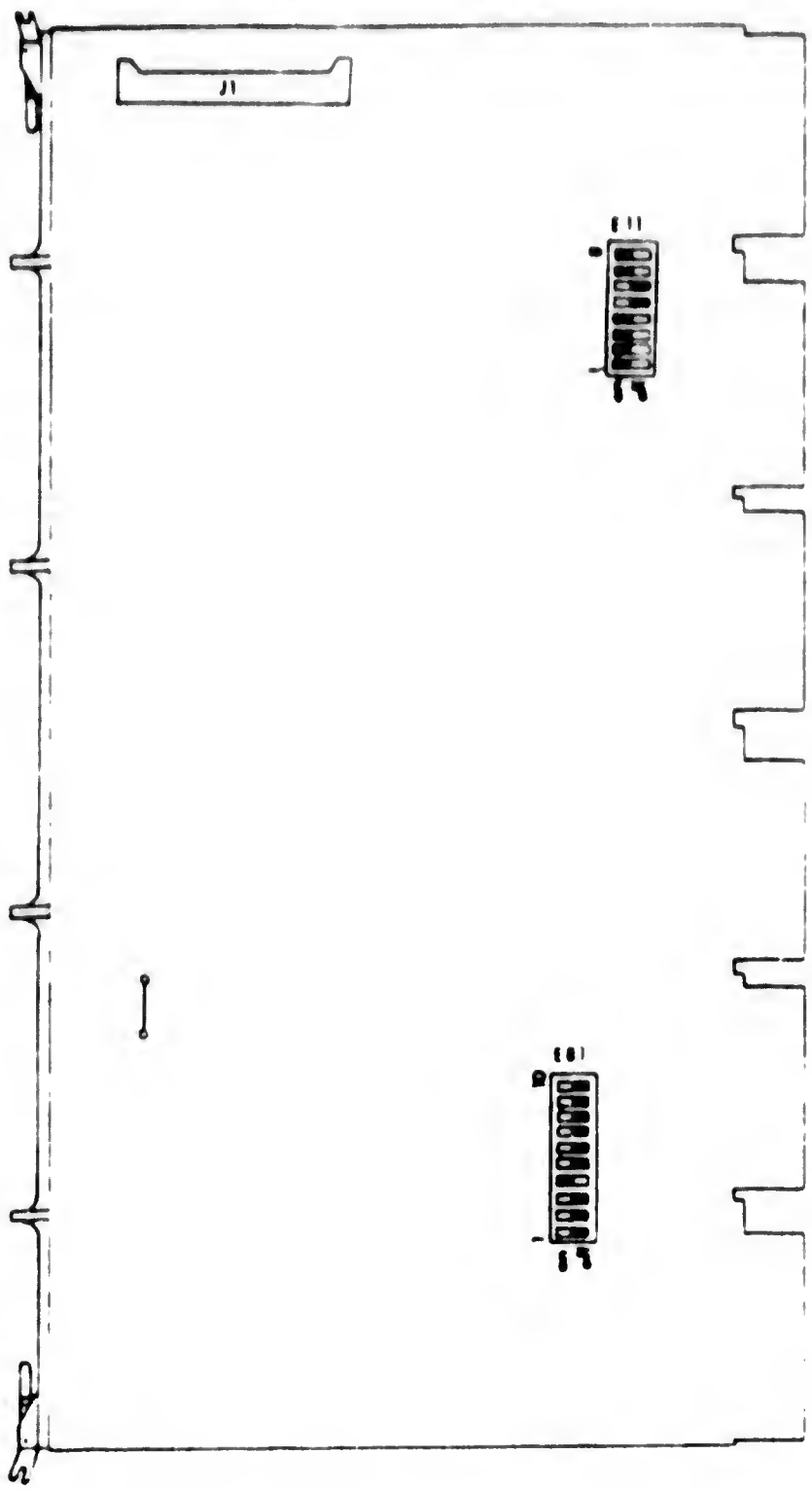


FIGURE 4
DB11-A Module

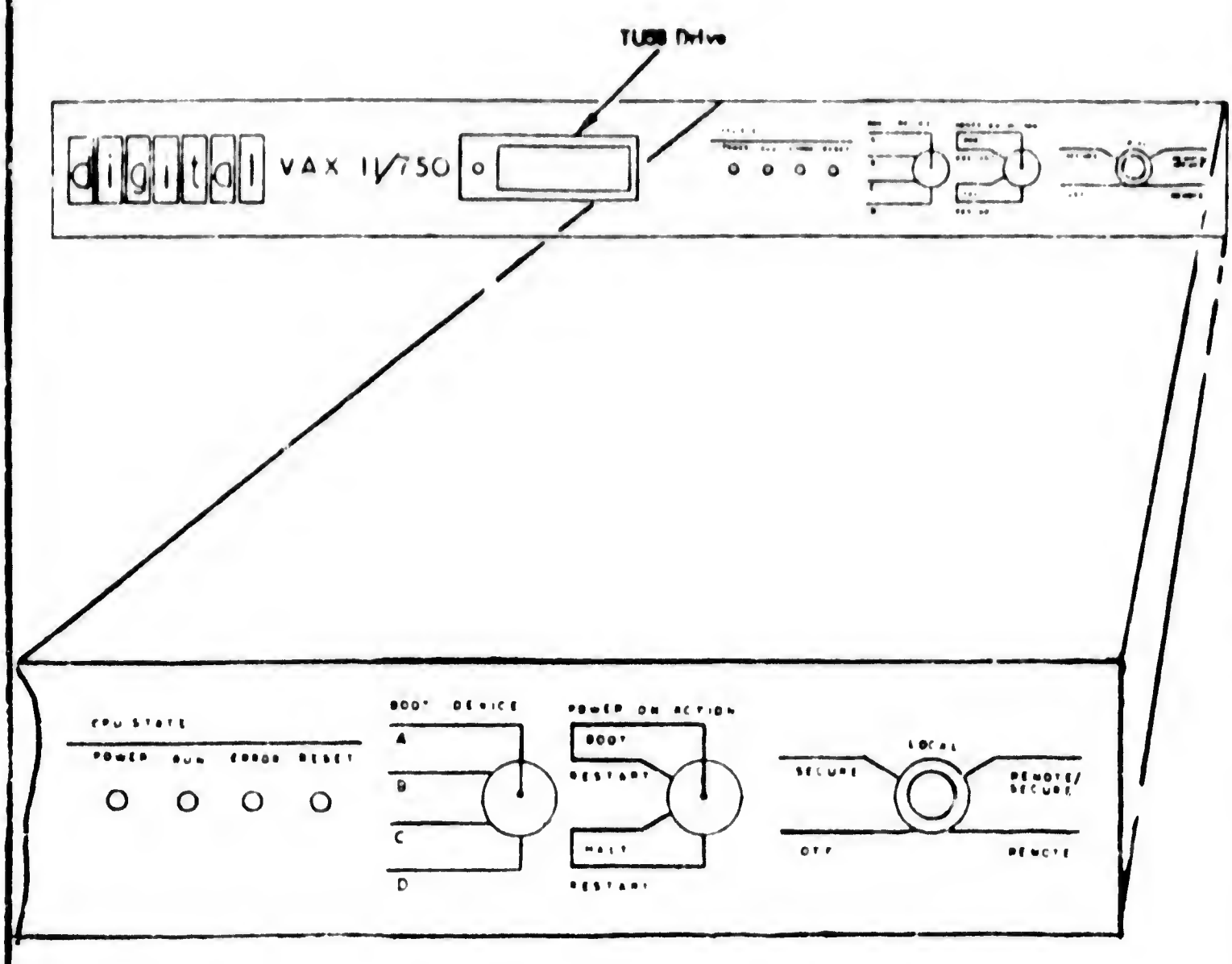


FIGURE 5
11/750 Control
Panel

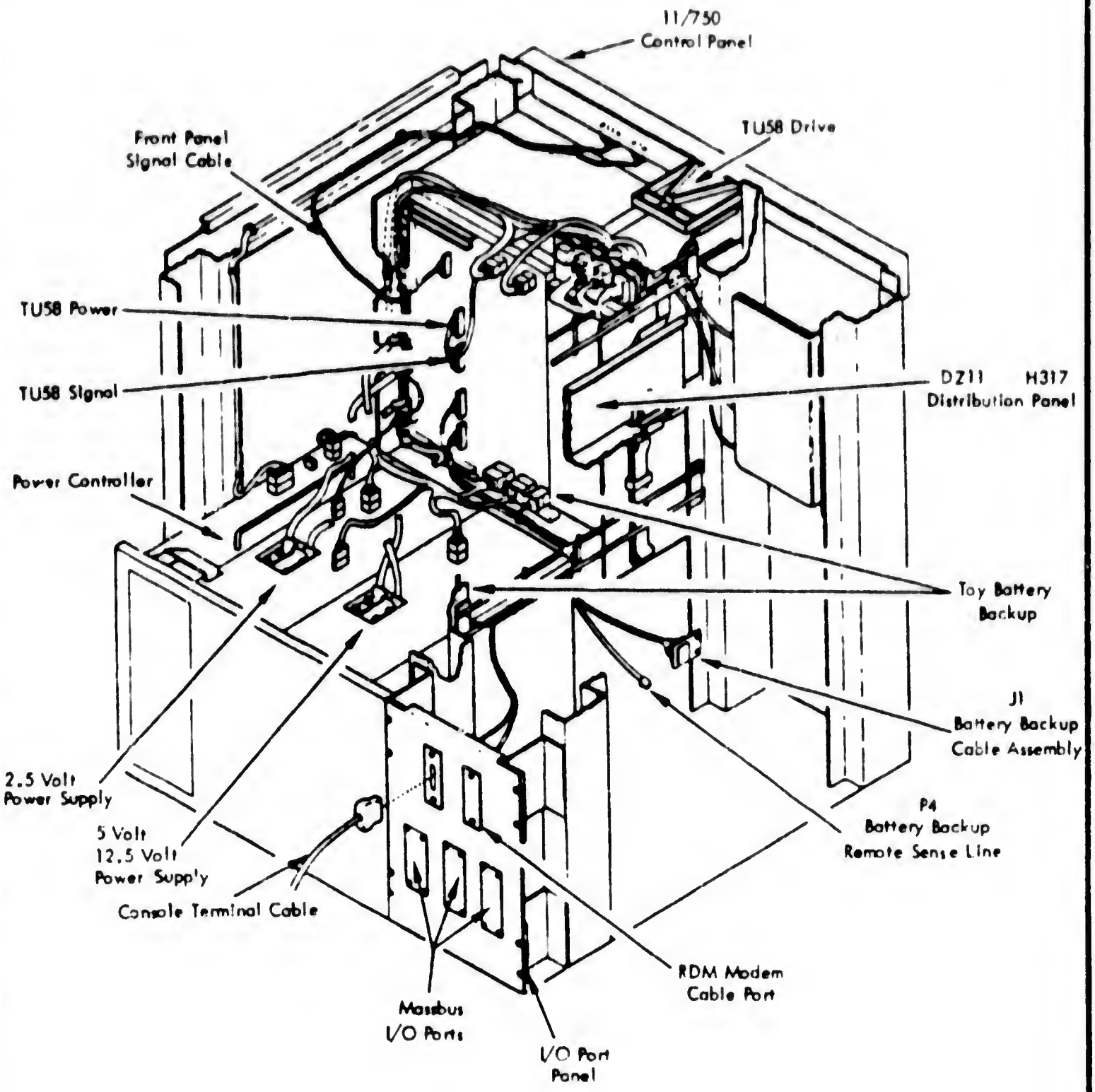


FIGURE 6
11/750 Rear View

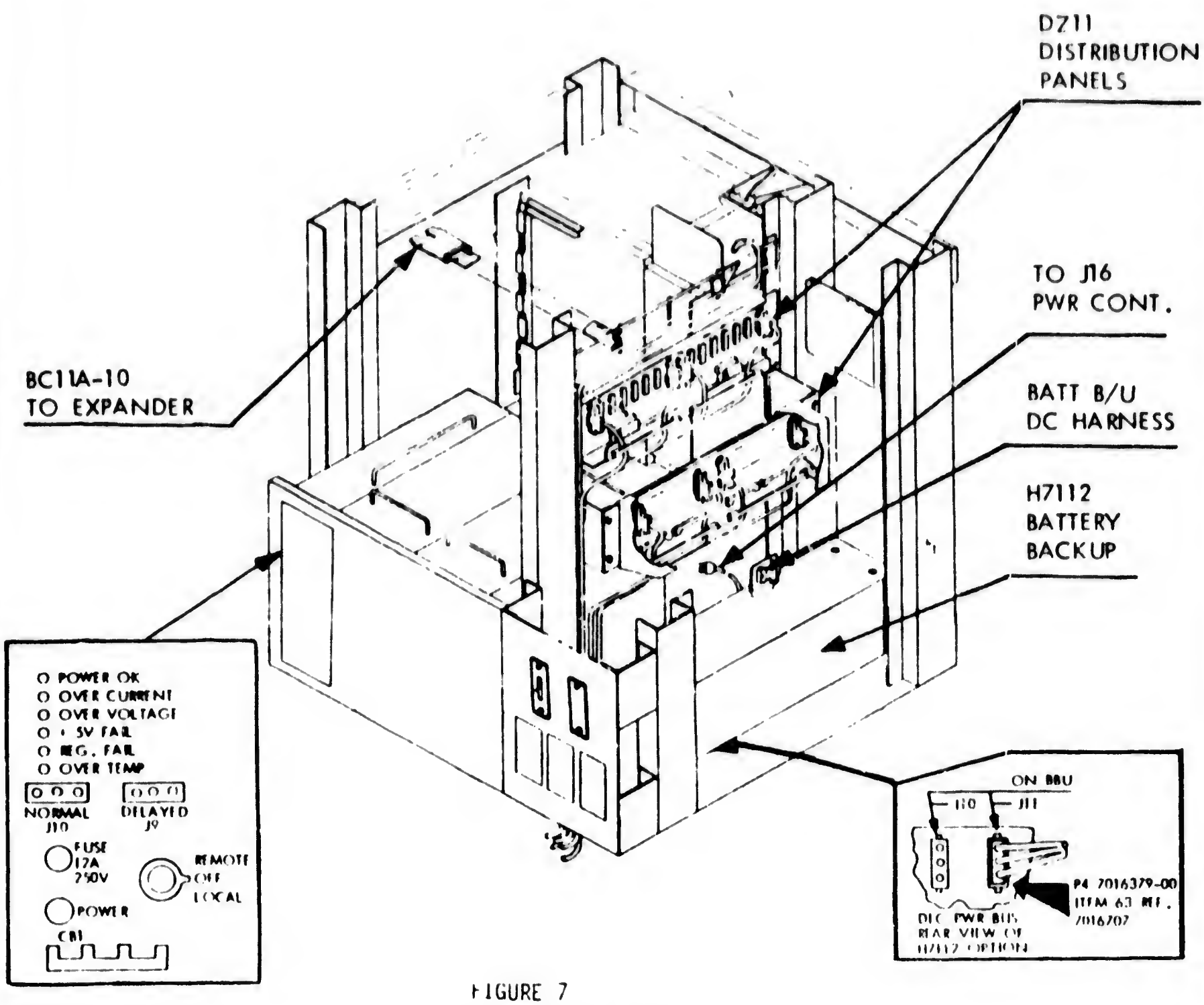


FIGURE 7

11/750 Side View
(Covers Removed)