IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

ADVANCED MICRO DEVICES, INC., et al.,

Plaintiffs and Counterdefendants,

v.

SAMSUNG ELECTRONICS CO., LTD, et al.,

Defendants and Counterclaimants.
/

No. C 08-986 SI

CLAIM CONSTRUCTION ORDER

On May 6 and 7, 2009, the Court held a claim construction hearing. Having considered the arguments of counsel and the papers submitted, the Court construes the disputed claims as follows.

BACKGROUND

Plaintiffs Advanced Micro Devices, Inc. and ATI Technologies, ULC ("AMD") brought suit against defendants Samsung Electronics Co., Ltd.; Samsung Semiconductor, Inc.; Samsung Austin Semiconductor, LLC; Samsung Electronics America, Inc.; Samsung Telecommunications America, LLC; Samsung Techwin Co.; and Samsung Opto-Electronics America, Inc. (collectively, "Samsung"), alleging infringement of United States Patents Nos. 5,545,592 to Iacoponi ("the Iacoponi patent"), 4,737,830 ("the '830 patent"), 5,248,893 ("the '893 patent"), 5,559,990 ("the '990 patent"), 5,377,200 ("the '200 patent"), 5,623,434 ("the '434 patent") and 6,784, 879 ("the '879 patent"). Samsung denied the alleged infringement of the AMD patents and asserted counter-claims against AMD, including unenforceability, invalidity, and infringement of United States Patent Nos. 6,407,429 ("the '429 patent"), 5,173,442 ("the '442 patent"), 5,091,339 ("the '339 patent") and 5,781,750 ("the '750 patent"), 5,470,065 ("the '065 patent") and 6,689,648 ("the '648 patent").

After filing a Joint Claim Construction Statement[1] the parties filed claim construction briefs, requesting that the Court construe seventeen disputed claim terms.[2]

LEGAL STANDARD

Claim construction is a matter of law. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996). Terms contained in claims are "generally given their ordinary and customary meaning." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (quotation omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention[.]" *Id.* at 1313. In determining the proper construction of a claim, a court begins with the intrinsic evidence of record, consisting of the claim language, the patent specification, and, if in evidence, the prosecution history. *Id.* at 1313; *see also Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir.1996). "The appropriate starting point . . . is always with the language of the asserted claim itself." *Comark Communications, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998); *see also Abtox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 (Fed. Cir. 1997).

Although claims are interpreted in light of the specification, this "does not mean that everything expressed in the specification must be read into all the claims." *Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 957 (Fed. Cir. 1983). For instance, limitations from a preferred embodiment described in the specification generally should not be read into the claim language. *See Comark*, 156 F.3d at 1186. However, it is a fundamental rule that "claims must be construed so as to be consistent with the specification." *Merck & Co., Inc. v. Teva Pharms. USA, Inc.*, 347 F.3d 1367, 1371 (Fed. Cir. 2003) (cited with approval by *Phillips*, 415 F.3d at 1316). Therefore, if the specification reveals an intentional

---

[1] In the Joint Claim Construction Statement, the parties agreed to the construction of one claim term. They agree that the term "in focus" in the '879 patent means "Actively being displayed and/or being worked upon." *See* Docket No. 92.

[2] The parties originally asked the Court to construe nineteen terms. In the course of their briefing on claim construction, they stipulated to constructions of two terms in the '893 patent. According to the parties' stipulation, (1) "self-aligned to the respective first and second opposed sides of the gate" shall be construed as "formed by a process in which the gate is used as a mask during source and drain implementation" and (2) "the depth of said first and second impurity regions" shall be construed as "the depth of the source and drain regions."

disclaimer or disavowal of claim scope, the claims must be read consistent with that limitation. *Phillips*, 415 F.3d at 1316.

Finally, the Court may consider the prosecution history of the patent, if in evidence. The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution. *See Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir.1995).

In most situations, analysis of this intrinsic evidence alone will resolve claim construction disputes. *See Vitronics*, 90 F.3d at 1583. Extrinsic evidence "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317. Courts should not rely on extrinsic evidence in claim construction to contradict the meaning of claims discernable from examination of the claims, the written description, and the prosecution history. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1308 (Fed. Cir.1999) (citing *Vitronics*, 90 F.3d at 1583). However, it is entirely appropriate "for a court to consult trustworthy extrinsic evidence to ensure that the claim construction it is tending to from the patent file is not inconsistent with clearly expressed, plainly apposite, and widely held understandings in the pertinent technical field." *Id.*

DISCUSSION

1. Claims in AMD's '990 patent containing disputed terms

The '990 patent, asserted by AMD, is entitled "Memories with Burst Mode Access" and teaches improvements to computer memory performance by making memory faster and more energy efficient. Claims 1-14, 20, 22-23 contain disputed terms, which are noted in italics.

> 1. A memory comprising:
> a plurality of rows of memory locations;
> a plurality of first registers, each first register for receiving a row address;
> a plurality of row decoders, each row decoder for activating a portion of a row identified by signals from one of said first registers;
> one or more *sense amplifiers* for amplifying contents of said memory locations in the row portions; and
> an output for providing output signals from said *sense amplifiers*,
> wherein at least two locations L1 and L2 in different rows having different row addresses in said memory can be read out to said output in *burst mode* such that the memory receives an address of one of said locations and provides in response contents

of a plurality of memory locations, including the locations L1 and L2, in the sequence of *consecutive addresses*, so that while one of said row decoders is activating a row portion comprising said location L1 and contents of said location L1 are being transferred from one or more of said *sense amplifiers* to said output, another one of said row decoders is activating a row portion comprising said location L2 and contents of said location L2 are being transferred from said location L2 to one or more of said *sense amplifiers*.

2. The memory of claim 1, said memory having a random mode in which the memory receives an address and provides in response the contents of a unique memory location,

wherein, both in *burst mode* and in random mode, while the contents of said location L1 are being transferred from one or more of said *sense amplifiers* to said output, the contents of said location L2 are being transferred from said location L2 to one or more of said *sense amplifiers*.

3. The memory of claim 1 wherein when the locations L1 and L2 are read out in *burst mode* and when the contents of said location L1 are being transferred from one or more of said *sense amplifiers* to said output and the contents of said location L2 are being transferred from said location L2 to one or more of said *sense amplifiers*, the *sense amplifiers* from which the contents of said location L1 are being transferred are enabled and the *sense amplifiers* to which the contents of said location L2 are being transferred are disabled, but these latter *sense amplifiers* become enabled subsequently for amplifying the contents of said location L2.

4. The memory of claim 1 wherein:

said memory comprises k pluralities S-1, . . . , S-k of locations wherein k is a number of said pluralities and is greater than or equal to two;

for each plurality S-i, said *sense amplifiers* can receive simultaneously the contents of number m of locations from said plurality S-i, wherein m is a positive integer; and

time tARA does not exceed m * (k-1) * (tOE), wherein:

tARA is measured from the time that an address of a location is made available to said memory to the time when one or more of said *sense amplifiers* develop an output signal indicative of the contents of said location; and

tOE is the time to transfer an output of any one of said sense amplifiers to said output of said memory.

5. The memory of claim 1 wherein, in *burst mode*, a time in which each location of said plurality except said one of said locations is read out to said output after a previous location has been read out to said output is shorter than a time in which said one of said locations is read out to said output after said address of said one of said locations has been received by said memory.

6. The memory of claim 1 wherein said memory is fabricated in an integrated circuit.

7. The memory of claim 1 further comprising:

a plurality of second registers, each second register for receiving at least a portion of a column address; and

a circuitry for each second register for selecting in response to signals from one of the second registers a plurality of columns to be read by the *sense amplifiers*.

8. A memory comprising:

a set of *consecutively addressed memory locations L1, . . . Ln*;

a plurality of *sense amplifier* circuits for amplifying contents of said memory locations; and

an output for providing output signals from said plurality of *sense amplifier* circuits,

wherein said memory has a *burst mode operation* for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of *consecutive addresses* with wrap around so that the next

location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of *sense amplifier* circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of *sense amplifier* circuits for amplification and subsequent transfer to said output, and

wherein said memory further comprises a control circuit for selectively enabling said *sense amplifier* circuits so that said control circuit enables a *sense amplifier* circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said *sense amplifier* circuits at the same time.

9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only:

(1) the *sense amplifier* circuit whose output signals are being transferred to said output of said memory, and

(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.

10. The memory of claim 7 wherein:

said set of locations comprises k subsets S-1, . . . , S-k wherein k is greater than or equal to two, such that, for a positive integer m and for any subset S-i, the contents of m *consecutively addressed locations* from said subset S-i can be transferred simultaneously to said plurality of *sense amplifier* circuits; and

in said operation, time tARA does not exceed m * (k-1) * (tOE), wherein:

tARA is measured from the time that an address of the first location to be read out in said operation is made available to said memory to the time when said plurality of *sense amplifier* circuits develops an output signal indicative of the contents of said first location; and

tOE is the time to transfer the contents of any one of said locations from said plurality of *sense amplifier* circuits to said output.

11. The memory of claim 8 wherein, in said operation, each location to be read out except the first location to be read out is read out to said output in a shorter time than the first location to be read out.

12. The memory of claim 8 wherein the sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.

13. The memory of claim 7 wherein in said operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:

the first location to be read out in said operation is read out to said output after time tARA+tOE wherein:

tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of *sense amplifier* circuits develops an output signal indicative of the contents of said first location; and

tOE is the time to transfer the contents of any one of said locations from said plurality of *sense amplifier* circuits to said output of said memory; and

every other location to be read out in said operation is read out to said output within time tOE.

14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.

20. An *integrated memory* comprising:

an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have *consecutive addresses*;

one X-decoder for each subarray;

one X-register for each X-decoder;
one Y-decoder for each subarray;
one Y-register for each Y-decoder;
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;
a plurality of *sense amplifier* circuits for each subarray, each *sense amplifier* circuit for amplifying signals from a column selected by the Y-select circuit of the subarray;
a memory output; and
a control circuit for selecting one of the *sense amplifier* circuits to provide data to the memory output,
wherein in a *burst mode read operation*, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.

22. The memory of claim 20 wherein in the *burst mode read operation* while data from the *sense amplifier* circuits of one of the subarrays are provided to the memory output, the *sense amplifier* circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.

23. The memory of claim 20 wherein in the *burst mode read operation*, the control circuit enables the *sense amplifier* circuit selected to provide data to the memory output and at the same time disables one or more *sense amplifier* circuits not selected to provide data to the memory output.

A. "Integrated memory" (claims 20, 22-23)

The parties dispute the meaning of "integrated memory" in independent claim 20 and dependent claims 22 and 23. Samsung argues that this term should not be construed because it appears in the preamble to claim 20 and is not a limitation on this claim. The Court disagrees. The '990 patent refers to "memory" in the preambles to claims 1-14 but refers to "integrated memory" only in claim 20, 22, and 23. The Court will assume that "integrated" was inserted before "memory" in the preamble to claim 20 in order to differentiate the type of memory disclosed in this claim. *See Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004) ("[W]hen an applicant uses different terms in a claim it is permissible to infer that he intended his choice of different terms to reflect a differentiation in the meaning of those terms.").

The parties dispute whether the "integrated memory" in claim 20 is limited to memory that is fabricated in a single integrated circuit. AMD's proposed construction of "integrated memory" is "a memory fabricated in a single integrated circuit." Samsung proposes "a memory containing one or more integrated circuits." The Court finds that AMD's construction has more support in the intrinsic evidence.

The '990 patent discloses both memories formed in one integrated circuit and memories without this limitation. For example, independent claim 1 teaches "a memory," while dependent claim 6 teaches, "The memory of claim 1 wherein said memory is fabricated in an integrated circuit." 13:13 and 14:16-17; *see also* Claims 8 and 14. The specification also states that "some embodiments are not integrated into one integrated circuit." 13:8-9. Under AMD's proposed construction, the inclusion of the word "integrated" teaches that claim 20 discloses memory fabricated in a single integrated circuit. Samsung's proposed definition renders "integrated" superfluous because memory is necessarily fabricated in at least one integrated circuit. Accordingly, the Court adopts AMD's proposed construction of "integrated memory."[3]

B. "Burst mode," "burst mode operation," "burst mode read operation" (claims 1-14, 20, 22-23)

"Burst mode" memory processing was prior art to the '990 patent. 1:8-10. Burst mode processing improved on serial processing, in which data from several memory locations[4] had to be transmitted one location at a time. Decl. of Andrew Wolfe in Supp. of AMD Br. ("Wolfe Decl.") ¶ 31. In contrast, burst mode made memory processing faster by allowing data from several memory locations to be transferred at the same time. *Id.* ¶ 30.

AMD proposes construing "burst mode" as "a serial transfer mode in which a memory transfers the contents of a plurality of locations in response to the address of one location." Samsung argues that "burst mode" means "a mode for sequentially accessing memory locations in which the memory receives the address of one memory location and provides in response the contents of a plurality of

[3] As the meaning of this term is evident from the intrinsic evidence, the Court need not consult the expert opinions offered by both parties. *See* Decl. of Andrew Wolfe (for AMD) and Decl. of Richard Pashley (for Samsung).

[4] "Memory locations" are cells that store data.

consecutive memory locations."[5] The parties agree that in burst mode, the memory receives the address[6] of a single memory location and responds by providing data from multiple memory locations with consecutive addresses. They disagree as to whether the multiple memory locations are themselves consecutive: Samsung argues that the locations must be consecutive; AMD argues that while the addresses are consecutive, the locations are not necessarily consecutive.

The Court agrees with Samsung that in the context of the '990 patent, "burst mode" provides consecutive memory locations with consecutive addresses. First, this limitation is provided by the specification. In the "background of invention" section, the specification states, "When a memory is read sequentially (that is, consecutive reads access memory locations at consecutive addresses), the memory access can be made faster by reading from the array several *consecutive* locations simultaneously. Such a 'burst mode' access is provided by memory 202 of Fig. 2." 1:36-41 (emphasis added). The specification explains why burst mode allows for faster memory performance: "Since only one address decoding operation and only one memory array access are performed to read four *consecutive* memory locations, the memory reads are sp[ed] up." 1:47-51 (emphasis added). The specification also explains that in some embodiments, the invention improves burst mode processing by allowing the "burst mode read" to "start at any location and [to] . . . continue for any number of locations." 1:58-61. This "boundaryless burst mode access" allows "any number of locations, not only groups of four locations, [to be] . . . read *consecutively* in burst mode. Sequential memory access is consequently quite fast." 1:61-64.

Second, Samsung's proposed definition is taken from a brief filed by AMD when it appealed the Patent Trademark Office's ("PTO") initial rejection of the '990 patent. *See* Decl. of Aaron R. Fahrenkrog in Supp. of AMD Br. ("Fahrenkrog Decl."), ex. G (Jan. 26, 1995 Office Action). In the "summary of the invention" section of its appellate brief, AMD wrote, "Burst mode access is a sequential access in which the memory receives the address of one memory location and provides the

---

[5] AMD construes "burst mode operation and "burst mode read operation" as "a serial transfer in which the contents of a plurality of locations are provided in response to the address of one location." Samsung argues that these terms should receive the same construction as "burst mode."

[6] An "address" is an identifier for a memory location.

contents of a plurality of consecutive memory locations." *See* Fahrenkrog Decl., ex. I (Sept. 27, 2005 Br.) at 2.

AMD points out that its construction of "burst mode" is taken from AMD's request for reconsideration, filed on April 27, 1995. In this filing, AMD responded to the PTO's conclusion that claim 2 merely recited a serial transfer. AMD attempted to distinguish the "burst mode" in claim 2 from the prior art as follows: "A burst mode transfer as claimed in claim 2 is not any serial transfer but a serial transfer in which the contents of a plurality of locations are provided in response to the address of one location." Fahrenkrog Decl., ex. H (Apr. 27, 1995 Amendment after Final Office Action) at 4. AMD is correct that in this document, it did not specify that the "plurality of locations" were consecutive. This omission is not dispositive, however, because there is no evidence that AMD was attempting to distinguish the invention on this basis. Instead, AMD focused on the innovation of transferring data in different rows having different row addresses. *See id.* (The prior art "does not teach or suggest transferring data in different rows having different row addresses in response to the same address . . . as recited in Claim 2.").

Accordingly, the Court adopts Samsung's construction of "burst mode."

C. "Consecutive addresses"; "consecutively addressed memory locations L1, . . . Ln"; "the locations L1 and L2, in the sequence of consecutive addresses" (claims 1-14, 20, 22-23)

AMD argues that the terms "consecutive addresses"; "consecutively addressed memory locations L1, . . . Ln"; "the locations L1 and L2, in the sequence of consecutive addresses" need no construction. Samsung proposes the following definition: "A set of addresses following one after the other in order wherein each memory location represents a memory cell, or cells, associated with a single address."

The Court agrees with AMD that these terms do not require construction. *See Phillips*, 415 F.3d at 1314 ("In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.").

Accordingly, these terms shall be given their ordinary meaning.

D. "Sense amplifiers . . . are enabled"; "sense amplifiers . . . are disabled"; "a control circuit for selectively enabling said sense amplifier circuits"; "the control circuit enables said sense amplifier circuit" (claims 3, 8, 23)

This dispute concerns the operation of sense amplifiers in the '990 patent. Sense amplifiers take data output from the memory and "amplify" it. As amplification takes power, the '990 patent teaches selectively disabling the sense amplifiers, thereby saving power. 2:38-44. Claims 3, 8 and 23 refer to enabling and/or disabling sense amplifiers. The parties dispute whether the '990 patent teaches that sense amplifiers are enabled only when they are transferring data. In AMD's proposed construction, sense amplifiers are enabled any time they are selected: "Sense amplifiers are enabled when they are selected to develop a signal on their outputs, and are disabled when they are not selected to develop a signal on their outputs." In Samsung's proposed construction, sense amplifiers are enabled only when they are transferring data: "Developing a signal on the output of a sense amplifier only when it is transferring data from its output to the memory output, and not developing a signal on the output of a sense amplifier when data is being transferred from a memory location to the sense amplifier."

The Court finds that AMD's construction has more support in the intrinsic evidence. The specification provides that in some embodiments, sense amplifiers are enabled even when they are not transferring data. For example, the specification states, "In some embodiments, each sense amplifier is enabled only while its output is transferred to the memory output. *In other embodiments, several sense amplifiers whose outputs are to be transferred immediately after the output of the current sense amplifier[] are also enabled*." 2:38-43 (emphasis added). *See also* 5:49-54 ("In some embodiments, control-multiplexer circuit 334 enables, in addition to the sense amplifier being read, a certain number of sense amplifier circuits to be read immediately after, so as to allow those sense amplifier circuits sufficient time to develop their output signals."). In these embodiments, sense amplifiers are "enabled" even when they are not transferring data.

Samsung cites four documents from the prosecution history in support of its contention that (1) during AMD's prosecution of the patent, AMD adopted Samsung's construction of this term and (2) the '990 patent was allowed only because AMD narrowed its scope. In its September 23, 1994 Amendment after Final Office Action, AMD distinguished the '990 patent from the prior by stating that "when the contents of L1 are being transferred from one or more sense amplifiers to the memory output . . . the

sense amplifiers from which the contents of L1 are being transferred are enabled." *See* Decl. of Christine Haskett in Supp. of Samsung Opp. Br., ex. 13 at 3. AMD made similar statements in its April 27, 1995 Amendment and September 27, 1995 appellate brief. *See* Fahrenkrog Decl., ex. H at 5 & ex. I at 3. These statements indicate that AMD argued that the power saving feature of the '990 patent distinguished it from the prior art. They do not reveal, as Samsung claims, that AMD argued to the PTO that sense amplifiers are enabled *only* when they are transferring data. The PTO's Notice of Allowability after AMD's appeal states that the prior art does not teach the claimed invention because "Claims 7 and 16 include the feature of selectively enabling and disabling sense amplifier circuits which is taught by neither Pinkam, Rao or Young et al." Haskett Decl., ex. 14 at "Examiner's statement of Reasons for Allowance." Contrary to Samsung's view, the statement of reasons does not demonstrate that the patent was allowed only because AMD narrowed the definition of when sense amplifiers are enabled.

Accordingly, the Court adopts AMD's construction of this term.

2. Disputed term in AMD's '893 patent: "Channel-free region," "channel free zone" (claims 1, 2, 4)

This patent describes a Metal Oxide Semiconductor Field Effect Transistor ("MOSFET"). The disputed term, "channel-free region" (or "channel-free zone"[7]), appears in claims 1, 2 and 4.

> 1. An insulated gate field effect device comprising:
> a first conductivity type semiconductor substrate having a main surface;
> said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main surface;
> an insulating film formed on said concave surface;
> a conductive gate electrode formed above said insulating film, overlying the concave surface;
> first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surfaces, self-aligned to and positioned at one side and the other side of said gate electrode respectively; and
> a first conductivity type region located in said semiconductor substrate between first and second impurity regions for defining a channel region and a *channel-free region* extending conformably under and along said concave surface;
> wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and
> wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first

[7] The parties agree that "channel-free region" and "channel-free zone" have the same meaning.

depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet.

. . .

2. An insulated gate field effect device according to claim 1, wherein one of said first and second impurity regions constitutes a drain region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the *channel-free region* and the drain region and the conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity of the *channel-free region.*

. . .

4. An insulated-gate field effect transistor comprising:

a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;

an insulating layer conformably disposed on the main surface and the concave surface portion;

a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;

implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and

a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;

wherein a *channel-free zone* develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and

wherein the gate and concave surface portion are curved at least in the vicinity of the *channel-free zone* such that a smoothly curved depletion zone boundary will develop in the vicinity of the *channel-free zone* when the transistor is in the turned-off state.

A MOSFET is a type of transistor. Transistors regulate the amount of current in a circuit. Figure 9 of the'893 patent illustrates a MOSFET. The basic features are the source (labeled "4" in Fig. 9), where current enters the transistor; the drain (5), where the current leaves the transistor; and the gate (21), which starts and stops the flow of current. When the transistor is turned on, current flows from the source to the drain through a channel (13). When the voltage is sufficiently high, the channel retracts, creating a "pinch-off" region at the drain. Figure 9 illustrates the retraction at Lg1 and labels this area "channel-free length."

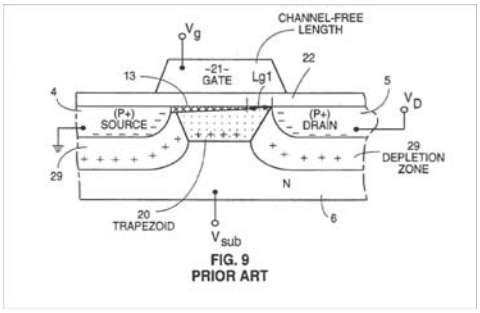


FIG. 9
PRIOR ART

Figure 4 illustrates the '893 patent. The claimed invention of the '893 patent was to improve the design of the MOSFET by introducing a curved structure. The curved surface made the channel longer than the conventional MOSFET without making the transistor larger. As Figure 4 illustrates, the "pinch-off" region (Lg2) is longer than in a conventional MOSFET. *See* 4:3-8 ("By comparing Fig. 4 to Fig. 9, it can be seen that . . . the distance Lg2 between the end of channel region 12 and the drain 5 is longer than the distance Lg1 indicated in Fig. 9.").

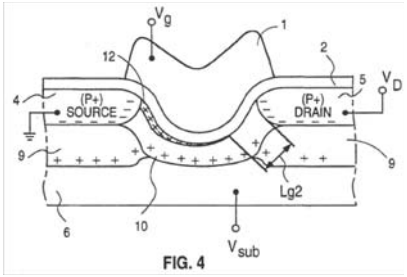


FIG. 4

The parties dispute the meaning of "channel-free region." They agree that the channel-free region encompasses the pinch-off region, but disagree as to whether it can also include the rest of the area between the source and the drain. AMD's proposed construction is: "The terms 'channel-free region' and 'channel free zone' refer to areas where there is no channel." In other words, AMD argues that when the transistor is turned off, a channel-free region exists between the source and drain. Samsung proposes the following construction: "Area without a channel and through which current flows between the channel and the drain." According to Samsung, the channel-free region describes only the pinch-off region. In Samsung's view, when the transistor is turned off, there is no "channel-free zone" between the source and drain.

Samsung's proposed construction contradicts the claim language. Claim 4 teaches that "a channel-free zone develops in the substrate, under the gate and between the source and drain regions, *when the transistor is in a turned-off state*[.]" 4:18-21 (emphasis added). Samsung's construction would render this language in claim 4 meaningless because, according to Samsung, the channel-free region does not exist when the transistor is turned off.

Samsung cites documents from the prosecution history showing that during the prosecution of the '893 patent, AMD referred to the areas Lg2 and Lg1 as "channel-free zones." *See, e.g.*, Haskett Decl., exs. 17 (July 7, 1992 Amendment at 3, 4), 19 (Nov. 10, 1992 Response to Office Action at 3). These documents are not instructive: it is undisputed that "channel-free zone" includes the pinch-off regions Lg1 and Lg2. The prosecution history cited by Samsung does not demonstrate that while prosecuting this patent, AMD limited the scope of this term to encompass only regions Lg1 and Lg2.

Samsung also objects that AMD's construction will be confusing to jurors because it suggests that a "channel-free region" exists anywhere a channel is absent. The Court disagrees. Read in the context of claims 1, 2, and 4 it is clear that the channel-free region exists in the substrate between the source and drain, and not elsewhere in the transistor.

Accordingly, the Court adopts AMD's construction.

3. Claims in AMD's '830 patent containing disputed terms

AMD asserts only claims 5 and 6 of the '830 patent. The disputed terms occur in independent Claim 1 and dependent claims 5 and 6:

> 1. In an improved integrated circuit structure comprising a semiconductor substrate having a plurality of active devices formed therein with a *Vcc current bus* and a Vss bus connected to said active devices thereon, the improvement comprising:
> (a) capacitance means formed beneath at least one of said busses comprising one or more MGS capacitors having a *gate electrode* forming a first plate of said capacitance means and *electrically connected* to one of said busses by at least one conductive path between said first plate and said one of said busses;
> (b) a doped region formed in said substrate beneath said *gate electrode* comprising the opposite plate of said capacitance means and separated from said *gate electrode* by gate oxide means formed on said substrate; and
> (c) electrode means comprising a source/drain in said substrate contiguous with said doped region and electrically connecting said doped region of said MOS capacitor to the other of said busses;
> whereby inductance voltages induced in said busses during switching will be compensated for by said capacitance means *electrically connected directly between said busses* and distributed along said busses to thereby reduce the voltage spikes produced by said induced voltages.
> . . .
> 5. The integrated circuit structure of claim 1 wherein said *gate electrode* under said bus *is divided into a plurality of segments* and each of said segments is *independently connected electrically* at a spaced apart point to one of said busses to thereby form a plurality of parallel capacitors distributed along said busses.
> 6. The integrated circuit structure of claim 5 wherein insulating means are provided to isolate each of said adjacent gate electrode segments in said structure from one another.

A. "Gate electrode . . . is divided into a plurality of segments" (claim 5)

The '830 patent teaches improvements to a decoupling capacitor. A decoupling capacitor reduces voltage spikes in electronic circuits. A voltage spike occurs when there are changes in the amount of current running through the power lines (called "busses") of electronic systems. Capacitors act as reservoirs to moderate voltage spikes. Capacitors consist of three elements: a top plate, a middle insulating layer, and a bottom plate.

Claim 1 teaches a capacitor in which the top plate is a "gate electrode," the middle insulating layer is "gate oxide," and the bottom plate is a "doped region of the substrate." The purported innovation of claim 5 is that separating the gate electrode into different segments isolates defects caused by voltage spikes so that the capacitor can continue to operate even when an individual segment is burnt out. 5:33-43.

While claim 5 indisputably discloses a segmented upper plate, the parties do not agree about whether it also teaches that the bottom plate is *not* segmented. They dispute whether the language "gate electrode . . . is divided into a plurality of segments" in claim 5 discloses a limitation in which the segments in the upper plate share a common, unsegmented doped region (bottom plate). According to AMD, the doped region cannot be segmented, while Samsung contends claim 5 discloses no such limitation on the bottom plate. AMD's proposed construction is: "For each doped region (lower plate), the gate electrode (upper plate) is divided into a plurality of segments." Samsung suggests the following construction: "In the improved integrated circuit structure of claim 1, the gate electrode is divided into two or more separate gate electrode segments."

The Court agrees with Samsung that claim 5 does not disclose a limitation requiring a common bottom plate. Although claim 5 refers only to the gate electrode, i.e. top plate, AMD argues that language elsewhere in the patent shows that claim 5 also imposes a limitation on the bottom plate. First, AMD cites Figure 16, which illustrates a preferred embodiment. AMD is correct that in Figure 16, the gate electrodes (18) share a common doped region (20). *See also* 5:11-17. AMD cites no intrinsic evidence, however, demonstrating that claim 5 should be limited to a preferred embodiment. *Phillips*, 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.").

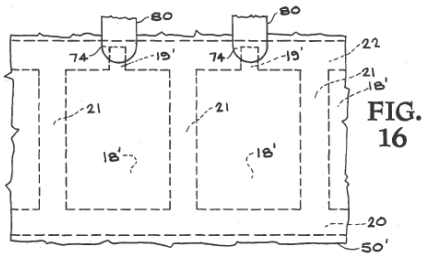


FIG. 16

Second, AMD points to dependent claim 2. This claim discloses several of the capacitors in claim 1: "The improved integrated circuit structure of claim 1 wherein said capacitance means comprise more than one of said MOS capacitors." 6:42-44. In other words, according to AMD, claim 2 discloses segmented gate electrodes and segmented doped regions. If claim 5 were intended to also disclose

segmented upper and bottom plates, AMD argues, it would have used the same language as claim 2. The Court disagrees. Claim 5 allows the possibility that the bottom plate is segmented, but also discloses an embodiment (as in Figure 16) in which the bottom plate is not segmented. As claim 5 incorporates both scenarios, there was no reason for patentee to use the same language as was used in claim 2.

Third, AMD notes that the "gate electrode" in dependent claim 5 refers to the gate electrode in claim 1. Because the gate electrode in claim 1 has "a" doped region, i.e. an unsegmented bottom plate, AMD argues that the gate electrode in claim 5 should also have a single doped region. AMD's reading of the claims is not convincing. Claim 1 discloses "one or more" capacitors. 6:21. An embodiment consisting of a single capacitor would necessarily have only one doped region. Claim 5, in contrast, discloses a structure that has multiple gate segments, which may or may not share a bottom plate. The "a" from claim 1 should therefore not be imported to claim 5. Contrary to AMD's contention, none of patent language cited by AMD imposes a limitation on the bottom plate.[8]

Accordingly, the Court adopts Samsung's construction.

B. "Vcc current bus" (claim 1, asserted claim 5)

The parties agree that the Vcc bus is the main power supply for an integrated circuit and that in the '830 patent, the Vcc bus is internal to the integrated circuit. They also agree that the Vcc bus supplies current[9] to the circuit. The only dispute is whether the construction of this term should specify that the Vcc bus supplies current to the transistors and capacitors. AMD's proposed construction is: "An internal bus (main conduit) for an integrated circuit that supplies charge *for the transistors and capacitors*" (emphasis added). Samsung proposes construing Vcc current bus as "The main power supply bus on an integrated circuit for receiving external current and providing that current to the

[8] The Court recognizes that AMD takes its construction from a summary judgment order by Judge Breyer in prior litigation over the '830 patent. *See Oki America, Inc. v. Advanced Micro Devices, Inc.*, 2006 WL 3290577, at *8 (N.D. Cal. Nov. 13, 2006). The issue in *Oki*, however, was whether claims 5 and 6 recited obvious limitations on claim 1; it appears that the structure of the bottom plate was not disputed.

[9] AMD proposes the word "charge," but agrees that current is "merely charge over time." Supp. Friedman Decl. ¶ 9.

integrated circuit." Although AMD's construction specifies that the Vcc bus supplies current to transistors and capacitors, AMD does not dispute that the Vcc bus is the current supply for the entire integrated circuit. The Court finds that AMD's construction could give the incorrect impression that the Vcc bus supplies current for the transistors and capacitors only. For this reason, Samsung's construction will be clearer to a jury.

AMD objects that Samsung's reference to "external" current could give jurors the incorrect impression that the Vcc bus is not part of the integrated circuit. The Court agrees that the word external could be confusing. Accordingly, the Court adopts a modified version of Samsung's construction: "The main power supply bus on an integrated circuit for receiving external current and providing that current to the integrated circuit. The Vcc bus is internal to the integrated circuit."

C. "Electrically connected directly between said busses" (claim 1, asserted claim 5)

Claim 1 teaches that the capacitor is "electrically connected directly" between the busses. The parties dispute whether in this "direct" electrical connection, there can be any device between the capacitor and the bus. According to AMD, a "direct" connection does not preclude "passive" devices, such as resistors. AMD proposes the following definition: "The bus and the capacitor are connected without any intervening active devices, such as transistors." Samsung construes the phrase as follows: "Connected through a direct and physical electrical connection, which includes no intermediate devices, to the Vcc current bus and the Vss bus." In other words, Samsung contends that in a "direct" electrical connection, there are no intermediate devices – active or passive.

The intrinsic evidence does not clarify whether a "direct" connection exists when a passive device such as a resistor is located between the capacitor and bus. The specification summarizes the invention as "an improved integrated circuit structure [that] comprises a Vcc bus and Vss bus having capacitance means coupled between the busses and distributed along the length of the busses." 2:23-26. Similarly, Figures 3A and 3B illustrate the invention with no device between the bus and the capacitor.

The prosecution history cited by AMD also fails to resolve this issue. AMD cites statements the patent applicants made to the PTO after the initial rejection of their application. The applicants attempted to distinguish the '830 patent from prior art by stating that the prior art references "disclose

coupling one plate of a capacitor to the source or drain of the switching device [i.e. transistor] in a memory cell while the other plate is connected to the Vcc line." Fahrenkrog Decl., ex. L (Jan. 8, 1986 Amendment) at 8-9. In other words, the applicants claimed that the prior art was distinguishable because the prior art disclosed a capacitor connected to a transistor. The applicants emphasized this point when they wrote:

> While the capacitors of the memory cells of the [prior art] references each have an upper plate connected to the Vcc (power) bus, the lower plate of their memory capacitors . . . is connected directly to the . . . transistor . . . , not to the Vss (ground) bus. While the Office Action generically refers to [the prior art] . . . as connecting [the] . . . capacitor to another bus . . . , the "connection" is only an indirect capacitive coupling through a dielectric to a signal bus . . . not to the Vss (ground) bus. Applicants' capacitance, on the other hand, is connected directly between the power busses, not to the signal busses.

Id. at 9-10 (emphasis original). In this statement, the applicants pointed out that when a capacitor connects to a bus through a transistor, there is an *indirect* connection between the capacitor and the transistor. These statements merely demonstrate that during prosecution of this patent, the applicants considered a connection indirect when it is interrupted by a transistor. This prosecution history is not instructive because the parties agree that the presence of a transistor renders a connection indirect. There is no evidence that the patent applicants intended their "direct" connection to encompass a connection that has a resistor between the capacitor and the bus.

As the intrinsic evidence is inconclusive, the Court turns to the extrinsic evidence. AMD's expert, Eby G. Friedman, opines that one skilled in the art would interpret a connection to be "direct" so long as "there is no 'active device' (which, in the context of an integrated circuit, means a transistor, which often acts as a switch) between the two end points of the line." Friedman Decl. ¶ 24. Samsung's expert, Marwan Hassoun, contends that one skilled in the art would understand a "direct" connection "to be a point-to-point electrical connection. If a passive device, such as a resistor, intervenes between two points, the connection is no longer point-to-point, and therefore not direct." Hassoun Decl. ¶ 32. These competing opinions about the meaning of "directly" in the context of an electrical connection do not help resolve the dispute. However, AMD's expert also points out that "[e]very conductor that connects two points electrically necessarily has some resistance and could be thought of as a resistor." Supp. Friedman Decl. ¶ 7. Samsung's definition would therefore mean that no connection could ever be direct and would render the insertion of the word "directly" in claim 1 meaningless. The Court finds

this testimony convincing and agrees that the presence of a passive device does not render a connection indirect.

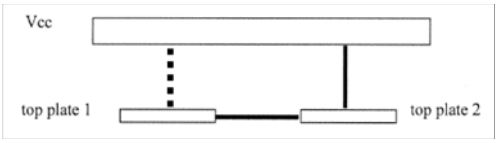
Accordingly, the Court adopts AMD's construction.

D. "Independently connected electrically" (claim 5)

Claim 5 teaches that each gate electrode segment is "independently connected electrically" to the bus. The parties dispute whether this language discloses that the gate electrode segments cannot connect to each other. AMD proposes the following construction of the phrase "independently connected electrically": "A gate segment is 'independently connected electrically' if it has its own connection or can connect without having to go through another gate segment." According to AMD, claim 5 imposes no limitation on whether the gate electrode segments can connect to each other, in addition to being connected to the bus. Samsung's proffered construction is: "Each gate electrode segment is connected through a separate electrical path that is not shared by any other gate electrode segment." Under Samsung's construction, each gate electrode segment must connect to the Vcc bus through a connection that is not shared with any other gate electrode segment.

The Court agrees with Samsung that the phrase "independently connected electrically" in claim 5 means that the gate electrode connects to the Vcc bus and not with any other gate electrode. AMD's construction is inconsistent with the innovation disclosed in claim 5. The specification explains that in a preferred embodiment of claim 5, the independent gate electrodes have "separate" connections with the bus so that the gate electrodes are "insulate[d]" from one another." 5:11-25. One advantage of this structure is that if a defect (i.e. a short) occurs between the bus and a single gate electrode, the defect is isolated. 5:33-43. The defect causes of the loss of an individual gate segment, but insulation prevents the short from spreading to the rest of the capacitor. *Id.*

Samsung points out that AMD's construction permits the connections illustrated in the following diagram, where the dashed line is a direct connection between the gate electrode and the bus, and the solid line represents a second connection, through another gate electrode. Samsung Opp. Br. at 29. Samsung explains that electrical current follows all paths simultaneously. Hassoun



Decl. ¶ 41. If, as AMD proposes, a gate electrode can have two connections to the bus (i.e. one that is direct and one that is through a second gate electrode), current will flow through both connections at once. In the foregoing diagram, current will necessarily flow through the direct connection (the dashed line) and the second gate electrode (the solid line). As a result, the first gate electrode will not be insulated and will not have an "independent" connection to the bus. If the direct connection shorts, the defect will not be isolated. AMD's construction is not viable because it allows for a construction that precludes the preferred embodiment of claim 5.

AMD objects that the phrase "connected through *a* separate electrical path" (emphasis added) in Samsung's construction incorrectly permits only a single electrical path between the gate electrode and the bus. AMD points out that nothing in claim 5 precludes multiple connections between the bus and gate. (Applying this embodiment to the foregoing diagram, AMD argues that there could be several dashed lines between the Vcc bus and the gate, where there is now only one dashed line.) The Court agrees that nothing the claim language or specification imposes a limitation of a single direct connection.

Accordingly, the Court adopts Samsung's construction, modified as follows: "Each gate electrode segment is connected through a separate electrical path, or paths, that are not shared by any other gate electrode segment."

4. Claims in AMD's '434 patent containing disputed terms

1. A multiplier for use in a data processing system having an *arithmetic and logic unit* (ALU), said multiplier comprising:
a first input terminal for receiving a first data value;
a second input terminal for receiving a second data value;
a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;
a first *bus coupling said carry save stage to said ALU*, wherein said first bus provides said carry signal to said ALU;
a second *bus coupling said carry save stage to said ALU*, wherein said second bus provides said sum signal to said ALU;
a first multiplexer coupled between said first bus and said ALU; and
a second multiplexer coupled between said second bus and said ALU, whereby said ALU is capable of adding said carry and sum signals to create a third data value equal to the product of said first and second data values.
2. The multiplier of claim 1, further comprising:

a third bus coupled between said first terminal and said first multiplexer; and

a fourth bus coupled between said second terminal and said second multiplexer.

3. The multiplier of claim 2, further comprising:

a first register coupled between said first multiplexer and said ALU, wherein said carry signal is stored in said first register; and

a second register coupled between said second multiplexer and said ALU, wherein said sum signal is stored in said second register.

4. The multiplier of claim 2, further comprising multiplexer select means coupled to said first and second multiplexers, said multiplexer select means having a first state and a second state,

wherein said multiplexer select means causes said first multiplexer to route said carry signal to said ALU and causes said second multiplexer to route said sum signal to said ALU when said multiplexer select means is in said first state, and

wherein said multiplexer select means causes said first multiplexer to route said first data value to said ALU and causes said second multiplexer to route said second data value to said ALU when said multiplexer select means is in said second state.

8. A multiplier for use in a system having an *arithmetic and logic unit* (ALU), said multiplier comprising:

a first input terminal for receiving a first data value;

a second input terminal for receiving a second data value;

a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;

means for coupling said carry save stage and said first and second input terminals to said ALU, wherein said carry and sum signals and said first and second data values are transmitted to said ALU, whereby said ALU is capable of adding said carry and sum signals to provide a third data value equal to the product of said first and second data values; and

means for controlling said means for coupling, said means for controlling having a first and a second state, wherein in said first state said means for controlling causes said means for coupling to route said carry and sum signals to said ALU and to prevent said means for coupling from routing said first and second data values to said ALU, and wherein in said second state said means for controlling causes said means for coupling to route said first and second data values to said ALU and to prevent said means for coupling from routing said carry and sum signals to said ALU.

11. A system comprising:

a carry save stage coupled to receive a first data value and a second data value, wherein the carry save stage generates a carry signal and a sum signal in response to the first and second data values;

a first selector circuit coupled to receive the carry signal and the first data value;

a second selector circuit coupled to receive the sum signal and the second data value;

a control signal source coupled to the first and second selector circuits, wherein the control signal source causes the first and second selector circuits to operate in a first mode and a second mode, wherein in the first mode, the first selector circuit passes the carry signal and the second selector circuit passes the sum signal, and wherein in the second mode, the first selector circuit passes the first data value and the second selector circuit passes the second data value; and

an *arithmetic and logic unit* (ALU) coupled to the first and second selector circuits, wherein the ALU receives the signals passed by the first and second selector circuits, and wherein in the first mode, the ALU adds the carry and sum signals to create a third data value equal to the product of the first and second data values.

A. Arithmetic and logic unit (claims 1-4, 8, 11)

The '434 patent relates to the field of data processing. It discloses a structure and method for using an arithmetic and logic unit ("ALU") in a multiplier circuit. 1:9-13. Both multiplier circuits and ALUs were prior art to the '434 patent. They are both circuits that perform operations on data retrieved from memory. 1:15-37. The claimed invention improves the multiplier circuit by making it smaller and more efficient. 2:5-10.

The parties agree that an ALU is a circuit that processes data from memory by performing both arithmetic operations (such as addition and subtraction) and logic operations (such as OR and AND) on the data. They also agree that an ALU can, but need not, include registers.[10] *Compare* 1:19-21 (specification states that prior art ALU "includes registers"), *with* 4:15-21 (claim 3 states that registers are external to the ALU). The parties dispute two narrow issues: (1) whether the construction of this term should include addition as an exemplary operation and (2) whether the construction should specify that an ALU may optionally include registers. AMD proposes the following construction: "Unit that can perform both arithmetic and logic operations." Samsung's proposed construction is: "A conventional circuit which performs arithmetic and logic operations (e.g. addition) within the data processing system and optionally includes registers capable of receiving inputs from multiple sources within that data processing system."

The Court finds that Samsung's construction is more likely to confuse jurors than to help them. Samsung's use of "addition" as an example is unlikely to help jurors understand what a logic operation is. In addition, Samsung's inclusion of information about registers is likely to be confusing because Samsung does not explain what registers are. This aspect of Samsung's construction is also unnecessary as there is no dispute that registers are optional. AMD's construction is more useful because it explains to jurors that an ALU simply performs the functions that its name suggests.

Accordingly, the Court adopts AMD's construction of this term.

[10] Registers temporarily save data. *See, e.g.*, 1:20-21.

B. Bus coupling said carry save stage to said ALU (claims 1-4)

The parties agree that the "bus" coupling the carry save stage to the ALU in claims 1-4 is a connection that transfers information between the "carry save" stage of data processing and the ALU. At issue in the construction of the phrase "bus coupling said carry save stage to said ALU" is whether the bus doing the coupling can modify the data that it transfers. AMD's proposed construction is: "Bus that can transfer information between the carry save stage and the ALU." Samsung offers the following construction: "A physical path between the carry save stage and ALU that does not modify the value from the carry save stage."

Samsung fails to cite intrinsic evidence in support of its claim that the bus disclosed in the '434 patent can never modify the values it transfers. Instead, Samsung relies on a 1994 dictionary, which defined a bus as an "electrical pathway along which signals are sent from one part of the computer to another." Haskett Decl., ex. 28 at 70. According to Samsung, use of the word "sent" demonstrates that data is merely transferred, and not modified, by a bus. AMD responds with an expert declaration stating that in 1994, it was understood that a bus could modify the values it transferred by shifting the order or position of bits. Wolfe Supp. Decl. ¶ 4. In light of this conflicting evidence about whether one of ordinary skill in the art understood in 1994 that a bus could modify the values it transfers, the dictionary definition cited by Samsung is not dispositive. The Court rejects Samsung's construction as it adds a negative limitation that is not present in the claim language. *See Omega Eng'g, Inc., v. Raytek Corp.*, 334 F.3d 1314, 1322 (Fed. Cir. 2003) (rejecting additional negative limitation that had "no anchor in the explicit claim language.").

Accordingly, the Court adopts AMD's construction.

5. Disputed term in AMD's '200 patent: Data pattern (claims 1-3, 5-8, 11-13, 15-17, 19)

> 1. A configuration register for controlling a logic testing circuit, said logic testing circuit being coupled to a logic module for testing the integrity of said logic module, said logic testing circuit having a normal state and a low power state, said configuration register comprising:
> a key input disposed to receive a key signal;
> a reset input disposed to receive a reset signal;
> an output coupled to said logic testing circuit;
> a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a

control signal responsive to said key signal and said reset signal;

wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and

wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined *data pattern*.

2. The configuration register of claim 1 wherein said control signal is a clock signal when said key signal matches said predetermined pattern, and wherein said output is coupled to a clock port of said logic testing circuit.

3. The configuration register of claim 2 further comprising a clock input coupled to a clock signal source, said clock signal being generated responsive to a signal generated by said clock signal source.

5. The configuration register of claim 3 further comprising a NOR gate, wherein said key logic circuit and said clock input are coupled to said output through said NOR gate.

6. A circuit arrangement comprising:

a logic component having a logic module and a built-in logic testing circuit, said logic testing circuit being coupled to said logic module for testing the integrity of said logic module and having a normal state and a low power state, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;

a configuration register for controlling said logic testing circuit, said configuration register comprising

a key input disposed to receive a key signal,

a reset input disposed to receive a reset signal,

an output coupled to said logic testing circuit, and

a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;

wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and

wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined *data pattern*.

7. The arrangement of claim 6 wherein said control signal is a clock signal when said key signal matches said predetermined *data pattern*, and wherein said output is coupled to a clock port of said logic testing circuit.

8. The arrangement of claim 7 further comprising a clock signal source, wherein said configuration register further comprises a clock input disposed to receive said clock signal from said clock signal source.

11. The arrangement of claim 6 wherein said logic testing circuit has a clock port and wherein the state of said logic testing circuit is responsive to a signal at said clock port.

12. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said low power state when a LOW is applied to a clock port, and wherein said control signal is LOW when said reset input is triggered by said reset signal.

13. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said normal state when a clock signal is applied to a clock port, and wherein said control signal is a clock signal when said key signal matches said predetermined *data pattern*.

15. A circuit arrangement comprising:

a logic component having a logic module and a built-in logic testing circuit for testing the integrity of said logic module, said logic testing circuit being coupled to said logic module and having a normal state and a low power state, said logic testing circuit further having a clock port, wherein the state of said logic testing circuit is responsive to a control signal applied at said clock port, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;

a configuration register for controlling said logic testing circuit, said

configuration register comprising
a key input disposed to receive a key signal,
a reset input disposed to receive a reset signal,
a clock input disposed to receive a clock signal,
a signal output coupled to the clock port of said logic testing circuit,
a key logic circuit coupled to said key input and said reset input, wherein said key logic circuit generates a mode signal responsive to said key signal and said reset signal,
wherein said mode signal is a disable signal when said reset input is triggered by said reset signal, and wherein said mode signal is an enable signal when said key signal matches a predetermined *data pattern*, and
a logic gate having inputs coupled to said clock input and said key logic circuit and an output coupled to said signal output, said logic gate generating at said signal output said control signal responsive to said clock signal and said mode signal; and
wherein said control signal drives said logic testing circuit to a low power state when said mode signal is said disable signal, and wherein said control signal drives said logic testing circuit to said normal state when said mode signal is said enable signal.

17. The arrangement of claim 15 further comprising a clock signal source coupled to said clock input, said clock signal source generating said clock signal.

19. The arrangement of claim 15 wherein said key input is a multi-bit digital input and wherein said predetermined *data pattern* is determined by the configuration of the components of said key logic circuit.

AMD's '200 patent is entitled "Power Saving Feature for Components Having Built-In Testing Logic." The '200 patent relates to the field of "built-in testing logic" on electronic devices. 1:6-8. Built-in self testing ("BIST") logic provides a way to test whether the components of computer systems are working properly. 1:13-20. A problem with the prior art was that BIST consumed power whether or not it was being used to run a test. 1:37:45. As a result, BIST-equipped components were less efficient. *Id.*

The claimed invention of the '200 patent is a "configuration register" that controls a component's BIST. 1:55-57. The configuration register includes a "key logic." 1:61-63. The key logic generates a signal that puts the BIST in a low power state when it is not being used. The key logic also generates a signal that puts the BIST in a "normal" state "when the key signal matches a predetermined data pattern." 1:66-2:2. The parties dispute the meaning of "data pattern."

Both parties agree that the data pattern functions like a key and turns on a component's internal testing system. They also agree that a data pattern consists of a pattern of bits, which represent information. The dispute concerns whether (1) it is accurate to characterize the pattern as a "sequence" and (2) whether "data" can include addresses and instructions. AMD contends that data pattern should be construed as "bit sequence." Samsung's proposal is: "A pattern of bits representing information and

not representing an address or an instruction."

The Court agrees with Samsung on the first disputed point. The ordinary meaning of "sequence" is "the following of one thing after another." The use of this word could suggest to the jury that the information in a data pattern arrives successively, rather than all at once. AMD does not contest that this interpretation would be incorrect because it would exclude the preferred embodiment. *See* 3:40-44. It is undisputed that in the context of the '200 patent, a data pattern consists of an ordered, predetermined set of data. The word "pattern" captures this ordered relationship and needs no construction.

On the second point, the Court agrees with AMD. Samsung points to no intrinsic evidence in support of the negative limitation it seeks to impose on the word "data." Instead, Samsung cites three dictionary definitions that purportedly establish that in the computer arts, the word data excludes addresses and instructions. *See* Haskett Decl., exs. 20-22. This extrinsic evidence does not persuade the Court that the word "data" is includes this negative limitation. One of the dictionaries cited by Samsung defines data as: "a general term for information; also used to distinguish input and output information from instructions." *See id.*, ex. 22 at 35. As AMD points out, this definition supports AMD's view that "data" can have a general meaning. The claims and specification place no limitations on the word data, and the Court declines to do so.

Accordingly, the Court construes "data pattern" as "a pattern of bits representing information."

6. Disputed term in Samsung's '750 patent: Separate instruction sets (claims 1, 14)

> 1. A central processing unit (CPU) for processing instructions from two *separate instruction sets*, said CPU comprising:
>
> first instruction decode means for decoding instructions from a first instruction set, said first instruction set having a first encoding of instructions;
>
> second instruction decode means for decoding only a subset of instructions from a second instruction set, said second instruction set having a second encoding of instructions, said first encoding of instructions independent from said second encoding of instructions;
>
> select means, coupled to said first instruction decode means and said second instruction decode means, for selecting said decoded instruction from either said first instruction decode means or from said second instruction decode means; and
>
> execute means for executing decoded instructions selected by said select means, whereby instructions from both said first instruction set and said second instruction set are executed by said CPU.
>
> . . .

14. A method for processing instructions from two *separate instruction sets* on a central processing unit (CPU)

The '750 patent, entitled "Dual-Instruction-Set Architecture CPU with Hidden Software Emulation Mode," relates to the field of computer microprocessors that can execute "multiple instruction sets." 1:21-24. Personal computers are operated by central processing units ("CPUs") that execute computer programs. "Instruction sets" are lists of instructions that the CPU is able to execute. Two types of CPUs are CISC (complex instruction set computer) and RISC (reduced instruction set computer). CPUs that execute multiple instruction sets are able to execute instructions written for the current CPU as well as for older CPUs. CPUs accomplish this task by translating older software programs so that they can be executed by a newer computer. This process is called decoding. The task can also be accomplished through hardware translation, which is faster but more expensive. The '750 patent combines hardware and software methods of translation.

The parties dispute the meaning of "separate instruction sets" in the preambles of claims 1 and 14. Samsung argues that this term need not be construed because it is in the preamble and does not impose a limitation on the claims. In the alternative, Samsung proposes "distinct groups of instructions" as a construction. AMD's proposed construction is: "One complex instruction set computer (CISC) x86 instruction set architecture and one reduced instruction set computer (RISC) PowerPC instruction set architecture. These instruction sets have independent encodings of instructions. Mere extensions of instruction sets do not constitute separate instruction sets because they have dependent encodings of instructions."

The Court agrees with Samsung that the term "separate instruction sets" in the preambles of claims 1 and 14 is non-limiting and therefore should not be construed. "[C]lear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation because such reliance indicates use of the preamble to define, in part, the claimed invention." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). "Without such reliance, however, a preamble generally is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention." *Id.* at 809; *see also Bristol-Myers Squibb Co. v. Ben Venue Labs.*,

Inc., 246 F.3d 1368, 1375 (Fed. Cir. 2001) (preamble language "for reducing hematologic toxicity" non-limiting where steps of the claimed method were "performed in the same way regardless whether or not the patient experiences a reduction in hematologic toxicity").

Here, the phrase "separate instruction sets" is not limiting because it does not add information about the structurally complete invention disclosed in the claim body. Claims 1 and 14 expressly disclose two different sets of encoding instructions ("first instruction set" and "second instruction set"). The deletion of the phrase "separate instruction sets" from the preambles of these claims would therefore have no effect on the claims themselves. AMD points to several references from the prosecution history in which the patent applicants used the term "separate instruction sets" to distinguish their invention from prior art. In each of these cases, however, the applicants used this phrase to describe limitations already disclosed in the claim bodies, not to impose an additional limitation on the invention. For example, the patent applicants argued that a prior art reference was "clearly directed to an extension of a single instruction set rather than a separate second instruction set." *See* Decl. of Anthony G. Beasley in Supp. of AMD Opp. Br. ("Beasley Decl.") , ex. H at 6 (emphasis original). They contrasted their own invention as follows: "Applicant's claim 1 recites 'two separate instruction sets' . . . . Claim 1 clearly disallows a mere extension of a single instruction set by stating: 'said first encoding of instructions independent from said second encoding of instructions'." *Id.* at 7. As this example shows, the patent applicants referred to "separate instruction sets" to describe a limitation disclosed in the body of claim 1, not to impose an additional limitation on their invention. The mere repetition of this phrase in the prosecution history does not establish the patent applicants' "clear reliance," *Catalina Mktg.*, 289 F.3d 808, on the preamble during their prosecution of the '750 patent.

Accordingly, the Court finds that the term "separate instruction sets" is non-limiting and needs no construction.

7. Disputed term in AMD's '879 patent: Control panel (asserted claims 11-24)

> 11. A video graphics processor comprising:
> a processing unit; and
> memory that stores programming instructions that, when read by the processing unit, causes the processing unit to (a) provide a video control icon that is visible on the display, wherein the video control icon relates to live video that is being presented as a

background on a display; (b) detect selection of the video control icon; (c) provide a *control panel* while the live video remains in the background and an application that was in focus remains in focus when the video control icon has been selected, wherein the *control panel* includes at least one of the following: a volume adjust icon, a mute icon, a pause icon, a rewind icon, and a fast-forward icon.

12. The video graphics processor of claim 11 further comprises, within the memory, programming instructions that, when read by the processing unit, causes the processing unit to provide, as the *control panel*, at least one of: volume adjust icon, mute icon, channel up icon, channel down icon, numerical channel display, and alpha-numeric channel display.

13. The video graphics processor of claim 11 comprises, within the memory, programming instructions that, when read by the processing unit, causes the processing unit to remove the *control panel* when another displayed element is selected.

14. A video graphics processor comprising:

a processing unit; and

memory that stores programming instructions that, when read by the processing unit, causes the processing unit to (a) detect selection of a video control icon, wherein the video control icon relates to live video that is being presented as a background on a display; (b) provide a *control panel* while the live video remain the background and an application that was in focus remains in focus when the video control icon has been selected; and (c) adjust at least one attribute of the live video based on an input received via the *control panel*, wherein the at least one attribute included: volume, mute, pause, rewind, and fast-forward.

15. The video graphics processor of claim 14 further comprises, within the memory, programming instructions that, when read by the processing unit, causes the processing unit to adjust the at least one attribute by adjusting at least one of: volume, mute, channel up, and channel down.

16. The video graphics processor of claim 14 further comprises, within the memory, programing instructions that, when read by the processing unit, causes the processing unit to remove the *control panel* when another displayed element is selected.

17. A digital storage device that stores programming instructions that, when read by a processing unit, causes the processing unit to provide control of background video, the digital storage device comprises:

first storage means for storing programming instructions that, when read by the processing unit, causes the processing unit to provide a video control icon that is visible on the display, wherein the video control icon relates to live video that is being presented as a background on a display;

second storage means for storing programming instructions that, when read by the processing unit, causes the programming unit to detect selection of the video control icon; and

third storage means for storing programming instructions that, when read by the processing unit, causes the processing unit to provide a *control panel* while the live video remains in the background and an application that was in focus remains in focus when the video control icon has been selected.

18. The digital storage device of claim 17 further comprises means for storing programming instructions that, when read by the processing unit, causes the processing unit to provide, as the *control panel*, at least one of: volume adjust icon, mute icon, pause icon, rewind icon, and fast-forward icon.

19. The digital storage device of claim 17 further comprises means for storing programming instructions that, when read by the processing unit, causes the processing unit to provide, as the *control panel*, at least one of: volume adjust icon, mute icon, channel up icon, channel down icon, numerical channel display, and alpha-numeric channel display.

20. The digital storage device of claim 17 further comprises means for storing programming instructions that, when read by the processing unit, causes the processing

unit to remove the *control panel* when another displayed element is selected.

21. A digital storage device that stores programming instructions tat, when read by a processing unit, causes the processing unit to provide control of background video, the digital storage device comprises:

first storage means for storing programming instructions that, when read by the processing unit, causes the processing unit to detect selection of a video control icon, wherein the video control icon relates to live video that is being presented as a background on a display;

second storage means for storing programming instructions that, when read by the processing unit, causes the processing unit to provide a *control panel* while the live video remains in the background and an application that was in focus remains in focus when the video control icon has been selected; and

second storage means for storing programming instructions that, when read by the processing unit, causes the processing unit to adjust at least one attribute of the live video based on an input received via the *control panel*.

22. The digital storage device of claim 21 further comprises means for storing programming instructions that, when read by the processing unit, causes the processing unit to adjust the at least one attribute by adjusting at least one of: volume, mute, pause, rewind, and fast-forward.

23. The digital storage device of claim 21 further comprises means for storing programming instructions that, when read by the processing unit, causes the processing unit to adjust the at least one attribute by adjusting at least one of: volume, mute, channel up, and channel down.

24. The digital storage device of claim 21 further comprises means for storing programming instructions that, when read by the processing unit, causes the processing unit to remove the *control panel* when another displayed element is selected.

The '879 patent is entitled "Method and Apparatus for Providing Control of Background Video." The disclosed invention allows users to control video that is playing in the background while applications in the foreground remain in focus. *See* Abstract. The parties agree that the "control panel" disclosed in asserted claims 11-24 teaches a screen that contains control functions. They dispute whether the control panel is limited to the screens of personal computers. AMD argues that the term "control panel" need not be construed. Alternatively, AMD proposes construing this term as: "Area of the screen containing control functions." Samsung's construction limits the control panel to something that appears on the screen of a personal computer: "An area of the personal computer screen containing control functions."

AMD is correct that the claim language does not expressly limit control panels to personal computer screens. The Court must read the claims in light of the specification, however. *See Phillips*, 415 F.3d at 1321 (specification is "the single best guide to the meaning of a disputed term") (quotation omitted). The specification of the '879 patent unequivocally limits this invention to computers. The abstract begins, "A method and apparatus for controlling background video on a computer display is

accomplished by providing a video control icon, which is visible on the display." The specification describes the technical field of the invention as follows: "This invention relates generally to computer displays and more particularly to providing control of background video." 1:7-9. The "background of the invention" section of the specification begins with a description of computers ("Computers are known to include a central processing unit, cache memory, hard drive memory . . .") and describes three means of displaying live video on a "computer monitor." 1:12-15; 1:23-33. The specification summarizes the problem addressed by the invention as follows:

> When an attribute of the live video [i.e. the video displayed on the computer monitor] is to be changed, other applications that were in focus (i.e., actively being displayed and/or being worked upon) must go into a background mode (i.e., taken out of focus). As such, the adjusting of attributes of the live video consume[s] the activity of the computer until such attributes have been changed and the live video is returned to the background mode. As one can readily appreciate, this can be someone burdensome to the user and is an ineffective use of the computer system.
>
> Therefore, a need exists for a method and apparatus for providing control of background video while the video remains in the background.

1:41-53. The section headed "detailed description of the drawings" begins, "Generally, the present invention provides a method and apparatus for controlling background video on a computer display." 2:2-4. Figure 1 of the patent illustrates the control panel on a screen. The specification explains that Figure 1 illustrates "a graphical representation of a computer screen." 2:19-20. The specification concludes with the following summary:

> The preceding discussion has presented a method and apparatus for controlling background video. By providing a video control icon which, when selected, pops up a control panel, live video can remain in the background while its attributes are changed via the control panel. This allows a user to simply adjust the attributes of the live background video without having to bring it in focus. As such, the overall operation[] of a computer system is improved.

3:47-54. This intrinsic evidence leaves no doubt that the inventor was working in the field of video displayed by a computer; there is no suggestion in the specification that the invention can be implemented without a computer. As the patentee consistently uses "control panel" in the specification to denote a mechanism for controlling video on a computer display, this understanding of the term is incorporated into the claim language. *See Bell Atlantic Network Servs., Inc. v. Covad Communic'ns Group*, 262 F.3d 1258, 1271 (Fed. Cir. 2001) (citation omitted) ("[W]hen a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has

defined that term by implication.")

AMD argues that invention taught in the '879 patent also encompasses user interfaces in devices such as digital cameras, camcorders, and cell phones. None of the intrinsic evidence cited by AMD supports this conclusion. First, AMD cites claim 12, which discloses the following options on the control panel: "volume adjust icon, mute icon, channel up icon, channel down icon . . . ." 4:59-60. (Claim 15 teaches control over the same attributes. 5:15-19; *see also* claims 19 & 23.) AMD points out that "channel up" and "channel down" displays make more on a television than on a computer. The specification explains, however, that the live video controlled by the control panel may be "sourced" from "a live television broadcast, satellite television, or cable television." 2:36-38. In other words, while the video is displayed on a computer screen, 2:21, the computer can be connected to a television, which is the source for the video, 2:37. The specification also provides that the source of the video could be a DVD player or VCR, 2:39-40, in which case the control panel on the computer screen would display "at least one of a volume adjust icon, a mute icon, a pause icon, a re-wind icon, and a fast forward icon," 2:40-41. Contrary to AMD's contention, the reference to channel controls in some claims does not establish that the control panel can be displayed on a television without a computer.

AMD also cites dependent claim 5, which provides: "The method of claim 1 further comprises, within step (a), providing the live video as the background on a computer display, a television, or a monitor." 5:12-14. Claim 5 does not support AMD's construction. This claim describes embodiments in which other devices (such a television) may be connected to a computer and used to display the video. Claim 5 merely lists types of devices that can display the patented application when those devices are connected to a computer.

Finally, AMD objects that the intrinsic evidence does not limit the control panel application to use on a "personal" computer. On this point, the Court agrees: the specification refers repeatedly to a computer, not a personal computer. The Court will modify Samsung's construction by omitting the word "personal." The Court also finds that Samsung's construction could confuse jurors by leading them to believe that a control panel can *only* be displayed on a computer screen. As the foregoing discussion has established, claim 5 discloses that a television could be used for a computer display. The Court will therefore replace "screen" with "display" in Samsung's proposed construction.

Accordingly, "control panel" shall be construed as follows: "An area of the computer display containing control functions."

8. Claims in Samsung's '065 patent containing disputed terms

The '065 patent, entitled "Method for Manufacturing Semiconductor Device," claims a method for improving accuracy and consistency in the manufacturing of semiconductor chips from silicon wafers. The semiconductor chip manufacturing process is sensitive to variations in the settings of machines used in the manufacturing process. 1:2-24. Prior art used "sampling" to achieve consistency in manufacturing. 1:31-55. Sampling involves selecting sample wafers from a lot and performing a manufacturing process on them. *Id.* The result is measured, variables (such as etching time and etching activation energy) are adjusted in accordance with the result, and the manufacturing process is performed on the rest of the lot. *Id.* This sampling technique has shortcomings, including the possibility that workers will err in measuring the samples and resetting equipment. 1:65-2:10. If an individual worker makes a mistake, that defect is repeated in the entire lot. *Id.* One of the claimed inventions of the '065 patent was to improve the reliability of the manufacturing process by eliminating sampling. 2:23-26. The parties dispute terms in claims 1, 3, 6, 8, 9, and 12 of the '065 patent.

> 1. A method for manufacturing a semiconductor device with manufacturing equipment performing a process having a working condition, said manufacturing equipment being adapted to manufacture said semiconductor device in units of lots, said method comprising the steps of:
>
> extracting an optimal working condition by *accumulatively averaging working conditions* of lots previously processed using said process performed by said manufacturing equipment;
>
> *extracting a correction condition by* extracting information *corresponding to an alignment state* of said process;
>
> setting a current working condition by adding said correction condition to said optimal working condition; and
>
> performing said process for an entire lot according to said current working condition.
>
> 2. A method for manufacturing a semiconductor device as claimed in claim 1, wherein said working condition includes process parameter values, and wherein said step of extracting said optimal working condition includes respectively averaging each of said process parameter values of said working conditions of said previously processed lots.
>
> 3. A method for manufacturing a semiconductor device as claimed in claim 2, further comprising a step of detecting a resultant value of performing said process according to said current working condition, and
>
> wherein said step of extracting said optimal working condition includes *accumulatively averaging working conditions* set for selected ones of said previously processed lots, each having a corresponding resultant value differing from a reference value by no more

than a standard deviation.

4. A method according to claim 1, wherein said working condition includes process parameter values and alignment parameter values and wherein said step of setting said current working condition includes adding said correction condition to said alignment parameter values of said optimal working condition.

. . .

6. A method according to claim 1, wherein said step of *extracting said correction condition* includes multiplying a correction value by a gain whose value is determined according to an amount of correlation between lots.

7. A method according to claim 1, further comprising the steps of:
detecting a resultant value of performing said process according to said current working condition; and
resetting said current working condition in accordance with said resultant value

8. A method for manufacturing a semiconductor device with manufacturing equipment performing a process having a working condition, said manufacturing equipment being adapted to manufacture said semiconductor device in units of lots, said method comprising the steps of:
extracting an optimal working condition by *accumulatively averaging working conditions* of lots previously processed using said process performed by said manufacturing equipment;
setting a current working condition based on said optimal working condition;
performing said process for an entire lot according to said current working condition;
detecting a resultant value of performing said process according to said current working condition; and
resetting said current working condition in accordance with said resultant value.

9. A method according to claim 8, further comprising a step of *extracting a correction condition* by extracting information *corresponding to an alignment state* of said process.

. . .

12. A method according to claim 8, wherein said step of extracting said optimal working condition includes *accumulatively averaging working conditions* set for selected ones of said previously processed lots for which said resultant value is within a standard deviation.

A. "Accumulatively averaging the working conditions" (claims 1, 3, 8, 12)

One of the steps in the method disclosed in claim 1 is "extracting an optimal working condition by accumulatively averaging working conditions of lots previously processed using said process performed by said manufacturing equipment[.]" The parties dispute (1) whether "working conditions" refers to anything beyond the parameters that restrict machine settings, (2) whether "working conditions" are limited to the alignment and exposure process, and (3) what it means to perform an "accumulative average." Samsung's proposed construction is: "Performing a mathematical averaging operation on a set of working conditions over time to determine a value representative of the set." AMD proposes: "For each parameter comprising a working condition, individually summing over previous values of that parameter and dividing the result by the total number of terms in the summation. In an

accumulative average, the number of terms in the average grows by one as each new value is calculated. A working condition is a group of settable parameter values that control alignment and exposure in a semiconductor manufacturing process."

The first disputed issue is the scope of "working conditions." The parties agree that in the context of this patent, "working conditions" at a minimum refers to "settable parameters" that control variables in processes used to manufacture semiconductors. Samsung argues that "working condition" also encompasses another meaning. According to Samsung, "working conditions" also refers to the variables themselves. Samsung Br. at 3. Samsung does not explain how "working conditions" can refer to both the settings and the variables the settings control. None of the intrinsic evidence Samsung relies on supports this interpretation. For instance, Samsung cites the following language from the specification: "If the working condition is incorrectly set due to measurement error or mistake by an individual worker, the defect is generated in the wafer of the whole lot manufactured by the same serial process." 1:67-2:5. This language emphasizes that a "working condition" is something that the worker sets, i.e. a machine setting, not the variable itself. Samsung does not support its contention that this term "also encompasses the variables that these machine settings affect." Samsung Reply at 6.

On the second disputed issue, the Court agrees with Samsung that "working conditions" are not limited to the alignment and exposure process. Samsung concedes that the "alignment" limitation restricts claims 1-7 and 9-10 to the photolithography process, but argues that claims 8, 11, and 12 include no such limitation. The specification explains that "for convenience sake," it will discuss only the photolithography process. 1:32. The specification also states that prior art fabrication processes are also used in etching processes. 1:46. AMD points to no intrinsic evidence limiting claims 8, 11 and 12 to the photolithography process. The Court therefore rejects the "alignment and exposure" portion of AMD's proposed construction.

Third, the parties dispute whether an "accumulative average" can include a weighted average. A weighed average gives different weight to the values that are averaged. AMD contends that an accumulative average does not include a weighted average. AMD refers to the following formula, which is provided in the preferred embodiment of the '065 patent. According to AMD, one of ordinary

$$Xm = \frac{1}{n-1} \sum_{i=1}^{n-1} (Xi \pm \varepsilon)$$

(n is a natural number of over 1)

skill in the art would interpret this formula as teaching that previous parameter values are added together and then divided by the number of processes performed. Samsung points out that AMD's interpretation does not adequately describe the formula because it omits the italicized E, which (as the Court will discuss more fully *infra*) represents a correction condition. In addition, the extrinsic evidence cited by AMD establishes that an accumulative average could encompass a weighted average. *See* Beasley Decl., ex M (Wikipedia article stating that "cumulative average" is "a type of moving average" and that a moving average could "use a weighted average"). AMD cites no intrinsic evidence demonstrating that the accumulative average in the '065 patent could not weight some values more than others. The Court therefore agrees with Samsung that AMD's construction of "accumulative average" is too narrow.

Accordingly, the Court adopts the following construction of this term: "Performing a mathematical averaging operation on a set of working conditions over time to determine a value representative of the set. A working condition is a group of settable parameter values that control variables in processes used to manufacture semiconductors."

B. Information "corresponding to an alignment state" (claims 1, 9)

One of the steps of the method disclosed in claim 1 is: "extracting a correction condition by extracting information corresponding to an alignment state of said process[.]" The parties dispute the scope of the limitation "corresponding to an alignment state." Samsung contends that information "corresponding to an alignment state" could include many different types of information, including identifying the equipment or tools that were used to process a particular layer of a semiconductor wafer. Samsung's proposed construction is, "relating to the alignment of a lower layer or a reference layer formed during the manufacturing process of a semiconductor device." AMD contends that the extracted information consists of a comparison of the alignments of wafers in two layers. AMD proposes construing this limitation as follows: "relating to the relative position of one layer on a semiconductor wafer as compared to another layer on the same wafer in a photolithography application."

The specification supports AMD's construction. In the preferred embodiment, the "alignment parameter . . . indicates the correlation between the reference layer and the layer expected to be currently

performed." 4:8-12.[11] In contrast, Samsung's broad construction of information that corresponds to an alignment state is not supported by the intrinsic evidence. Samsung argues that information "corresponding to an alignment state" could include "reflectivity of the individual wafers," Samsung Br. at 9, but offers no citation to support this construction. Samsung also contends that information "corresponding to an alignment state" could include "the identification of the particular equipment that was used to process the lower layer in the current lot." *Id.* Samsung cites the following language from the specification in support of this reading: "When the parameters are added for processing using the same equipment, it is possible to set more precise optimal parameters. Thereby, it is also possible to minimize errors generated in the alignment & exposure process." 5:54-57. The Court finds that nothing in this language indicates that "information corresponding to an alignment state" includes information that identifies the processing equipment. This portion of the specification follows an explanation of how the preferred embodiment derives parameters, i.e. data that will be used to reset manufacturing processes. The concluding paragraph at 5:54-57, which Samsung relies on, simply explains that accuracy is increased if the same equipment is used to control the manufacturing process *and* to derive the information that will be used to correct that process.

Samsung also argues that "information," as it is used in claim 1, must be broader than the term "resultant value" in claim 8. Samsung's comparison of the claim language in claim 8 is inapt. Claim 1 explicitly limits the type of "information" that is extracted: this step in the method concerns only information "corresponding to an alignment state." The reference to resultant values in claim 8 is not pertinent.

Accordingly, the Court adopts AMD's construction.

C. "Extracting a correction condition" (claims 1, 6, 9)

As noted in the foregoing section, one of the steps of the method disclosed in claim 1 is: "extracting a correction condition by extracting information corresponding to an alignment state of said process[.]" The parties dispute the scope of another limitation in this step: "extracting a correction

[11] Samsung agrees with AMD that the "alignment state" limitation refers to the photolithography process. Samsung Reply at 7.

condition."

The parties agree that "extracting a correction condition" is a step in the photolithography process that involves obtaining information that is used to correct the "optimal working condition" in order to arrive at the "current working condition." 6:11-18. Samsung's proposed construction is: "Creating a value or data set to be used to affect the determination of a current working condition." AMD proposes the following construction: "Subtracting an objective value from a resultant value so that, when this difference value is added to the optimal working condition, a process can be performed without error."

The Court finds that Samsung's construction accurately conveys the function of the "correction condition" as it is taught in the claim language. The Court rejects AMD's construction for two reasons. First, it adds terminology – "resultant value" and "difference value" – that is unlikely to be clear to a jury. Second, AMD's proposed language is taken from the section of the preferred embodiment that teaches calculating an "optimal condition." 3:31. The preferred embodiment supplies the following equation for this calculation:

$$Xm = \frac{1}{n-1} \sum_{i=1}^{n-1} (Xi \pm E)$$

(n is a natural number of over 1)

The specification teaches that in this equation, the italicized E "indicates a correction element obtained by subtracting an objective value from a resultant value." 3:43-44. AMD argues that this explanation of the equation should be used to construe "correction condition." The Court disagrees. Claim 1 makes clear that the steps of "extracting an optimal working condition" and "extracting a correction condition" are distinct. 6:7-11. AMD provides no reason for defining "correction condition" by using the preferred embodiment's description of how to calculate the "optimal condition."

Accordingly, the Court adopts Samsung's construction of this term.

CONCLUSION

For the foregoing reasons, the Court hereby adopts the constructions set forth above.

Dated: September 17, 2009

Susan Illston

SUSAN ILLSTON
United States District Judge