

1 ROBERT T. HASLAM (Bar No. 71134)
 rhaslam@cov.com
 2 MICHAEL K. PLIMACK (Bar No. 133869)
 mplimack@cov.com
 3 CHRISTINE SAUNDERS HASKETT (Bar No. 188053)
 chaskett@cov.com
 4 COVINGTON & BURLING LLP
 One Front Street
 5 San Francisco, CA 94111
 Telephone: (415) 591-6000
 6 Facsimile: (415) 591-6091

7 ALAN H. BLANKENHEIMER (Bar No. 218713)
 ablankenheimer@cov.com
 8 LAURA E. MUSCHAMP (Bar No. 228717)
 lmuschamp@cov.com
 9 JO DALE CAROTHERS (Bar No. 228703)
 jcarothers@cov.com
 10 COVINGTON & BURLING LLP
 9191 Towne Centre Drive, 6th Floor
 11 San Diego, CA 92122-1225
 Telephone: (858) 678-1800
 12 Facsimile: (858) 678-1600

13 Attorneys for Defendants and Counterclaimants SAMSUNG ELECTRONICS CO., LTD.,
 14 SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, LLC,
 SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS
 15 AMERICA, LLC, and SAMSUNG DIGITAL IMAGING CO., LTD.

16 UNITED STATES DISTRICT COURT
 17 NORTHERN DISTRICT OF CALIFORNIA

18
 19 ADVANCED MICRO DEVICES, INC., et al.,
 20 Plaintiffs and Counterdefendants,
 21 v.
 22 SAMSUNG ELECTRONICS CO., LTD., et al.,
 23 Defendants and Counterclaimants.

Case No. 3:08-CV-0986-SI

**DEFENDANTS' AND
 COUNTERCLAIMANTS' MOTION
 FOR SUMMARY JUDGMENT OF
 NON-INFRINGEMENT OF U.S.
 PATENT NO. 5,559,990**

REDACTED PUBLIC VERSION

**DATE: AUGUST 13, 2010
 TIME: 9:00 A.M.
 COURTROOM: 10, 19TH FLOOR
 JUDGE: THE HONORABLE SUSAN
 ILLSTON**

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NOTICE OF MOTION AND MOTION FOR SUMMARY JUDGMENT

TO ALL PARTIES AND THEIR COUNSEL OF RECORD:

PLEASE TAKE NOTICE that on August 13, 2010 at 9:00 a.m., or as soon thereafter as the matter may be heard before the Honorable Judge Illston, United States Court House, San Francisco, California, Defendants and Counterclaimants SAMSUNG ELECTRONICS CO., LTD., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, LLC, SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA, LLC, and SAMSUNG DIGITAL IMAGING CO., LTD., (collectively, "Samsung") will move and hereby do move for an order granting summary judgment under Rule 56 of the Federal Rules of Civil Procedure that the products Plaintiffs and Counterdefendants ADVANCED MICRO DEVICES, INC. and ATI TECHNOLOGIES, INC. (collectively, "AMD") accuse of infringing U.S. Patent No. 5,559,990 ("the '990 patent") do not infringe any of the asserted claims of that patent as a matter of law.

This motion is made on the following three separate and independent grounds: First, none of the accused products satisfy the "Y-select circuit" limitation of all asserted claims. Second, none of the accused products satisfy the "plurality of sense amplifier circuits . . . for amplifying signals from a column selected by the Y-select circuit" limitation of all asserted claims. Third, none of the accused products alternate reading between multiple subarrays during a burst mode read operation as required by claim 22.

This motion is based on this Notice of Motion and Motion; the accompanying Memorandum of Points and Authorities; the accompanying declarations of Laura E. Muschamp and evidence attached thereto; the pleadings and papers on file in this case; and any argument or evidence the Court may receive at the hearing on this motion.

MEMORANDUM OF POINTS AND AUTHORITIES**I. INTRODUCTION**

AMD alleges infringement by Samsung of independent claim 20 and two of its dependent claims, 22 and 23 of U.S. Patent No. 5,559,990 ("990 patent"). For purposes of this motion,

1 Samsung accepts AMD's allegations regarding the operation of the accused Samsung memories.
2 The dispute lies solely in the proper construction of three claim limitations.

3 The first two claim terms that require construction are the "Y-select circuit" and "plurality
4 of sense amplifiers . . . for amplifying signals from a column selected by the Y-select circuit"
5 limitations contained in independent claim 20. Muschamp Decl., Ex. 1, U.S. Patent No. 5,559,990
6 ("hereinafter, Ex. 1, '990 patent") col.17 ll.3-5. These terms have not been construed by this Court.
7 Samsung construes these terms in light of the specification and according to their ordinary meaning
8 as follows:

- 9 • A "Y-select circuit" is a circuit located between the memory array and the sense amplifiers
10 that selects the column that is to be provided to the sense amplifier circuit for amplification.
11 The proper meaning of "Y-select circuit" is apparent from the specification as well as from
12 the plain language of claim 20.
- 13 • "A plurality of sense amplifier circuits . . . for amplifying signals from a column selected by
14 the Y-select circuit of the subarray" means exactly what it says: the sense amplifiers
15 amplify signals from columns selected by the Y-select circuit. To perform this function the
16 Y-select circuit must select a column and provide the selected column to the sense amplifier
17 for amplification. The plain language of the claim limitation requires the signal amplified
18 by the sense amplifiers to be provided from the Y-select circuit. The signal cannot be *from*
19 the Y-select circuit unless the Y-select circuit selects the column before it is provided to the
20 sense amplifier for amplification.

21 Reading the Y-select circuit limitation together with the plurality of sense amplifier circuits
22 together leaves no doubt that the Y-select circuit must select the columns provided to the sense
23 amplifier circuits. The sense amplifier receives the signal from the Y-select circuit, and only after
24 receiving this signal can the sense amplifier circuits amplify the signal *from the selected column*.

25 Properly construed, Samsung does not infringe the Y-select circuit or plurality of sense
26 amplifiers limitations. AMD's infringement contentions fail to identify a Y-select circuit that
27 selects columns that are then amplified by the sense amplifiers. Instead, AMD focuses on circuitry
28 that receives the already amplified signals from the sense amplifiers as the Y-select circuit.
Because the accused Samsung memories operate in the opposite manner from what is claimed,
summary judgment of no infringement should be granted.

The third limitation in dispute, burst mode, is found in all asserted claims and was
previously construed by this Court as "a mode for sequentially accessing memory locations in

1 which the memory receives the address of one memory location and provides in response the
2 contents of a plurality of consecutive memory locations.” Dkt. 255, Claim Construction Order, at
3 7, 9. Claim 22 requires reading from multiple subarrays during a burst read operation. A burst read
4 operation involves reading in response to a single address, and it is undisputed that the Samsung
5 memories can only read from a single subarray in response to a single address. Summary judgment
6 of claim 22 should be granted for this additional reason.

7 **II. FACTUAL BACKGROUND**

8 **A. The Technology of the '990 Patent**

9 The '990 patent relates to memory devices. Memory devices are electronic components
10 that store information in memory locations. The memory locations are organized in rows and
11 columns, such that each memory location is uniquely identified by its row and column position. To
12 access this information, an address is provided that identifies the row and column position for the
13 memory location to be accessed. Ex. 1, '990 patent, col. 1 ll.8-30.

14 The '990 patent discloses an allegedly novel memory device that is divided into a plurality
15 of subarrays that alternately transfers information to the memory output of the device. The '990
16 patent discloses the memory as two halves that are mirror images of each other. Ex. 1, '990 patent,
17 col.3 ll.49-51. Each half of the memory contains its own dedicated subarray, registers, decoders, y-
18 select circuitry, and sense amplifiers. Ex. 1, '990 patent, fig.3; col.3 ll.52-53.

19 To access a memory location, an address is received by X- and Y-registers which then pass
20 the address to the X- and Y-decoders. Ex. 1, '990 patent, col.4 ll.40-48. The X-decoder decodes
21 the address to create a signal that will select a row, and the Y-decoder decodes the address to
22 create a signal that will be used to select the column. Ex. 1, '990 patent, col.4 ll.12-25. The Y-
23 decoder provides its signal to a Y-select circuit which performs the actual selection of the column.
24 Ex. 1, '990 patent, col.4 ll.10-13; ll.52-53. The Y-select circuit forms a connection between the
25 memory location and the sense amplifier to allow the information stored in the memory location to
26 flow to the sense amplifiers. The sense amplifiers amplify the information from the columns
27 selected by the Y-select circuit. Ex. 1, '990 patent, col.4 ll.52-56. A control circuit is then used to
28

1 select the sense amplifiers to provide the amplified information to the memory output. Ex. 1, '990
2 patent, col.5 ll.10-26; col.13 ll.58-59.

3 The '990 patent also teaches that the memory operates in a burst mode. The '990 patent
4 admits that burst mode memories are prior art but claims an allegedly improved "boundaryless
5 burst mode access . . . [that] can continue for any number of locations . . . not only groups of four
6 locations" Ex. 1, '990 patent, col.1 ll.58-64; *see also* col.5 ll.37-44; Abstract. To achieve this
7 boundaryless burst mode, the '990 patent teaches to divide the memory into multiple subarrays and
8 alternate reading between the subarrays. Ex. 1, '990 patent, col.1 ll.65-67; col.2 ll.27-37. The '990
9 patent teaches that burst mode improves speed because only a single address has to be decoded
10 even though multiple memory locations are accessed. Ex. 1, '990 patent, col.1 ll.47-50.

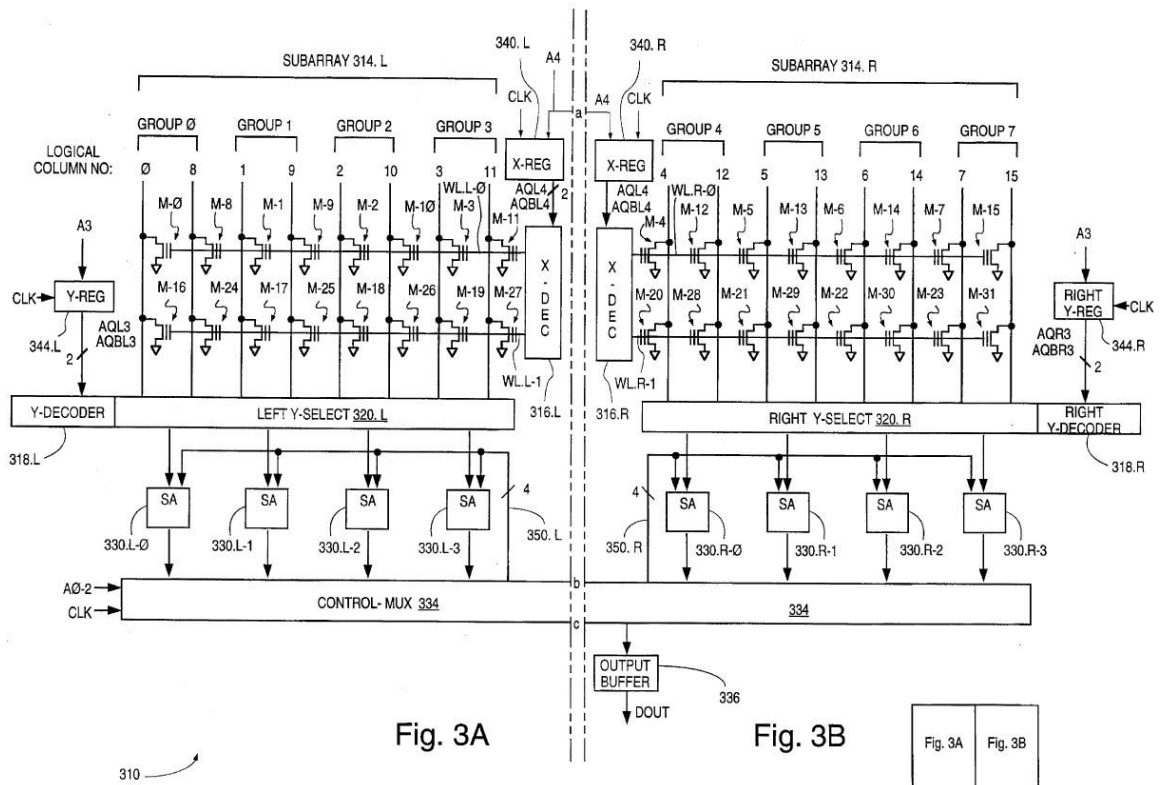
11 **B. The Limitations of Claims 20 and 22**

12 The memory of claim 20 is defined in terms of a specific memory structure. Claim 20
13 recites a plurality of subarrays and for each subarray one X-decoder and one Y-decoder, one X-
14 register for each X-decoder and one Y-register for each Y-decoder, one Y-select circuit, and a
15 plurality of sense amplifier circuits. Ex. 1, '990 patent, col.16 l.61-col.17 l.3. Claim 20 recites that
16 the Y-select circuit selects columns associated with the memory cells and provides that information
17 to the sense amplifiers to amplify the signal from the selected columns. Ex. 1, '990 patent, col.17
18 ll.1-6. A control circuit selects the amplified information from the sense amplifier to provide
19 information to the memory output. Ex. 1, '990 patent, col.17 ll.9-10.

20 For purposes of this motion, the key limitations of claim 20 are as follows:

- 21 • "one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-
22 decoder of the subarray to select all the columns that occupy a selected position in the
23 groups of the subarray;" Ex. 1, '990 patent, col.16 l.66-col.17 l.2, and
- 24 • "a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for
25 amplifying signals from a column selected by the Y-select circuit of the subarray;" Ex. 1,
26 '990 patent, col.17 ll.3-6.

27 Figure 3 illustrates the relationship between the Y-select circuit and the sense amplifiers.
28



Ex. 1, '990 patent, fig.3. As shown in Figure 3, the Y-decoder provides a signal to the Y-select circuit. The Y-select circuit is located between the memory array and the sense amplifiers. The Y-select circuit uses the information from the column decoder to select the columns in the memory array to provide information to the sense amplifiers for subsequent amplification.

The memory structure and flow of information recited by claim 20 is also shown in Figure 7. Ex. 1, '990 patent, fig.7. Figure 7 shows that the Y-select circuit (320.x) selects columns from the subarrays (314.x), the Y-select circuit provides information from the memory cells corresponding to the selected columns to the sense amplifiers (330.x), the sense amplifiers amplify the selected information, and the control circuit (334) selects the sense amplifier to provide information to the memory output (DOUT).

The asserted claims also require that the memory operate in a burst mode. Claim 22 further requires that during the burst mode operation, data is alternately read from two subarrays. In other words, the burst read must occur across subarrays, not just within one subarray.

1 **C. The Samsung Memory Devices**

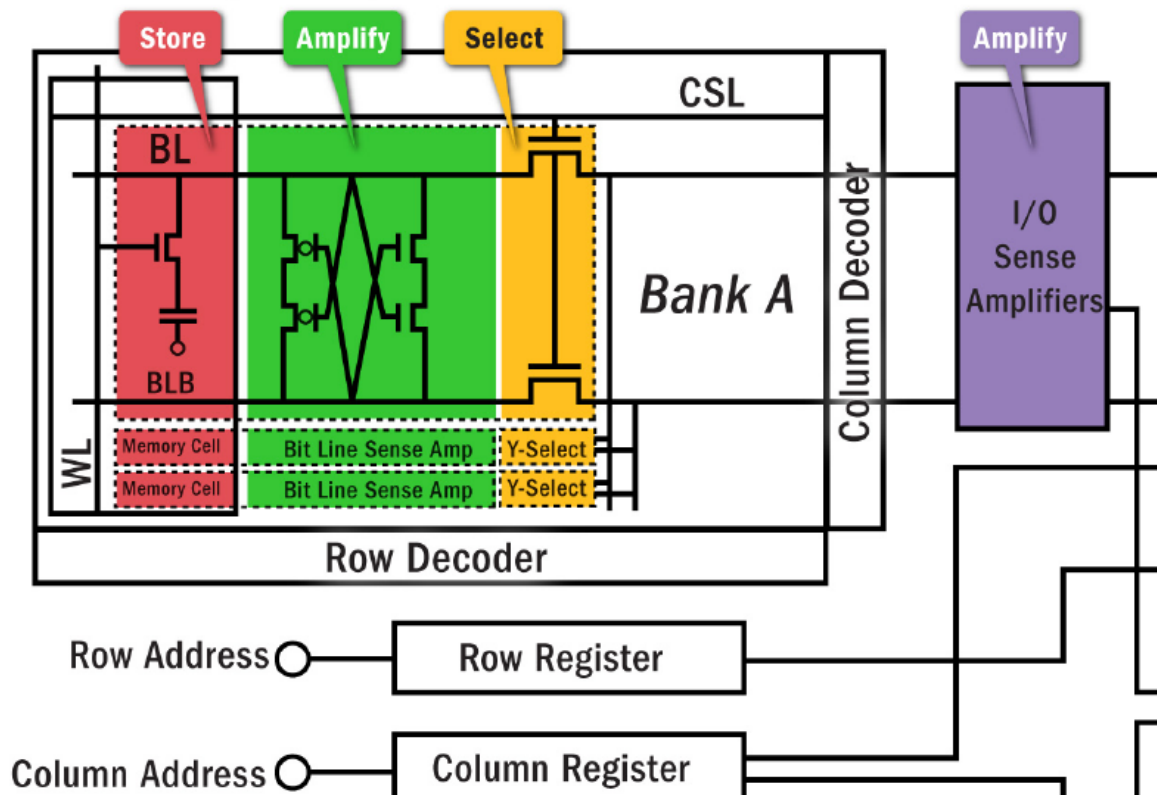
2 The accused Samsung memory devices are divided into multiple banks or subarrays. The
3 accused Samsung devices only read information from one subarray in response to a single address.
4 To access information from a second subarray, a new address must be provided. *See e.g.*,
5 Muschamp Decl. Exs. 2-8, AMD’s Final Infringement Contentions (“FICs”), Cheng ’990 Group 2
6 at 80-81; Cheng ’990 Group 3 at 69-70; Cheng ’990 Group 12 at 65-66; Cheng ’990 Group 14 at
7 62-64; Cheng ’990 Group 15 at 77-78; Cheng ’990 Group 16 at 65-66; Cheng ’990 Group 17 at 64-
8 65.

9 The accused Samsung devices have two types of sense amplifiers. The bit line sense
10 amplifiers are directly connected to the columns/bit lines. There is one bit line sense amplifier for
11 each column. The bit line sense amplifiers amplify the signals stored in the memory cells. The
12 output of the bit line sense amplifiers are connected to pass transistors. The pass transistors are
13 connected between the bit line sense amplifiers and the I/O sense amplifiers. These pass transistors
14 receive a signal from the Y-decoder to select which bit line sense amplifiers will provide
15 information to the IO sense amplifiers. AMD identifies these transistors as the Y-select circuit.
16 Muschamp Decl. Exs. 2-8, AMD’s FICs, Cheng ’990 Group 2 at 59-62; Cheng ’990 Group 3 at 54-
17 56; Cheng ’990 Group 12 at 45-49; Cheng ’990 Group 14 at 46-50; Cheng ’990 Group 15 at 59-62;
18 Cheng ’990 Group 16 at 50-54; Cheng ’990 Group 17 at 50-54.

19 The structure of the memory cells, bit line sense amplifiers, Y-select circuits and IO sense
20 amplifiers in the Samsung products is provided below:
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Samsung Memory Device Structure: Amplification Within Bank



As can be seen from the above graphic, the bit line sense amplifiers amplify signals from a memory cell. After the bit line sense amplifiers amplify this information, the pass transistors (Y-select circuit) are used to select the bit line sense amplifiers that will provide information to the IO sense amplifiers. Only the IO sense amplifiers amplify a signal selected by the Y-select circuit. The bit line sense amplifiers amplify the signals from the memory cells before the Y-select circuit makes a selection.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

1 The Samsung devices also have a burst mode in which multiple memory locations are read
2 in response to a single address. The burst mode in the Samsung products is limited to reading from
3 4, 8 or 16 memory locations located in the same subarray and the same row. To read from a
4 different subarray or a different row, a new address must be provided to start a new burst operation.
5 The Samsung devices cannot alternate reading between multiple subarrays in response to one
6 address and cannot perform a boundaryless burst. Muschamp Decl. Exs. 2-8, AMD's FICs, Cheng
7 '990 Group 2 at 80; Cheng '990 Group 3 at 68-69; Cheng '990 Group 12 at 64; Cheng '990 Group
8 14 at 59, 62; Cheng '990 Group 15 at 72, 76; Cheng '990 Group 16 at 60, 65; Cheng '990 Group 17
9 at 57, 63-64.

10 III. LEGAL STANDARD

11 Summary judgment is appropriate when no genuine issue of material fact exists and the
12 moving party is entitled to judgment as a matter of law. *Celotex Corp. v. Catrett*, 477 U.S. 317,
13 322-23 (1986); *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 247-48 (1986). "Summary
14 judgment is as appropriate in a patent case as in any other [C]ourt[s] should utilize the
15 salutary procedure of Fed. R. Civ. P. 56 to avoid unnecessary expense to the parties and wasteful
16 utilization of the jury process and judicial resources." *Barmag Barmen Maschinefabrik AG v.*
17 *Murata Mach., Ltd.*, 731 F.2d 831, 835 (Fed. Cir. 1984). To defeat a summary judgment motion,
18 the opposing party must do "more than simply show that there is some metaphysical doubt as to the
19 material facts." *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 586 (1986).
20 Instead, the opposing party must set forth "specific facts showing that there is a genuine issue for
21 trial." Fed. R. Civ. P. 56(e); *Id.* at 587.

22 For literal infringement, the patentee must establish that every claim limitation is found in
23 the accused product. *General Mills, Inc. v. Hunt-Wesson, Inc.*, 103 F.3d 978, 981 (Fed. Cir. 1997).
24 If the patentee's "proof is deficient in meeting an essential part of the legal standard for
25 infringement," summary judgment should be granted. *TechSearch L.L.C. v. Intel Corp.*, 286 F.3d
26 1360, 1372 (Fed. Cir. 2002). Summary judgment should also be granted if only one conclusion as
27 to infringement could be reached by a reasonable jury." *Id.* at 1369.
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1 Summary judgment of noninfringement is also appropriate when the parties do not dispute
2 any relevant facts regarding the accused product. *General Mills, Inc. v. Hunt-Wesson, Inc.*, 103
3 F.3d 978, 983 (Fed. Cir. 1997). When the structure of the accused device is not in dispute, “the
4 question of literal infringement collapses into claim construction and is amenable to summary
5 judgment.” *Id.*

6 Claim construction is a matter of law. *See Markman v. Westview Instruments, Inc.*, 517
7 U.S. 370, 390 (1996). “It is elementary that claim construction begins with, and remains focused
8 on, the language of the claims.” *Biagro Western Sales, Inc. v. Grow More, Inc.*, 423 F.3d 1296,
9 1302 (Fed. Cir. 2005). “[T]he words of a claim are generally given their ordinary and customary
10 meaning, which is the meaning the term would have to a person of ordinary skill in the art at the
11 time of the invention.” *Id.* at 1302, citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed.
12 Cir. 2005) (en banc). “[E]ach term must be construed to implement the invention described in the
13 specification.” *On Demand Machine Corp. v. Ingram Indus., Inc.*, 442 F.3d 1331, 1344 (Fed. Cir.
14 2006) citing *Autogiro Co. of Am. v. United States*, 384 F.2d 391, 397-98 (Ct. Cl. 1967) (“use of the
15 specification as a concordance for the claim . . . is a basic concept of patent law”). “[T]he
16 specification is always highly relevant to the claim construction analysis. Usually, it is dispositive;
17 it is the single best guide to the meaning of a disputed term.” *Semitoool, Inc. v. Dynamic Micro Sys.*
18 *Semiconductor Equip. GmbH*, 444 F.3d 1337, 1347 (Fed. Cir. 2006) citing *Phillips v. AWH Corp.*,
19 415 F.3d 1303, 1315 (Fed. Cir. 2005) (en banc). “The construction that stays true to the claim
20 language and most naturally aligns with the patent's description of the invention will be, in the end,
21 the correct construction.” *Renishaw PLC v. Marposs Societa' Per Azioni*, 158 F.3d 1243, 1250
22 (Fed. Cir. 1998).

23 IV. ARGUMENT

24 A. Summary Judgment of No Literal Infringement of Claim 20 Should be Granted 25 Because Samsung Does Not Have a Y-select Circuit to Select Columns that Are 26 Amplified by the Plurality of Sense Amplifiers.

26 Under the plain meaning of claim 20, read in light of the specification, the term “Y-select
27 circuit” requires that it select the columns that subsequently provide the signals that are amplified
28 by the sense amplifiers. Even if the Court were to construe this limitation differently, the “plurality

1 of sense amplifiers” limitation explicitly requires the Y-select circuit to first select a column that is
 2 subsequently amplified by the sense amplifiers to practice claim 20. The circuitry AMD identifies
 3 as the “Y-select circuit” in the Samsung products does not provide information to the sense
 4 amplifiers for amplification, and the sense amplifiers do not amplify information provided from the
 5 Y-select circuit. The Samsung products do not practice claim 20.

6 **1. The “Y-select circuit” should be construed as a circuit that selects columns**
 7 **from an array and provides the signals to a sense amplifier.**

8 **a. The specification supports Samsung’s construction.**

9 The specification provides a complete description of the role of the Y-select circuit in the
 10 selection and amplification of information stored in the memory array. To read information from a
 11 memory array, an X-decoder select the row containing the desired information. A Y-decoder and
 12 Y-select circuit are then used to select the columns in the selected row that will provide information
 13 to the sense amplifiers for amplification and subsequent transfer to the output. The ’990 patent
 14 describes the relationship between the Y-decoder, Y-select circuit and sense amplifiers in the
 15 context of the prior art as follows:

16 Y-decoder 116 decodes the address *i* and signals Y-select circuit 118
 17 to select the column (that is, the bit line) connected to the memory
 18 location *M-i*. Y-select circuit 118 connects the selected bit line to
 19 sense amplifier circuit 120 which suitably amplifies the bit line
 signal. The amplified signal is latched into register 130 from which
 the signal is read to output buffer 134.

20 Ex. 1, ’990 patent, col.1 ll.25-30. The patent specification teaches that the Y-select circuit connects
 21 the column to the sense amplifier. *See, e.g.*, Ex. 1, ’990 patent, fig.3. The function of the Y-select
 22 circuit is to create a path between the memory array and the sense amplifier to provide the sense
 23 amplifier with selected information from the memory array.

24 The specification later confirms that the Y-select circuit of the claimed memory selects a
 25 column that is provided to the sense amplifier: “In either mode Y-select circuit 320.L selects
 26 simultaneously one column from each group 0 through 3 and provides the selected column signals
 27 to the respective sense amplifier circuits 330.L-0 through 330.L-3.” Ex. 1, ’990 patent, col.4 ll.6-9.
 28 In essence, the Y-select circuit is a switch located between the memory array and the sense

1 amplifiers to connect or disconnect the column from the sense amplifiers depending on whether the
2 columns are selected or not selected. The selected columns are connected via this switch to the
3 sense amplifiers for amplification.

4 The figures in the '990 patent confirm that the Y-select circuit lies between the memory
5 array and the sense amplifiers and selects the columns to provide information to the sense
6 amplifiers for amplification. Figures 1 and 2 are prior art memory devices that include a Y-select
7 circuit that connects the columns in the memory array to the sense amplifiers. Ex. 1, '990 patent,
8 fig.1; fig.2. Figure 3, 7 and 8 are embodiments of the alleged invention and, like the prior art
9 memories shown in Figures 1 and 2, include a Y-select circuit that connects the columns of the
10 memory array to the sense amplifiers. Ex. 1, '990 patent, fig.3; fig.7; fig.8. The figures, like the
11 specification, confirm that the Y-select circuit selects the columns that provide information to the
12 sense amplifiers for amplification.

13 The '990 specification unambiguously shows that the Y-select circuit performs its function
14 of selecting columns prior to amplification. The specification is the "single best guide to the
15 meaning of a disputed term," *Semitoil, Inc. v. Dynamic Micro Sys. Semiconductor Equip. GmbH*,
16 444 F.3d 1337, 1347 (Fed. Cir. 2006) *citing Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir.
17 2005) (en banc), and the Y-select circuit should be construed to require the selection of columns
18 prior to signal amplification.

19 **b. Samsung's construction is supported by the testimony of the AMD**
20 **engineers involved in the project that led to the '990 patent.**

21 The proper construction of "Y-select circuit" is not only apparent from the specification but
22 is also confirmed by AMD engineers involved in the development of the project that became the
23 '990 patent. Elvan Young and Pearl Cheng both worked on the project that led to the '990 patent
24 and both confirmed that a Y-select circuit is a circuit that selects a column and provides information
25 from the selected column to a sense amplifier.

26 Mr. Young originally defined the 97105A project that formed the basis for the '990 patent.
27 Muschamp Decl. Ex. 9, Exempt Performance Appraisal, Review Period 1/1/89 - 12/31/89, at 2
28 (AMD003618015); Muschamp Decl., Ex. 10, Deposition of Pearl Cheng ("Ex. 10, Cheng Dep.") at

1 31:17-18. Mr. Young testified that “[t]he Y-select circuitry is -- refers to the Y decoder circuitry. It
2 selects which one of the Y pass gates are going to be activated to connect the -- whichever bit line
3 with the current memory bit on it to the sense amplifiers.” Muschamp Decl., Ex. 11, Deposition of
4 Elvan Young (“Ex. 11, Young Dep.”) at 184:2-7. Mr. Young confirmed that a Y-select circuit
5 controls the flow of information between the memory array and the sense amplifiers, and that the
6 output of the Y-select circuit would provide information to the sense amplifiers. Ex. 11, Young
7 Dep., at 184:8-25. Because the function of the Y-select circuit is to select which columns to
8 provide to the sense amplifiers, a Y-select circuit is not used if a sense amplifier is connected to
9 every column—because no selection is required. Ex. 11, Young Dep. at 185:10-21.

10 The first named inventor of the ’990 patent confirmed that a Y-select circuit selects
11 columns that are then amplified by the sense amplifier. Pearl Cheng was the design engineer
12 assigned to do the detail design work on the 97105A project, and is the first named inventor on
13 the ’990 patent. During her deposition, Ms. Cheng described her alleged invention including the
14 role of the Y-select circuit. Ex. 10, Cheng Dep. at 36:23-42:4. Ms. Cheng explained that the Y-
15 select circuit selects a column and after the column has been selected the sense amplifiers amplify
16 the signal from the selected column: “And then the way memories work is you have an array
17 associated with the array, its decoder that selects your row, and a Y select that is controlled by Y
18 decoders that selects your column. *And once you select your bit, you sense it with a sense*
19 *amplifier.*” Ex. 10, Cheng Dep. at 37:13-17 (emphasis added).

20 The engineers involved in the project leading to the ’990 patent confirmed the meaning of
21 Y-select circuit provided by the specification. Y-select circuit should be construed by this Court as
22 a circuit that selects a column and provides information from the selected column to the sense
23 amplifiers for amplification. *Renishaw*, 158 F.3d at 1250 (“The construction that stays true to the
24 claim language and most naturally aligns with the patent's description of the invention will be, in
25 the end, the correct construction.”).

1 **2. The plurality of sense amplifiers limitation should be construed to require**
2 **the sense amplifiers to amplify signals received from the columns selected**
3 **by the Y-select circuit.**

4 **a. The plain language of the claim supports Samsung's construction.**

5 Even if the term "Y-select circuit" is not itself construed to require that the Y-select circuit
6 select columns to provide to the sense amplifiers, the "plurality of sense amplifiers" limitation
7 explicitly requires the Y-select circuit to first select a column that is subsequently amplified by the
8 sense amplifiers to practice claim 20. This additional limitation limits the manner in which the Y-
select circuit can function within the invention of claim 20.

9 Claim 20 requires a "plurality of sense amplifier circuits for each subarray, each sense
10 amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the
11 subarray." Ex. 1, '990 patent, col.17 ll.4-7. Claim 20 does not simply recite a plurality of sense
12 amplifier circuits for each subarray. Claim 20 requires that the sense amplifiers "amplify signals
13 from a column selected by the Y-select circuit." Ex. 1, '990 patent, col.17 ll.4-7. For the sense
14 amplifiers to amplify a signal received from the Y-select circuit, the Y-select circuit must select the
15 column and provide the signal to the sense amplifiers. If the reverse is true and the sense amplifiers
16 provide a signal to the Y-select circuit, the signal amplified by the sense amplifiers is not from the
17 Y-select circuit as required by claim 20.

18 The plain language of the plurality of sense amplifiers limitation requires that the sense
19 amplifiers receive signals *from* the columns selected by the Y-select circuit. This Court should
20 construe the plurality of sense amplifiers according to the plain language of the claims and hold that
21 the Y-select circuit must select the columns and then provide the selected columns to the sense
22 amplifiers for amplification. *Semitoool*, 444 F.3d at 1346, citing *Phillips*, 415 F.3d at 1314 ("[T]he
23 claims themselves provide substantial guidance as to the meaning of particular claim terms.").

24 **b. The specification supports Samsung's construction.**

25 The '990 specification uniformly teaches that the sense amplifiers amplify signals from the
26 columns previously selected by the Y-select circuit. Beginning with the Abstract, the '990 patent
27 teaches that "[t]he memory locations in the selected row and columns are read by the sense
28

1 amplifier circuits.” Ex. 1, ’990 patent, at [57] (Abstract). The ’990 patent further teaches that
2 “[t]he contents of the memory locations in the selected row and the selected columns are transferred
3 to the sense amplifiers corresponding to the respective groups[,]” Ex. 1, ’990 patent, col.2 ll.18-21,
4 and that “Y-select circuit 320.L selects simultaneously one column from each group 0 through 3
5 and provides the selected column to the respective sense amplifier circuits 330.L-0 through 330.L-
6 3.” Ex. 1, ’990 patent, col.4 ll.6-9.

7 The figures also confirm that the sense amplifiers receive information from the Y-select
8 circuit; they do not provide information to the Y-select circuit. Prior art Figures 1 and 2, as well as
9 preferred embodiments 3, 7, and 8 all illustrate, without exception, this positioning of the Y-select
10 circuit between the memory cell array and the sense amplifier circuits. This uniformity of position
11 leaves no doubt that the Y-select circuit must be located between the memory cell array and the
12 sense amplifier circuits for the sense amplifiers to amplify signals from a column selected by the Y-
13 select circuit.

14 The specification teaches that the sense amplifiers amplify signals from memory cells
15 corresponding to the selected rows and column. The selection must precede the amplification for
16 the sense amplifiers to amplify signals from the selected memory locations, and the plurality of
17 sense amplifier circuits limitation should be so construed. “[E]ach term must be construed to
18 implement the invention described in the specification.” *On Demand*, 442 F.3d at 1344. The
19 plurality of sense amplifier circuits limitation should be construed to require the Y-select circuit to
20 select columns for subsequent amplification by the sense amplifiers.

21 **3. The Samsung devices do not meet the “Y-select circuit” or “plurality of**
22 **sense amplifiers” limitations and do not infringe claim 20.**

23 A memory can only infringe claim 20 if there is a Y-select circuit located between the
24 columns of the memory array and the sense amplifiers. *See General Mills*, 103 F.3d at 981 (“Literal
25 infringement requires that every limitation of the patent claim be found in the accused infringing
26 device.”). This is necessitated by both the meaning of “Y-select circuit” and the limitation
27 requiring the Y-select circuit to select the column to be amplified by the sense amplifier. The sense
28 amplifiers cannot amplify signals from a column selected by the Y-select circuit unless the Y-select

1 circuit selects the columns from the memory array and provides the signals to the sense amplifiers.
2 Thus, to analyze infringement, the Y-select circuit and the sense amplifiers must first be identified.

3 As mentioned above, the Samsung products have both bit line sense amplifiers and IO
4 sense amplifiers. AMD claims that the bit line sense amplifiers are the “plurality of sense
5 amplifiers” recited in claim 20. *See, e.g.*, Muschamp Decl. Exs. 2-8, AMD’s FICs, Cheng ’990
6 Group 2, at 59-67; Cheng ’990 Group 3, at 54-58; Cheng ’990 Group 12, at 45-52; Cheng ’990
7 Group 14, at 46-52; Cheng ’990 Group 15, at 59-66; Cheng ’990 Group 16, at 50-56; Cheng ’990
8 Group 17, at 41-47. For purposes of this motion, Samsung accepts AMD’s allegation that the bit
9 line sense amplifier are the plurality of sense amplifiers.

10 The bit line sense amplifiers are connected directly to the columns of the memory array.
11 There is no Y-select circuit between the columns of the subarray and the sense amplifiers to select
12 the columns to be amplified by the sense amplifiers. Rather, AMD alleges that pass transistors
13 connected to the output of these sense amplifiers act as the Y-select circuit.

14 AMD admits that the pass transistors in the Samsung products receive amplified signals
15 from the sense amplifiers; they do not provide signals to the sense amplifiers. There is no dispute
16 that any column selection takes place after amplification of the columns by the bit lines sense
17 amplifiers. This operation is described in AMD’s FICs.

18 Specifically, AMD’s FICs describe the sense amplifiers in the Samsung memories as
19 providing signals to the Y-select circuit, not a Y-select circuit providing signals to the sense
20 amplifiers. For example, AMD states:

21 “[A] word line (WL) in the array is asserted which enables a transistor that shares the
22 charge stored in the DRAM cells with either the BL<x>b or BLB <x> line. . . . Then
23 the sense amplifier power supplies, LA and LAB, are turned on. . . . This causes the
24 sense amplifier to amplify the difference between BL<x>/BLB<x>. The sense
25 amplifier drives this difference back onto the same lines, BL<x>/BLB<x>, that were
the inputs of the sense amplifier. This shows that the sense amplifiers are for
amplifying the signal from a column (either BL<x>/BLB<x>).”

26 Muschamp Decl. Ex. 2, AMD’s FICs, Cheng ’990 Group 2, at 62. “The bit-line inputs to the top
27 sense amplifier . . . are BL<0> and BLB<0>.” *Id.* at 68.
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B. AMD Has Not Asserted Infringement of the Sense Amplifier Limitation Under the Doctrine of Equivalents and Any Attempt To Do So Would Improperly Read Language Out of the Claim.

AMD has not asserted that the “plurality of sense amplifiers limitation is infringed under the doctrine of equivalents. AMD is bound by its Final Infringement Contentions and cannot now rely on the doctrine of equivalents in attempt to salvage this patent. *See Genentech, Inc. v. Amgen, Inc.*, 289 F.3d 761, 773-74 (Fed. Cir. 2002) (holding that Northern California District Court did not abuse discretion in precluding Genentech from asserting doctrine of equivalents because “Genentech did not expressly include that theory in a claim chart, as strictly required under Civil Local Rule 16-9.” *Id.* at 773.). *See also MEMC Elec. Materials v. Mitsubishi Materials Silicon Corp.*, No. C 01-4925 SBA, 2004 WL 5363616, at *5 (N.D. Cal. 2004) (holding that MEMC was precluded from pursuing doctrine of equivalents because it failed to “provide infringement contentions sufficient to assert claims under the doctrine of equivalents pursuant to Patent L.R. 3-1.”); *Rambus, Inc., v. Hynix Semiconductor, Inc.*, Nos. C-05-00334 RMW, C-05-02298 RMW, C-06-00244 RMW, 2008 WL 5411564, at *3 (N.D. Cal. 2008) (holding that plaintiff’s failure to assert anything more than noting “that to the extent that any limitation is found to be not literally present, [plaintiff] asserts that such limitation is present under the doctrine of equivalents” provided an additional reason to dismiss plaintiff’s claims of infringement under doctrine of equivalents.)

1 Because Samsung does not literally infringe claim 20, and AMD has not asserted infringement
2 pursuant to the doctrine of equivalents, summary judgment of no infringement should be granted.

3 Further, any allegation of infringement under the doctrine of equivalents would fail as any
4 equivalents analysis requires the Court to truncate the “plurality of sense amplifiers” limitation to
5 remove the language “for amplifying signals from a column selected by the Y-select circuit of the
6 subarray.” Ex. 1, ’990 patent, col.17 ll.3-6. “[T]he doctrine [of equivalents] may not be invoked,
7 and summary judgment of non-infringement is appropriate, where the theory of equivalents would
8 entirely vitiate a particular claim element.” *Sharper Image Corp. v. Neotec, Inc.*, 373 F. Supp. 2d
9 993, 999 (N.D. Cal. 2005).

10 **C. Claims 22 and 23 Are Dependent on Claim 20 and Samsung Cannot Infringe**
11 **Claims 22 and 23 Since It Does Not Infringe Claim 20.**

12 AMD has accused Samsung memory devices of infringing claims 22 and 23 of the ’990
13 patent. Claims 22 and 23 are dependent claims of claim 20 and contain all the limitations of claim
14 20. Ex. 1, ’990 patent, col.3 ll.3-13; *see* 35 U.S.C. § 112 ¶ 4 (“A claim in dependent form shall be
15 construed to incorporate by reference all the limitations of the claim to which it refers.”).

16 Samsung does not and cannot infringe claims 22 and 23 because it does not infringe claim
17 20. “One who does not infringe an independent claim cannot infringe a claim dependent on (and
18 thus containing all the limitations of) that claim.” *Monsanto Co. v. Syngenta Seeds, Inc.*, 503 F.3d
19 1352, 1359 (Fed. Cir. 2007) (quoting *Wahpeton Canvas Co., Inc. v. Frontier, Inc.*, 870 F.2d 1546,
20 1552 n.9 (Fed. Cir. 1989) (further noting “[i]t is axiomatic that dependent claims cannot be found
21 infringed unless the claims from which they depend have been found to have been infringed”
22 *Id.* at 1553.)). *See also, Hoffer v. Microsoft Corp.*, 405 F.3d 1326, 1331 (Fed. Cir. 2005) (holding
23 that the dependent claim not infringed because the independent claim is not infringed); *Kim v.*
24 *ConAgra Foods Inc.*, 465 F.3d 1312, 1316 n.1 (Fed. Cir. 2006) (holding that because independent
25 claims are not infringed, “it necessarily follows in this case that the dependent claims are also not
26 infringed.”). As the accused Samsung memory devices do not practice the Y-select circuit and
27 plurality of sense amplifiers limitation of claim 20, the accused Samsung memory devices similarly
28 lack these limitations of dependent claims 22 and 23. Accordingly, the accused Samsung memory

1 devices cannot infringe claims 22 and 23, and summary judgment of no infringement should be
2 ordered.

3 **D. Summary Judgment of Claim 22 Should be Granted for the Additional Reason**
4 **that Claim 22 Requires Reading from Multiple Subarrays During a Burst**
5 **Mode but the Samsung Devices Can Only Read from a Single Array.**

6 AMD's infringement contentions are based on a new construction of burst mode that
7 includes reading from multiple locations in response to multiple addresses. This new construction
8 contradicts AMD's prior statements to this Court, AMD's statements to the Patent and Trademark
9 Office during prosecution, the patent specification, and this Court's construction. As such, AMD's
10 new construction should be rejected.

11 **1. This Court should affirm its construction of "burst mode" requiring**
12 **reading from multiple subarrays in response to a single address.**

13 "Burst mode" was construed by this Court to mean "a mode for sequentially accessing
14 memory locations in which the memory receives the address of one memory location and provides
15 in response the contents of a plurality of consecutive memory locations." Dkt. 255, Claim
16 Construction Order, at 7, 9. In reaching its construction of burst mode, the Court noted that the
17 parties agreed that "in burst mode, the memory receives the address of a single memory location
18 and responds by providing data from multiple memory locations with consecutive addresses." *Id.*
19 at 8.

20 Both parties proposed constructions of burst mode that required reading from multiple
21 memory locations in response to a single address. The only dispute between the parties was
22 whether burst mode required reading from consecutive physical locations. The Court ultimately
23 agreed with Samsung on the meaning of burst mode, but that dispute is not relevant to this motion.

24 Prior to making its representations to this Court, AMD repeatedly told the patent office that
25 burst mode required reading from multiple locations in response to a single address. For example,
26 in an early rejection, the patent examiner stated that "[a] burst mode transfer is nothing more than a
27 beginning mode address and an ending address which is equivalent to [a] serial transfer"
28 Muschamp Decl. Ex. 12, Final Office Action, dated June 23, 1994, at 3 (AMDFH000001775).
AMD disputed this characterization of burst mode. Notably for this motion, AMD represented to

1 the examiner that a burst mode required reading from multiple locations in response to single
2 address: “A burst mode transfer as claimed in Claim 2 is not any serial transfer but a serial transfer
3 in which the contents of a plurality of locations are provided in response to *the address of one*
4 *location.*” Muschamp Decl. Ex. 13, Amendment After Final Office Action (37 C.F.R. 1.312) dated
5 April 27, 1995, at 4 (AMDFH000001839) (emphasis added).

6 In its appeal brief, AMD again represented that burst mode required reading from multiple
7 locations in response to a single address. AMD told the Patent and Trademark Office that burst
8 mode “is a sequential access in which *the memory receives the address of one memory location* and
9 provides in response the contents of a plurality of consecutive memory locations.” Muschamp
10 Decl. Ex. 14, Appeal Brief, dated Sept. 27, 1995, at 2 (AMDFH000001856) (emphasis added).
11 This Court adopted AMD’s description of burst mode from its appeal brief as its claim
12 construction. Dkt. 255, Claim Construction Order at 7, 9.

13 AMD further described a prior art burst mode in which “four locations in the same memory
14 row can be read in burst mode *in response to one address.*” Muschamp Decl. Ex. 14, Appeal
15 Brief, dated Sept. 27, 1995, at 2 (AMDFH000001856) (emphasis added). AMD explained that its
16 alleged invention was an improvement because “memory locations in different rows having
17 different row addresses can be read in burst mode *in response to one address.*” *Id.* (emphasis
18 added). AMD repeatedly represented that burst mode, both as it existed in the prior art as well as
19 its claimed improved burst mode, refers to memory locations read in response to one address. The
20 benefit of burst mode in the alleged invention is that it can continue across rows and across
21 subarrays without requiring a new address, unlike prior art burst modes that ended after a fixed
22 number of locations and required a second address to continue reading from memory. *See* Ex. 1,
23 ’990 patent, col.1 ll.36-64; Muschamp Decl. Ex. 15, Amendment In Response to Office Action at
24 14 (AMDFH000001730); Muschamp Decl. Ex. 13, Amendment After Final Office Action (37
25 C.F.R. 1.312) dated April 27, 1995, at 3-5 (AMDFH000001838-40); Muschamp Decl. Ex. 14,
26 Appeal Brief, dated Sept. 27, 1995, at Appeal Brief at 2, 6-7 (AMDFH000001856, 1860-61).

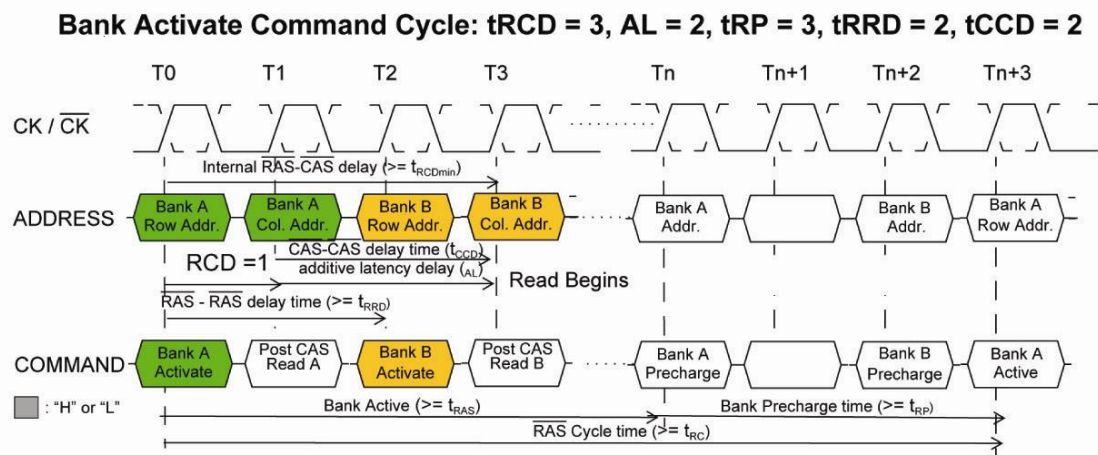
27 AMD represented to both this Court and the patent office that burst mode is a sequential
28 read of multiple memory locations in response to a single address. Claim 22 requires that certain

1 operations take place during a burst mode read operation. The operation described in claim 22 must
 2 take place “during a burst mode read operation,” and AMD’s statements to the patent office and to
 3 this Court require that these actions take place in response to one address.

4 **2. It is undisputed that the accused Samsung devices can only read from a**
 5 **single subarray in response to a single address and do not literally infringe**
 6 **based on this Court’s construction of “burst mode.”**

7 The Samsung memories do not have a continuous burst mode as described in the ’990
 8 patent. The burst modes in the Samsung products are limited to bursts of four, eight or sixteen
 9 locations. These locations must be located in the same row of a single subarray. Muschamp Decl.,
 10 Exs. 2-8, AMD’s FIC’s, Cheng ’990 Group 2 at 80; Cheng ’990 Group 3 at 68-69; Cheng ’990
 11 Group 12 at 64; Cheng ’990 Group 14 at 59, 62; Cheng ’990 Group 15 at 72, 76; Cheng ’990 Group
 12 16 at 60, 65; Cheng ’990 Group 17 at 57, 63-64.

13 AMD relies upon a mode of operation in the Samsung products referred to as seamless
 14 burst mode. The seamless burst mode does not refer to reading multiple locations in response to a
 15 single address. Rather, the seamless burst mode refers to a string of burst modes. So, for example,
 16 four locations could be read from one subarray in response to one address and a second burst mode
 17 could take place in a second subarray in response to a different address. This operation is shown in
 18 the following diagram which forms the basis for AMD’s infringement allegations regarding claim
 19 22.



1 Muschamp Decl., Exs. 2-8, AMD's FIC's, Cheng '990 Group 2 at 80-81; Cheng '990 Group 3 at
2 69-70; Cheng '990 Group 12 at 65-66; Cheng '990 Group 14 at 62-64; Cheng '990 Group 15 at 77-
3 78; Cheng '990 Group 16 at 65-66; Cheng '990 Group 17 at 64-65.

4 As can be seen in the above figure, the address for a location in Bank A (subarray A) is
5 provided and in response to the Bank A address memory locations are read from Bank A.
6 Subsequently, the address for a location in Bank B is provided and in response to the Bank B
7 address memory locations are read from Bank B.

8 There is no dispute that the Samsung products can only read from one subarray in response
9 to one address. To read from a second subarray, a new address must be provided. That is, a new
10 burst must be started for reading to take place from a second subarray.

11 Contrary to the operation of the Samsung devices, claim 22 requires alternating reading
12 from two subarrays in a burst mode read operation. Claim 22 captures the teaching in the
13 specification and prosecution history that burst mode refers to reading from multiple memory
14 locations in response to a single address and provides for a continuous burst mode that can read
15 from an unlimited number of memory locations in response to the single address. Ex. 1, '990
16 patent, col. 1 ll.36-50; col. 1 ll.58-col. 2 ll.37. This continuous burst mode is achieved by
17 alternating reads from multiple memory arrays, and these reads all take place *in response to* a single
18 address.

19 Claim 22 requires reading from multiple memory locations during a burst mode, that is in
20 response to a single address. Summary judgment of no infringement should be granted in favor of
21 Samsung based on the undisputed fact that the Samsung products cannot read from multiple
22 subarrays in response to a single address.

23 **3. AMD does not assert infringement of claim 22 under the doctrine of**
24 **equivalents and Samsung's motion for summary judgment of no**
25 **infringement of claim 22 should be granted.**

26 AMD has not asserted infringement of claim 22 under the doctrine of equivalents. As set
27 forth above, AMD is bound by its Final Infringement Contentions and cannot now rely on the
28 doctrine of equivalents. *See Genentech, Inc.*, 289 F.3d at 773 (Genentech precluded from asserting
doctrine of equivalents because it "did not expressly include that theory in a claim chart.");

1 *MEMC Elec. Materials*, 2004 WL 5363616, at *5 (MEMC precluded from pursuing doctrine of
2 equivalents because it failed to “provide infringement contentions sufficient to assert claims under
3 the doctrine of equivalents.”); *Rambus, Inc.*, 2008 WL 5411564, at *3 (Plaintiff precluded from
4 pursuing infringement under the doctrine of equivalents based on its failure to provide an
5 infringement analysis under the doctrine of equivalence.). Samsung does not literally infringe
6 claim 22, and AMD does not assert infringement under the doctrine of equivalents. Summary
7 judgment of no infringement of claim 22 should be ordered.

8 **V. CONCLUSION**

9 For the foregoing reasons, Samsung requests that the Court grant its motion for summary
10 judgment of non-infringement of the '990 patent as to all accused products and all asserted claims
11 on the basis that they do not meet the “Y-select circuit” limitation and/or on the basis that they do
12 not meet the “plurality of sense amplifiers . . . for amplifying signals from a column selected by the
13 Y-select circuit” limitation.

14 Samsung further requests that the Court grant it summary judgment of non-infringement of
15 claim 22 as to all accused products on the basis that they do not alternate reading from multiple
16 subarrays during a burst mode read operation.

17
18 DATED: July 1, 2010

COVINGTON & BURLING LLP

19
20 By Laura E. Muschamp

Laura E. Muschamp

21
22 Attorneys for Defendants and Counterclaimants
23 SAMSUNG ELECTRONICS CO., LTD., SAMSUNG
24 SEMICONDUCTOR, INC., SAMSUNG AUSTIN
25 SEMICONDUCTOR, LLC, SAMSUNG
26 ELECTRONICS AMERICA, INC., SAMSUNG
27 TELECOMMUNICATIONS AMERICA, LLC, and
28 SAMSUNG DIGITAL IMAGING CO., LTD.