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William H. Manning
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August 25, 2008

Hon. Susan Illston
United States District Court
Northern District of California
Courtroom 10, 19th Floor
450 Golden Gate Avenue
San Francisco, CA 94102

Re: *Advanced Micro Devices, Inc., et al. v. Samsung Electronics Co., Ltd., et al.*
Case No. CV-08-0986-SI

Dear Judge Illston:

The mediation with Judge Infante between the parties has concluded without agreement. Accordingly, AMD requests a case management conference to seek the Court's assistance with three issues requiring immediate resolution if the Court's deadlines are to be met:

1) the single unresolved issue in the parties' stipulated protective order;

2) production of Samsung documents, central to proving infringement, that Samsung has stated will not be produced; and

3) identification of AMD documents responsive to the unfocused Samsung discovery requests.

All these issues can be resolved with a single solution: prompt identification of exemplar products for discovery and trial purposes. Although Samsung has acknowledged that identification of exemplars offers a path to resolution, it has steadfastly refused to act on this acknowledgement. Accordingly, AMD requests an in-person conference with the Court where these issues can be discussed and where AMD can share background information on the technology involved that will assist the Court in resolving these issues.

I. Protective Order

The lone remaining protective order issue is whether Samsung will produce documents it designates with the highest level of confidentiality at Heller Ehrman's office in San Francisco, or instead at the office of Robins, Kaplan, Miller & Ciresi in Minneapolis. Samsung has demanded that AMD's outside counsel and experts review these documents at the offices of Heller Ehrman.

This demand is unreasonable given the importance of the documents, the low risks inherent in producing such documents at the office of Robins, Kaplan, Miller & Ciresi, and the burden that conducting a review in this manner would impose on AMD.

According to Samsung's counsel, Samsung plans to use the most-confidential protective order designation for its layout database, which contains documents such as chip schematics and diagrams. These documents set out the physical structure of the Samsung accused products. They will be vital to proving infringement and will be numerous given the number of accused Samsung products.

Because Samsung represents that the database holds the information in a format that can be used in a fabrication facility to make the chips, Samsung is afraid that someone could take the files from counsel's office and use them to produce copies of Samsung's devices.

Such fears are unfounded. In the last five years, Robins, Kaplan, Miller & Ciresi has safely hosted without incident some of the most sensitive information in the computer industry, including RTL code for Intel's Pentium line of microprocessors and the source code for Microsoft's Windows operating system. Indeed, a Robins, Kaplan, Miller & Ciresi attorney recently personally returned RTL to Intel, maintaining personal custody of that code on the flight from Minneapolis to San Francisco. This was done at Intel's request after Robins lawyers initiated communication with Intel and at Robins' expense. Robins is familiar with maintaining the highest security levels for this sensitive information, including utilizing non-networked computers and employing double- and triple-locked doors with keyed access limited to just a few attorneys and experts.

In contrast, the burdens that would result from requiring AMD to review documents at Heller Ehrman's office are quite real. Given that there are over 15,000 accused products (if Samsung fails to identify the 30-50 proper exemplar products), it could take several months of full-time work for AMD's experts to review the documents that demonstrate infringement. AMD's experts are likely to work weekends and evenings to complete their review. Samsung's counsel has indicated that access during weekends and evenings is unlikely. Also, AMD's experts and consultants often discuss the technical aspects of the documents as they relate to infringement. Such discussions, which are integral to engineering, will be difficult or impossible to conduct at opposing counsel's offices. Finally, Samsung will be able to monitor the amount of time that AMD's testifying and consulting experts spend reviewing documents, giving Samsung insights into AMD's litigation strategy.

AMD has proposed that Samsung's layout database should be produced on non-networked computers in a locked room. The locked room would be located in Robins, Kaplan, Miller & Ciresi's Minneapolis office. That office has locks on all floor access doors. Keys to that room would be made available to only a small number of lawyers and a paralegal who are working on the Samsung matter. Samsung has rejected this proposal.

II. Samsung's Document Production

AMD served Samsung with targeted document requests on May 9, seeking documents relating to Samsung's accused products. AMD significantly aided Samsung's document collection efforts by providing Samsung with an itemized list identifying accused products. Samsung has already indicated that it has no intention of producing technical documents that reflect all of the Samsung accused products because there are too many accused products. Instead, Samsung has suggested that it will produce documents that represent only a subset of the accused products. Samsung has offered no explanation for how it will select which documents to produce and which to withhold, nor has Samsung agreed that its subset constitutes exemplars for the other accused products.

Samsung cannot have it both ways. Even though it is not producing the technical documents for all accused products, Samsung would require infringement proof at trial for all these products. Absent agreement on exemplars, AMD will be required to prove at trial infringement for each and every one of the accused products without the benefit of Samsung discovery responses pertaining to those products. Consequently, Samsung must either identify exemplar products or fully respond to AMD's discovery on each and every one of the accused products.

III. AMD's Document Production

AMD has offered to identify exemplars of AMD products that are accused of infringing Samsung's patents, but Samsung has yet to provide the information needed to allow AMD to complete this identification. Samsung has served requests seeking documents relating to AMD's accused products but its requests are vague and overbroad because, unlike AMD, Samsung has not identified specific accused products and has described only general lines of processors. The problem is compounded by Samsung's failure to link its discovery requests to the Samsung asserted patents. Without further clarification, AMD cannot identify appropriate exemplars or reasonably collect all responsive documents by the parties' October 15 document production deadline.

IV. Exemplars

An exemplar products agreement presents a singular solution to these three issues discussed above. Such an agreement would reduce the number of products in dispute. A reasonable exemplars agreement would reduce the number of Samsung accused products from over 15,000 to less than 50. Consequently, the exemplars agreement would 1) limit the number of technical documents Samsung must produce, thereby reducing Samsung's concern for stolen documents; and 2) provide AMD with the clarification it needs to collect and produce the documents Samsung has requested.

Samsung's concerns regarding the number of accused products and associated discovery would be resolved because discovery would be limited to approximately 50 Samsung products.

Although the use of exemplars in this case was expected by the parties, Samsung has thus far refused to identify exemplars or to work with AMD to reach this result. On May 6, immediately

after Samsung identified Heller Ehrman as its outside counsel, my partner, Brad Engdahl, and I flew to San Francisco for a face-to-face meeting with Mr. Haslem and other Heller Ehrman counsel. At this initial meeting, the parties agreed that exemplar products would streamline nearly all aspects of the case. This was not surprising, as exemplars are often used in patent litigation. Indeed, one court has ordered the identification of exemplars in litigation involving large numbers of accused products. *Connectel, LLC v. Cisco Sys., Inc.*, 391 F.Supp.2d 526, 528 (E.D. Tex. 2005) (ordering plaintiff to submit preliminary infringement contentions based on designated exemplar accused infringing products). Samsung itself has proposed exemplars in patent litigation. In *Rambus, Inc. v. Hynix Semiconductor, Inc.*, Case No. 5:05-cv-00334-RMW, currently pending in this District, Samsung proposed that one part represent all DDR2 SDRAM and GDDR2 SDRAM memory products in suit. These same memory product lines are also at issue in this case.

On June 10, AMD sent Samsung a 7-page letter proposing that the parties begin a discussion about establishing exemplar product categories in the interests of streamlining the litigation. AMD laid out in detail, for each of its 7 asserted patents, exemplar categories that would allow the parties to identify a reasonable number of products for each category for purposes of discovery. Following discovery, the parties could identify a single product from each category, for the purposes of trial. *See* Ex. A, letter dated June 10, 2008 from William Manning to Robert Haslem.

On June 25, Samsung's counsel responded, stating that it was "willing to consider" entering into an exemplar agreement, but required "more information about AMD's infringement case." *See* Ex. B, letter dated June 25, 2008 from Christine Haskett to William Manning at 1. Samsung specifically requested infringement claim charts. *Id*. at 1-4.

Two weeks later, on July 10, AMD responded by providing Samsung 22 detailed claim charts that map each and every element of the asserted claims of each patent to specific Samsung accused products. *See* Ex. C, letter dated July 10, 2008 from William Manning to Christine Haskett and Ex. D, an example of one of the 22 claim charts provided to Samsung. AMD explained that these charts will likely correspond to its Preliminary Infringement Contentions, which are due on September 30, 2008. In addition, AMD provided to Samsung, in electronic and paper copies in several bankers' boxes, all of the supporting source documents referenced in the claim charts, including third-party teardown reports of Samsung products. AMD has also sent Samsung a product list that identifies 15,000 Samsung products that practice one or more of the asserted patents. We will have this product list at any case management conference that is scheduled to show the Court the detail that AMD has achieved on the product list without any formal discovery occurring.

AMD's letter of July 10 also provided a thorough explanation on a patent-by-patent basis of AMD's methodology used to identify proposed exemplar products. AMD estimated it should need "detailed infringement discovery for only 40 products." *Id.* at 2. Despite all of the information provided by AMD, Samsung has yet to respond, much less suggest proposed exemplars.

In the July 10 letter, AMD further advised Samsung that AMD would agree to exemplars regarding its own products to assist Samsung in asserting its six patents against AMD. AMD advised Samsung that AMD "has taken steps to identify exemplar AMD products that Samsung has accused of infringement." *Id.* at 2. To complete this identification, AMD requested that Samsung "provide information as AMD has provided with this letter, including infringement claim charts and supporting documentation." *Id.* Although Samsung had indicated that exemplar AMD products would be appropriate, Samsung has not provided AMD with any information that would allow AMD to create exemplar categories. This is particularly important because Samsung, unlike AMD, failed to identify *any* specific accused products in its pleadings or discovery requests.

Having received no response to its letter of July 10, on July 30 AMD renewed its request that Samsung provide detailed information regarding its infringement contentions. *See* Ex. E, letter dated July 30, 2008 from Cole Fauver to Christine Haskett.

To date, Samsung has not supplied the requested information. Samsung must identify what features of AMD's products are alleged to infringe before AMD can categorize the accused AMD products. To respond to Samsung's discovery requests by October 15, AMD needs the requested information immediately.

Given these realities, AMD is perplexed as to why Samsung has resisted identifying exemplars for use in this litigation. AMD believes that a case management conference with the Court in September would be of great assistance in resolving these issues. AMD further believes that the Court would benefit from a more in-depth understanding of the technology involved in the case and the patents, in that it would enhance the Court's ability to guide the parties to mutual agreement on these and future case management issues. Attached as Exs. F-L are tutorial materials describing the technology pertaining to each of the 7 AMD patents-in-suit. AMD respectfully suggests that any case management conference include time for a brief discussion of the technology.

AMD appreciates the Court's consideration of this request.

Respectfully submitted,

ROBINS, KAPLAN, MILLER & CIRESI L.L.P.

William H. Manning

cc: Robert Haslem
Michael Plimack
Christine Haskett

Civ. No 3:08-cv-00986-SI

ADVANCED MICRO DEVICES, INC., et al.,

Plaintiffs,

V.

SAMSUNG ELECTRONICS CO., LTD., et al.,

Defendants.

EXHIBITS

EXHIBIT A	Letter dated June 10, 2008 from William Manning to Robert Haslem
EXHIBIT B	Letter dated June 25, 2008 from Christine Haskett to William Manning
EXHIBIT C	Letter dated July 10, 2008 from William Manning to Christine Haskett
EXHIBIT D	One of the 22 claim charts provided to Samsung on July 10, 2008
EXHIBIT E	Letter dated July 30, 2008 from Cole Fauver to Christine Haskett
EXHIBIT F	Demonstrative materials describing the technology pertaining to the Cheng ’990 patent-in-suit
EXHIBIT G	Demonstrative materials describing the technology pertaining to the Sakamoto ’893 patent-in-suit
EXHIBIT H	Demonstrative materials describing the technology pertaining to the Patel ’830 patent-in-suit
EXHIBIT I	Demonstrative materials describing the technology pertaining to the Iacoponi ’592 patent-in-suit
EXHIBIT J	Demonstrative materials describing the technology pertaining to the Purcell ’434 patent-in-suit
EXHIBIT K	Demonstrative materials describing the technology pertaining to the Pedneau ’200 patent-in-suit
EXHIBIT L	Demonstrative materials describing the technology pertaining to the Orr ‘879 patent-in-suit

EXHIBIT A

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June 10, 2008

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Re: ***Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al.***
Case No. CV-08-0986-SI

Dear Counsel:

The seven patents asserted by AMD implicate a wide range of Samsung products. AMD has a right to pursue discovery on each product in order to obtain proof that it infringes one or more patent claims. Samsung already has indicated that it believes such discovery will impose an undue burden. In this case, however, the structural and operational features of each product are highly relevant and subject to discovery.

We suggest that the parties open a discussion about an agreement to group Samsung's products in a way that will reduce the amount of necessary discovery and will streamline this case for trial. We propose that the parties agree on one exemplar product that will represent the structural and operational features of each group. Samsung would then agree that if AMD proves that the exemplar product embodies all elements of a patent claim, then all products in that group also embody all elements of that patent claim.

At this stage in the litigation, only Samsung has access to the detailed information regarding the structure and operation of the accused products. Before AMD will enter any stipulation regarding an exemplar product, Samsung must provide AMD with sufficient evidence that the exemplar does, in fact, represent the structural and operational features of all products in the group.

Identifying exemplar products will reduce the amount of detailed discovery that AMD will require to support its infringement case. It also will streamline trial and eliminate repetitive evidence regarding substantially similar Samsung products. We therefore suggest that the parties begin a process of identifying relevant groups of Samsung products and appropriate exemplar products to represent those groups.

In the following sections, we intend to open the discussion regarding potential product groups and exemplar products. This discussion does not represent any admission by AMD about the operation of Samsung products or waive AMD's right to rely on infringement proof that AMD obtains through formal discovery. Any agreement regarding exemplars would have to contain detailed, mutually acceptable language setting forth the effect of proving that the exemplars infringe and the manner in which the use of exemplars would limit discovery and the admissibility of evidence at trial. By opening this discussion, we are expressing our sincere interest in finding a mutually agreeable solution to this issue.

I. Cheng 5,559,990

Samsung's website indicates that it manufactures and sells memory falling into at least nine different categories, including DDR, DDR2, DDR3, SDRAM, GDDR, RDRAM, XDR, SRAM and NOR Flash. Samsung's publicly available datasheets for products falling within each of the memory categories noted above show that, within each category, most products share the operational and structural characteristics that are relevant to the asserted claims of the Cheng patent. We propose, therefore, that the parties agree on an exemplar Samsung product for each category.

To identify the appropriate exemplar product categories applicable to the Cheng patent, AMD will require detailed discovery of approximately 30 of the over 2000 memory products on the Exhibit A previously provided to Samsung by AMD. Based upon review of the materials Samsung produces in response to this discovery, AMD expects to be able to further narrow these representative product categories to perhaps 15, subject to Samsung's agreement that the operational and structural features of each product within these groups is the same for purposes of the asserted claims. Accordingly, we suggest that the parties agree that if the factfinder determines that a chosen exemplar embodies all elements of an asserted Cheng patent claim, then all other products grouped with that exemplar also embody all elements of that claim.

II. Sakamoto 5,248,893

As we understand it, Samsung makes two different types of transistors with gates that are recessed below the surface of the substrate (RCAT and S-RCAT). We have also seen references

to U-RCATS in the publicly available literature, but do not know for certain whether such products have hit the market yet. We are in possession of an image of cross section a S-RCAT transistor from a Samsung DRAM chip (K4T51083QE), which was attached to Plaintiffs' First Set of Requests for Admission. We have also seen cross sections of RCAT transistors in the publicly available literature written by Samsung engineers. *See e.g.* Kim, Kinam *Technology for sub-50 nm DRAM and NAND Flash Manufacturing* (IEEE 2005).

As a first step to reaching a stipulation, we would need you to identify which models of Samsung's DRAMs have RCAT transistors, which models have S-RCAT transistors, and which have traditional transistors with gates that cover a flat surface of the substrate. As to the S-RCAT transistors, the publicly available literature suggests that the S-RCAT transistors found in model K4T51083QE are representative of the S-RCAT transistors found in Samsung's DRAMs generally. However, we have not yet had the benefit of discovery to confirm this fact. Accordingly, we could handle the S-RCATs in a fashion that it similar to Iacoponi proposal discussed above. Samsung would provide us with satisfactory evidence that this fact is true, including proof that the transistors in other DRAMs operate the same way as the exemplar chip, have the same general appearance, are layered in the same fashion, and that the various components of the transistors have the same composition. Assuming that we could obtain such assurances, we could enter into a stipulation wherein we would agree that the resolution of the question of whether the exemplar chip infringes the Sakamoto patent would resolve the issue of S-RCATS generally.

As to the DRAM products with RCAT type transistors, we would need further information, as the publicly available literature does not tie Samsung's RCAT design to particular model numbers. Before reaching any stipulations, we would have to negotiate obtaining additional information about individual designs.

Finally, we would have to resolve whether there are DRAM products with gates that are recessed below the main surface other than RCATs and S-RCATS, and whether recessed gates are used in other Samsung products.

III. Patel 4,737,830

Given the wide variety of possible capacitor layouts, it is difficult for us to propose, based upon the information currently available to us, any stipulations regarding whether any particular products are representative of larger product groups for purposes of the Patel patent. Rather, it may make sense for us negotiate a multi-step process to streamline the issues. The first step of such process would be to resolve informally which products or groups of products have on-chip decoupling capacitors. We could then identify those claim elements that are genuinely in dispute between the parties. Once we have narrowed down the chips and the claim elements, we could isolate the chips that represent the different manifestations of that element in Samsung's chips. We could then stipulate that resolution of the issue of whether that element is present in the exemplar chip resolves the issue of whether that element is present in the broader group of chips that the chip represents. I understand that this proposal is somewhat vague, but it

is necessarily so given the nature of the patent, the nature of Samsung's products, and the current state of discovery.

IV. Iacoponi 5,545,592

AMD is in possession of images of cross-sections of contacts found in a Samsung DRAM chip (K4T1G164QA-ZCD5) and a NAND Flash chip (K9WAG08U1A). Copies of these images were attached to Plaintiffs' First Set of Requests for Admission. We believe that these contacts are representative of the contacts found in all Samsung's DRAMs and NAND Flash chips, respectively. However, we have not yet had the benefit of discovery to confirm this conclusion. Accordingly, before we could enter into any stipulations regarding these chips, Samsung would have to provide us with satisfactory evidence that the contacts found in these two chips are representative. Such evidence would not need to be in the form of a formal discovery exchange. It is our hope that we could work out a mechanism by which Samsung would provide us with the evidence informally. This evidence would have to be sufficient to allow us to conclude with confidence that the process used to manufacture the two exemplar chips is the same, in every material way, as the process used to manufacture Samsung's other DRAM and NAND Flash chips. Similarly, we would have to ensure that the contacts in other DRAMs and NAND Flash chips have the same general appearance as the exemplar chips, are layered in the same fashion, and that the various layers have the same composition.

Assuming that we could receive the appropriate assurances, we could enter into a stipulation by which the infringement portion of the trial would focus on the two exemplar chips. We could stipulate that the determination of infringement or non-infringement reached by the fact finder (whether it be the court on summary judgment or the jury after trial) regarding the two exemplar chips would apply to all DRAMs and NAND Flash chips that Samsung has made, used, sold, or imported into the United States.

Obviously, we would have to enter into a different stipulation if not all of Samsung's DRAMs and NAND Flash chips use the plasma nitridation process, or if there are material differences in the plasma nitridation processes used during fabrication of Samsung's chips. Further, we would have to have some mechanism for determining whether Samsung's products other than NAND Flash and DRAM chips have nitrided contacts. Regardless of the factual scenario, I am sure that there will be a way to streamline this portion of the case if we are both cooperative and creative.

V. Purcell 5,623,434

Publicly available information demonstrates that Samsung sells products that incorporate ARM7TDMI or ARM9TDMI cores licensed by ARM Holdings, PLC. Publicly available information also shows that those products satisfy all elements of claims from the Purcell patent. We propose, therefore, that the parties agree on an exemplar Samsung product that incorporates an ARM7TDMI core and an exemplar Samsung product that incorporates an ARM9TDMI core.

Samsung's website indicates that its S3C3410 application processor contains an ARM7TDMI core. AMD believes that all Samsung semiconductor parts that incorporate an ARM7TDMI core have the same relevant structural and operational features as the S3C3410 application processor. AMD suggests that the parties agree that if the factfinder determines that the S3C3410 application processor embodies all elements of any Purcell patent claim, then all other Samsung semiconductor parts that incorporate an ARM7TDMI core also embody all elements of that claim. In order to reach this agreement, AMD will need appropriate assurances and evidence from Samsung that the S3C3410 represents the structure and operation of all Samsung semiconductor parts that incorporate ARM7TDMI cores.

Samsung's website indicates that its S3C2410 application processor incorporates an ARM920T core. According to the ARM920T technical reference manual, that core contains an ARM9TDMI design. AMD believes that all Samsung semiconductor parts that incorporate an ARM9TDMI core have the same relevant structural and operational features as the S3C2410 application processor. We suggest that the parties agree that if the factfinder determines that the S3C2410 application processor embodies all elements of any Purcell patent claim, then all other Samsung semiconductor parts that incorporate an ARM9TDMI core also embody all elements of that claim. In order to reach this agreement, AMD will need appropriate assurances and evidence from Samsung that the S3C2410 represents the structure and operation of all Samsung semiconductor parts that incorporate ARM9TDMI cores.

AMD is unable to identify potential exemplar products for Samsung's proprietary semiconductor parts, because the relevant information resides in Samsung's sole possession, custody, or control. Agreeing on the exemplar products proposed above, therefore, will not eliminate AMD's need for discovery to determine whether Samsung's proprietary semiconductor parts also practice the Purcell patent claims. AMD may be willing to agree on product groupings and exemplar products for proprietary parts if Samsung provides sufficient evidence and assurances to AMD regarding the structure, operation, and shared features of Samsung's proprietary products.

VI. Pedneau 5,377,200

Publicly available information shows that Samsung sells products that incorporate ARM7EJ-S, ARM9E-S, and ARM9EJ-S cores licensed by ARM Holdings, PLC. Publicly available information also shows that those products satisfy all elements of claims from the Pedneau patent.

ARM documentation shows that the relevant features of the ARM7EJ-S, ARM9E-S, and ARM9EJ-S cores operate in the same way. We propose, therefore, that the parties identify one exemplar product to represent all Samsung semiconductor parts that incorporate any of those three ARM cores.

Samsung's website indicates that the S3C2412 application processor incorporates an ARM926EJ-S core. We suggest that the parties agree that if the factfinder determines that the S3C2412 application processor embodies all elements of any Pedneau patent claim, then all other

Samsung semiconductor parts that incorporate an ARM926EJ-S, ARM9E-S, or ARM7EJ-S core also embody all elements of that claim. In order to reach this agreement, AMD will need appropriate assurances and evidence from Samsung that the S3C2412 represents the structure and operation of all Samsung semiconductor parts that incorporate ARM7EJ-S, ARM9E-S, and ARM9EJ-S cores.

Again, AMD is unable to identify potential exemplar products for Samsung's proprietary semiconductor parts, because the relevant information resides in Samsung's sole possession, custody, or control. Agreeing on the exemplar products proposed above, therefore, will not eliminate AMD's need for discovery to determine whether Samsung's proprietary semiconductor parts also practice the Pedneau patent claims. AMD may be willing to agree on product groupings and exemplar products for proprietary parts if Samsung provides sufficient evidence and assurances to AMD regarding the structure, operation, and shared features of Samsung's proprietary products.

VII. Orr 6,784,879

Publicly available Samsung user manuals do not provide detail about the user interface that Samsung provides on its consumer electronics devices that display video. AMD has identified a Samsung television, Samsung video camcorder, and Samsung cell phone that AMD believes represent the user interface incorporated in many other Samsung products in those categories. We therefore propose that Samsung stipulate to groups of televisions, camcorders, and cell phones that incorporate the same or similar user interface.

AMD believes that many other Samsung televisions have the same user menu interface and picture-in-picture capability as the Samsung LN-T4065F LCD television. Samsung has the information necessary to determine the television models that make up that group, but AMD would be willing to work toward an agreement on those models if Samsung provides sufficient evidence and assurances to AMD about the products' operation.

Similarly, AMD believes that the user interface demonstrated by the Samsung SC-HMX10 camcorder is present in other Samsung camcorders. Again, Samsung has the relevant information to determine the models in this group, but AMD would be willing to agree to those models with sufficient evidence and assurances from Samsung about the products' operation.

Finally, AMD believes that other Samsung cell phones use the same user interface as the Samsung Glyde SCH-u940. If Samsung provides evidence and assurances to AMD regarding the Samsung cell phones, their operation, and their shared features, AMD will consider agreeing on the cell phone models that make up that group.

AMD requires discovery on the user interfaces of other Samsung products that display video images in order to determine the scope of infringement of the Orr patent. AMD may be willing to discuss other exemplars and product groups based on formal discovery and other information provided by Samsung.

VIII. Conclusion

We believe that we can work to find a mutually agreeable solution that will allow AMD to obtain relevant structural and operational information about Samsung products, while at the same time streamlining discovery and trial preparation. We look forward to your response.

Sincerely,

ROBINS, KAPLAN, MILLER & CIRESI L.L.P.

William H. Manning

WHM/arf

Cc: John Bovich, Esq.
Brad P. Engdahl, Esq.

EXHIBIT B

HellerEhrman LLP

June 25, 2008

Via E-mail

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Re: Advanced Micro Devices, Inc., et al. v. Samsung Electronics Co., Ltd., et al.

Dear Bill:

I write in response to your letter of June 10, 2008 regarding the possibility of grouping the Samsung products that AMD accuses of infringement in order to streamline discovery in this case. Samsung is willing to consider entering into some type of an agreement regarding representative products, but in order to do so, we need more information about AMD's reasoning underlying its infringement case. Only then can we understand the product features that AMD sees as relevant to its case and propose appropriate groupings of products.

With this requirement in mind, I respond below to the discussion in your letter regarding each of the patents asserted by AMD in turn. None of this discussion should be construed as an admission by Samsung of infringement of any of the claims of the AMD patents.

I. U.S. Patent No. 5,559,990

You state in your letter that most of Samsung's memory products "share the operational and structural characteristics that are relevant to the asserted claims of the Cheng patent." You have not shared with us, however, what you believe those operational and structural characteristics to be. You then suggest that the parties "agree on an exemplar Samsung product for each category [of memory]."

In order to be able to suggest representative products for the purposes of this patent, we need to know what the "operational and structural characteristics" are that AMD sees as significant to its case. We propose that AMD provide us with a claim chart for one Samsung product that AMD contends infringes each of claims 1, 8, 15, 19, and 20 of the '990 patent. In particular, this chart must explain where in the accused product AMD contends the

limitations of these claims are met. Once we have that chart, we will be in a better position to consider whether there are products representative of groups of products that have in common the features that AMD believes are important to its infringement case.

Finally, with respect to this patent, you state that AMD will require detailed discovery on approximately 30 of Samsung's products, after which AMD expects to be able to narrow the representative products to 15. We are unclear as to where these numbers are coming from, particularly given that your letter lists only nine categories of memory. We also do not understand how AMD plans to narrow the number of representative products from 30 to 15. Please explain in detail your reasoning behind this proposal.

II. U.S. Patent No. 5,248,893

With respect to this patent, you have asked Samsung to provide "proof that the transistors in other DRAMs operate the same way as the exemplar [K4T51083QE] chip, have the same general appearance, are layered in the same fashion, and that the various components of the transistors have the same composition." Again, we may be able to provide you with this information once we know which aspects of the appearance, layering, and component compositions AMD sees as important to its case. We suggest that you provide us with a claim chart showing how AMD contends that this product infringes claims 1, 4, and 14 of the '893 patent, explaining particularly how the product is contended to satisfy each of the requirements of those claims. Once we have that chart, we will be in a better position to consider which universe of products the K4T51083QE product would be a representative of, and also suggest representative products for other groups.

We also suggest a similar approach for the RCAT transistors. In this case, we suggest that AMD provide us with a claim chart showing how the RCAT transistors that AMD has seen described in the publicly available literature infringe claims 1, 4, and 14 of the '893 patent, so that we can identify representative products containing RCAT transistors.

III. U.S. Patent No. 4,737,830

Although, as you note, there is a wide variety of possible capacitor layouts in semiconductor products generally, we are hopeful that representative products may be identified for the purposes of this patent. Again, to assist us in making a preliminary identification of such products, please provide us with a claim chart showing how one Samsung product is contended to infringe claim 5 of the '830 patent, particularly pointing out how AMD contends each of the limitations of claims 1 and 5 are satisfied. Once we have that claim chart, we will be in a better position to consider whether there are products representative of groups of products that have the relevant features in common.

IV. U.S. Patent No. 5,545,592

You have asked Samsung to provide evidence that "the process used to manufacture the two exemplar [K4T1G164QA-ZCD5 and K9WAG08U1A] chips is the same, in every material way, as the process used to manufacture Samsung's other DRAM and NAND Flash chips." Again, however, we first need to know from AMD what it considers to be "every material way" in this context. We suggest that you provide us with a claim chart showing how AMD contends the K4T1G164QA-ZCD5 and K9WAG08U1A products infringe claims 1 and 8 of the '592 patent, particularly pointing out how these products are contended to satisfy each of the limitations of those claims. Once we have that chart, we will be in a better position to consider whether there are products representative of groups of Samsung products that have in common the features that AMD believes to be important to its case.

V. U.S. Patent No. 5,623,434 and U.S. Patent No. 5,377,200

It is our understanding from your letter that AMD is asserting these patents against the circuitry of the ARM cores contained in various Samsung products. Accordingly, we are willing to consider providing you with a list of which Samsung products incorporate which of the ARM cores that you have listed. We would also consider agreeing to a representative product containing each pertinent type of ARM core, provided that the parties agree that the '434 and '200 patents are being asserted against circuitry that is solely contained with the ARM core, and not against any circuitry outside of the ARM core. Obviously, if circuitry outside of the ARM core is implicated in any way, it will be much more difficult to agree on representative products.

Finally, with respect to both of these patents, you have stated that an agreement as to representative products containing ARM cores "will not eliminate AMD's need for discovery to determine whether Samsung's proprietary semiconductor parts also practice the . . . patent claims." Unless you have some evidence, however, that any Samsung product not incorporating an ARM core infringes any of the claims of these two patents, we do not believe that you have the necessary basis to pursue an infringement claim against such products, under Rule 11. Obviously, if you do have such evidence, please let us know.

VI. U.S. Patent No. 6,784,879

You have proposed that Samsung identify the groups of televisions, camcorders, and cell phones that incorporate "the same or similar user interface" as the television, camcorder, and cell phone that AMD has identified. In order to do as you propose, however, we need to know what it is about that user interface that AMD believes infringes the '879 patent. Although you have noted the picture-in-picture aspect of certain Samsung televisions, you have not told us what it is about the picture-in-picture feature that allegedly infringes the '879 patent. Furthermore, as camcorders and cell phones generally do not have a picture-in-

picture features, we do not know what it is about the user interfaces of those products that AMD is accusing of infringement.

We propose that AMD provide us with a claim chart showing how the particular television, camcorder, and cell phone identified by AMD are contended to infringe claims 1, 6, 11, 14, 17, and 21 of the '879 patent, particularly pointing out what it is about those products that is contended to infringe each of the limitations of those claims. Once we have that chart, we will be in a better position to consider whether there are groups of products that have the relevant features in common.

* * *

Finally, we note that your letter does not state whether AMD is also interested in identifying representative AMD products accused of infringement by Samsung, in order to limit the discovery that will be required of AMD in this case. Please let us know AMD's position on this point.

Very truly yours,

Christine Saunders Haskett

EXHIBIT C

ROBINS, KAPLAN, MILLER & CIRESI L.L.P.

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ATTORNEYS AT LAW

William H. Manning
612-349-8461

July 10, 2008

VIA FEDERAL EXPRESS

Christine Saunders Haskett, Esq.
Heller Ehrman LLP
333 Bush Street
San Francisco, CA 94104-2878

Re: ***Advanced Micro Devices, Inc., et al. v. Samsung Electronics Co., Ltd., et al.***

Dear Christine:

I write to advance our conversation regarding identifying exemplar Samsung products in order to streamline discovery and trial. I have considered your letter dated June 25, 2008, and believe that AMD can address the concerns you have raised.

As I understand your letter, you have taken the position that for the Cheng '990, Sakamoto '893, Patel '830, Iacoponi '592, and Orr '879 patents, you cannot begin to identify representative Samsung products until AMD provides, for each patent, a claim chart that shows where each claim element is found in an accused product, and the documents that support each chart. We respect your request, and in response I have enclosed with this letter a detailed claim chart for each of those five patents. This detail should allow you to propose an exemplar product for each patent based on the relevant infringing structural and operational features that AMD has identified.

In addition to the claim charts for each patent that you requested, I have also enclosed a set of infringement claim charts based on publicly available information that AMD and its experts have reviewed. This set includes additional infringement claim charts and supporting documents for the five patents mentioned above, as well as charts and supporting documents for the Purcell '434 and Pedneau '200 patents, which you did not request. The charts I have enclosed likely will correspond to the preliminary infringement contentions that AMD will produce to Samsung and the Court on September 30. This set of information should allow you and your client to identify exemplar products for each patent and the other products contained within the groups the exemplars represent. I have enclosed three sets of the charts and supporting documents in both electronic and hard copy for your convenience.

The enclosed charts do not constitute preliminary infringement contentions under the Northern District of California Local Rules, nor do they constitute any kind of discovery

response or any other type of paper or pleading being served in this litigation. Instead, they are informal documents that we are sending for the purpose of identifying product groupings and exemplars. Therefore, AMD will not be bound by these charts and retains the right to change them.

As you can see from the charts and discussion below, it is easily possible to reduce the number of products that will require significant discovery in this case. For example, the number of Samsung products that will require detailed discovery for the Cheng patent should be reduced to 15 to 20 exemplar products. The other six patents will require far fewer exemplar products. The Sakamoto patent should require only one exemplar product, the Patel patent should require only three, and the Iacoponi patent only two. The parties should be able to agree that for the Purcell and Pedneau patents, AMD will need detailed discovery on only exemplar products that contain specific ARM cores—two products for Purcell, and three for Pedneau—along with discovery on agreed-upon exemplars of Samsung proprietary processors. Finally, for the Orr patent, AMD should only need discovery on three exemplar products if Samsung can identify groups of products that employ similar user interfaces. In sum, of the over 15,000 products on the list attached as Exhibit A to Plaintiffs' First Set of Interrogatories, AMD should need detailed infringement discovery for only 40 products.

In order to facilitate mutual cooperation in streamlining this case for discovery and trial, AMD also has taken steps to identify exemplar AMD products that Samsung has accused of infringement. At this point, however, Samsung has given AMD minimal information about Samsung's infringement contention, including what products and structures within those products allegedly infringe which asserted patents. AMD therefore needs Samsung to provide information as AMD has provided with this letter, including infringement claim charts and supporting documentation. AMD can have meaningful conversation about exemplar AMD products only after Samsung provides allegations of infringement that are more detailed than the assertion against "semiconductor devices and/or products incorporating semiconductor devices" in Samsung's Answer and Counterclaims, and a list of "accused products" in Samsung's discovery requests.

The following sections of this letter respond to the patent-specific concerns that you raised in your letter. I believe that this letter and the enclosures provide Samsung more than enough information to identify product groups and representative exemplar products.

I. U.S. Patent No. 5,559,990 (Cheng)

Your letter correctly states that AMD believes that most of Samsung's memory products share the operational and structural characteristics that are relevant to the claims of the Cheng '990 patent. These operational and structural characteristics are clearly understood from the patent claims themselves, which define the scope of the Cheng invention and the characteristics necessary to determine both infringement and exemplar categories. However, to provide greater assistance to Samsung to determine which products are representative of groups of products for purposes of discovery and infringement, I have enclosed as Exhibits B-J detailed infringement charts for claims of the Cheng patent. These infringement charts show from publicly available

information the operational and structural characteristics of Samsung memory products which confirm infringement of the Cheng patent.

Your letter also raised questions regarding AMD estimates for the necessary discovery of approximately 15 to 30 Samsung products for purposes of infringement. The chart enclosed as Exhibit A below will assist Samsung in understanding our reasoning behind these numbers and guide Samsung to denoting certain memory products as representative of a larger group of products. The first column of the chart outlines the nine categories of memory which infringe the Cheng patent, as described in our letter of June 10. For each of these categories, the second column lists our current understanding of the Samsung memory chips, by part number, which fall under this category and for which AMD is entitled to collect damages. Obviously, it is Samsung's burden to verify and supplement this list with any missing products, based upon the product list and interrogatories previously provided to Samsung. The third column lists the publicly available datasheet for that product. Samsung's grouping of multiple products being covered with the same datasheet naturally leads to a grouping of products. The number of groups can be consolidated by noting the similarity of structures and characteristics of Samsung memory products within those groups based upon publicly available documentation.

The fourth column sets forth our suggested discovery groupings based on this consolidation. Discovery on these 38 groups of products should allow AMD to further reduce the number of groupings by approximately a factor of two. This reduction will be made based upon studying the relevant technical documentation for these groupings and ascertaining the similar operational and structural characteristics that are not clearly determinable based upon publicly available documentation alone. The end result will be approximately 15-20 exemplar groups for the Cheng patent. AMD is open to discussions with Samsung engineers to further reduce the number of exemplar groups.

II. U.S. Patent No. 5,248,893 (Sakamoto)

Your letter requests claim charts for Samsung's products containing S-RCAT and RCAT transistors so that Samsung can understand which of its products share the appearance, layering, and composition characteristics that are relevant to infringement of the Sakamoto '893 patent. In particular, Samsung has requested charts for claims 1, 4, and 14. To provide greater assistance to Samsung to determine which products are representative of groups of products for purposes of discovery and infringement, I have enclosed as Exhibit K a detailed claim chart for all claims of the Sakamoto patent that AMD presently intends to assert against Samsung products. This infringement chart shows the operational and structural characteristics of Samsung memory products which indicate infringement of the Sakamoto patent.

The enclosed claim chart contains information about both S-RCAT and RCAT transistors. Based on published Samsung technical papers, we believe that the infringement analysis for the S-RCAT transistors applies equally to Samsung's RCAT technology for all asserted claims of the Sakamoto patent.

III. U.S. Patent No. 4,737,830 (Patel)

Your letter requests claim charts for a representative product that infringes claim 5 of the Patel '830 patent. To provide greater assistance to Samsung to determine which products are representative of groups of products for purposes of discovery and infringement, I have enclosed as Exhibit L a detailed claim chart demonstrating how claims 5 and 6 of the Patel patent, which include the limitations of claim 1, read on Samsung's DRAM memory. In addition, AMD has enclosed as Exhibits M-N claim charts for Samsung NAND and SRAM memory. While capacitor layout can vary, we believe that Samsung follows time-tested industry protocol that includes placing capacitors below power busses in memory devices. We believe that Samsung follows similar design practices for other semiconductor products, including processors. This practice should make it easier for Samsung to group products for purposes of infringement and discovery.

IV. U.S. Patent No. 5,545,592 (Iacoponi)

Samsung requested claim charts that illustrate how Samsung's K4TIGI64QA-ZCD5 and K9WAG08UIA products infringe claims 1 and 8 of the Iacoponi '592 patent. Enclosed as Exhibits O-P are detailed claim charts for the claims of the Iacoponi patent that AMD presently intends to assert against Samsung. These claim charts specifically identify the layers in Samsung's source/drain contacts that correspond to the claim limitations of the Iacoponi patent. We believe that it will be relatively easy for Samsung to establish product groupings based on the use of these process steps across many Samsung product lines.

V. U.S. Patent No. 5,623,434 (Purcell) and U.S. Patent No. 5,377,200 (Pedneau)

You have suggested that Samsung will consider providing a list of products that incorporate the ARM processor cores identified in my June 10, 2008 letter. We believe that such a list will substantially advance the goal of identifying exemplar products that AMD accused of infringing the Purcell and Pedneau patents. We therefore request that Samsung provide that list as soon as possible. I have enclosed as Exhibits Q-R claim charts that demonstrate infringement of Purcell by ARM7TDMI and ARM9TDMI products, and have enclosed as Exhibits S-U claim charts that demonstrate infringement of Pedneau by ARM7EJ-S, ARM9EJ-S, and ARM9E-S products.

You also have suggested that Samsung does not have an obligation to provide discovery regarding Samsung's proprietary processor parts. Case law, however, demonstrates that AMD may obtain discovery on products that are not named specifically in preliminary infringement contentions. *See DR Sys., Inc. v. Fujifilm Med. Sys. USA, Inc.*, No. 06cv417 JLS (NLS), 2008 WL 1734241, at *3 (S.D. Cal. Apr. 10, 2008) (allowing discovery on products not named in infringement contentions); *LG Elecs. Inc. v. Q-lity Computer Inc.*, 211 F.R.D. 360, 368 (N.D. Cal. 2002) (showing that judges do not limit discovery to products named in infringement contentions); *O2 Micro Int'l Ltd. v. Monolithic Power Sys., Inc.*, 467 F.3d 1355, 1366 (Fed. Cir. 2006) ("If a local patent rule required the final identification of infringement and invalidity contentions to occur at the outset of the case, shortly after the pleadings were filed and well

before the end of discovery, it might well conflict with the spirit, if not the letter, of the notice pleading and broad discovery regime created by the Federal Rules."). Samsung makes and sells proprietary processors, including the CalmRISC series, for use in microcontrollers and other small parts that would benefit from using the inventions claimed by Purcell and Pedneau. These parts, like ARM cores, are based on reduced instruction set computing architectures. Therefore, information about these proprietary products is relevant and discoverable.

In order to expedite the process of identifying exemplar products for Samsung's proprietary cores, AMD suggests that Samsung review the enclosed claim charts for Purcell and Pedneau and provide AMD with documentation for the relevant features of the architecture used by Samsung's proprietary processor cores. The parties can then develop an agreement about exemplar products for Samsung's proprietary semiconductor parts.

VI. U.S. Patent No. 6,784,879 (Orr)

I have enclosed as Exhibits V-X claim charts for the television, digital camcorder, and cell phone that I identified in my June 10 letter. The charts show which features of those products infringe the Orr claims. As you have suggested, you now should have the information needed to identify groups of Samsung consumer electronics that use the same or similar user interfaces as these products.

VII. Conclusion

AMD now has responded to all requests you made and issues you raised in your letter on June 25, 2008. The detailed claim charts and supporting documentation enclosed with this letter will give you enough information to propose exemplar products and product groupings. It should easily be possible, if the parties cooperate, to reduce AMD's infringement discovery to a very small subset of the 15,000 products listed in Exhibit A to Plaintiffs' First Set of Interrogatories. That subset may contain only approximately 40 products. Reaching an agreement on these exemplars and the groups they represent will meet your prior request to streamline discovery. When Samsung provides AMD with the same information, in the same level of detail, AMD will unquestionably cooperate to identify exemplar products of its own. We look forward to continuing this discussion.

Sincerely,

ROBINS, KAPLAN, MILLER & CIRESI L.L.P.

William H. Manning

WHM/arf

cc: Robert T. Haslam, Esq., w/o enclosures (*via email only*)
Michael K. Plimack, Esq., w/o enclosures (*via email only*)
Alan H. Blankenheimer, Esq., w/o enclsoures (*via email only*)

Enclosures:

Banker's boxes, each containing claim charts and supporting documents for all seven patents, and CDs containing the same materials.

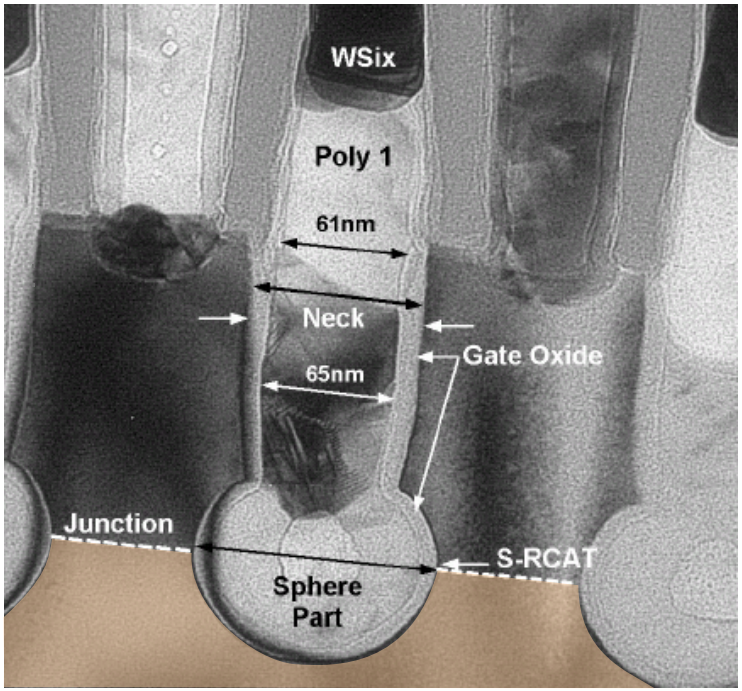
EXHIBIT D

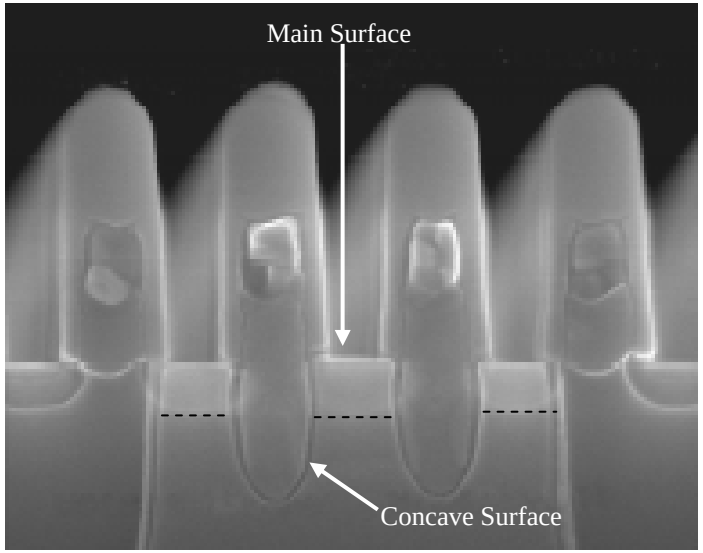
***Advanced Micro Devices, Inc., et al. v. Samsung Electronics Co., Ltd., et al.*, Case No. CV-08-0986-SI**
Exhibit K – Sakamoto 5,248,893 – DRAM Infringement Chart

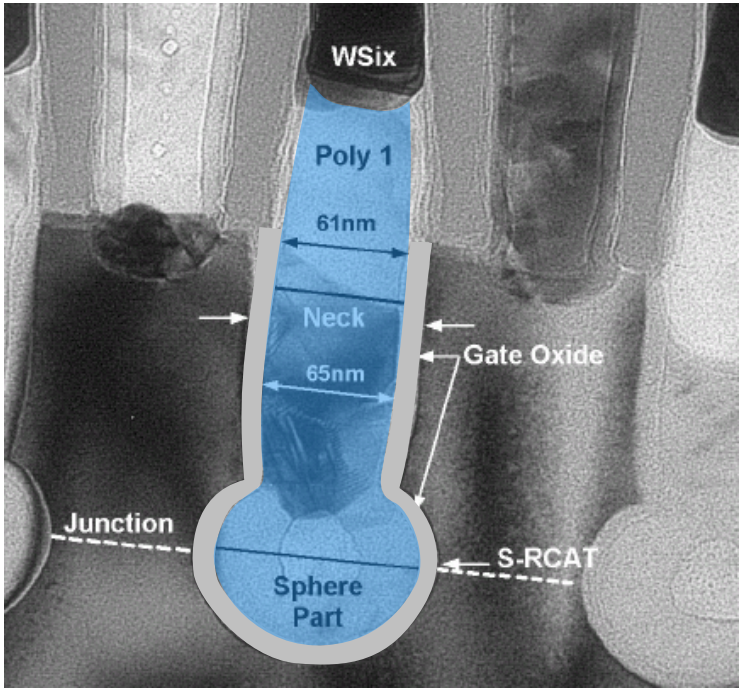
The following sets forth the manner in which the Defendants' (collectively referred to as "Samsung") DRAM products infringe U.S. Patent No. 5,248,893. Plaintiffs allege that all elements are present literally, but reserve the right to allege that any particular element is present by equivalents if Samsung establishes that the element is not present literally.

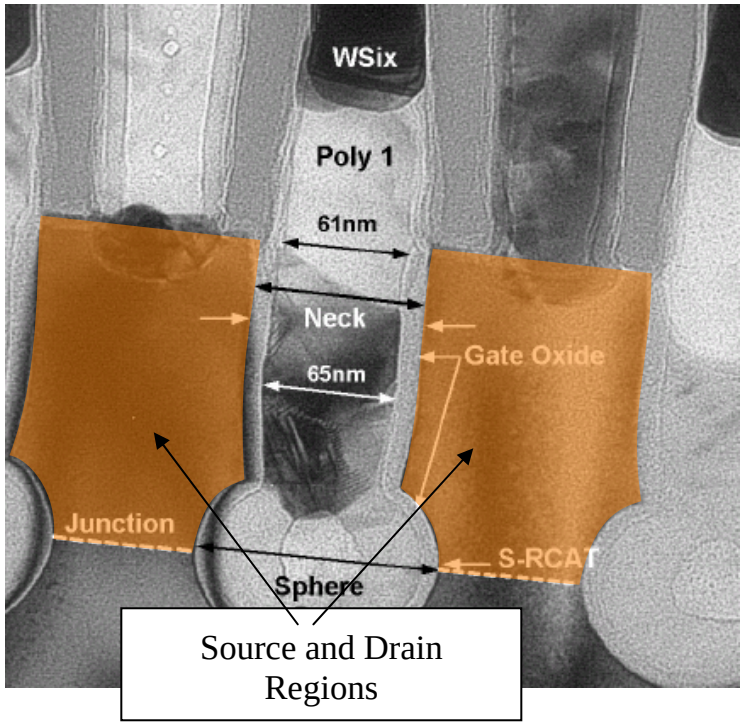
Claim	Claim Element Text	Infringement Support
1	An insulated gate field effect device comprising:	Samsung's DRAMs include insulated gate field effect transistors as set forth below.
1(a)	a first conductivity type semiconductor substrate having a main surface;	Samsung's DRAMs include a semiconductor substrate of a first conductivity type. The substrate has a main surface. This is shown in the figure below, which consists of a TEM image of a cross section of a transistor from an exemplar Samsung DRAM (K4T51083QE).[1] This figure shows the presence of a semiconductor substrate. The area below the dotted line labeled "Junction" has a first conductivity type. The area of the main surface is labeled on the TEM image.

[1] Plaintiffs' contentions are not limited to the exemplar Samsung DRAM chips depicted herein. Those depictions are for illustrative purposes only. Plaintiffs contend that Samsung's DRAM chips generally infringe, but are unable to identify the precise models without further discovery.

Claim	Claim Element Text	Infringement Support
		 The TEM set forth above is from a cross section of a Samsung S-RCAT design. AMD's contentions are not limited to Samsung's DRAMs containing S-RCATs. Samsung's DRAMs containing RCATs also meet this claim element. As set forth in the cross-section SEM image depicted below (taken from Kim et al., Technology for sub-50nm DRAM and NAND Flash Memory, (2005)), those products have a substrate with a main surface (see area labeled "main surface"). The area below the dotted line would be of a first conductivity type.

Claim	Claim Element Text	Infringement Support
		
1(b)	said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main surface;	The semiconductor substrate in Samsung's DRAMs have a concave (i.e., recessed below the main surface) surface that extends from the main surface to a predetermined depth below the surface. This feature is illustrated in the two images reproduced above (see areas labeled "Concave Surface").
1(c)	an insulating film formed on said concave surface;	Samsung's DRAMs include an insulating layer on the concave surface portion. The S-RCAT TEM image set forth above shows the insulating layer in the concave area (see area labeled "Gate Oxide").
1(d)	a conductive gate electrode formed above said insulating film, overlying	Samsung's DRAMs include a conductive gate electrode formed above the insulating film, overlying the concave surface. This is illustrated in the S-RCAT TEM, which is reproduced below with relevant labels (see area labeled "Gate".)

Claim	Claim Element Text	Infringement Support
	the concave surface;	The location of this gate shows that it is above the insulating film and overlies the concave surface. 
1(e)	first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surfaces, self	Samsung's DRAMs have first and second impurity regions. They appear in the S-RCAT TEM reproduced below, in the area labeled "Source and Drain Regions." They are formed in the substrate, and are in the vicinity of the main surface because they extend up to the main surface. They are on either sides of the gate and are self-aligned to the gate because two separate masks are not needed to align the gate and the edges of source/drain regions. This is confirmed by the following

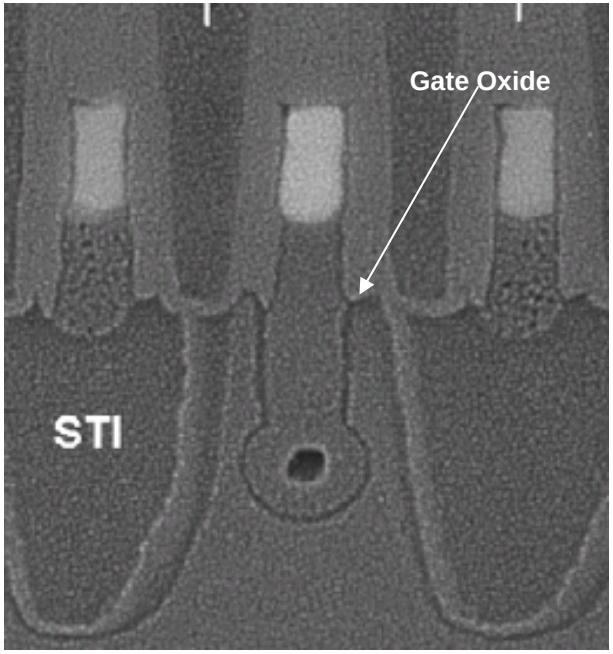
Claim	Claim Element Text	Infringement Support
	aligned to and positioned at one side and the other side of said gate electrode respectively; and	publications: J.Y. Kim et al, S-RCAT (Sphere-shaped-Recess-Channel-Array Transistor) Technology for 70nm DRAM Feature Size and Beyond, 2005 Symposium on VLSI Technology Digest of Technical Papers; and H.J. Oh et al., High-Density Low-Power-Operating DRAM Device Adopting $6F^2$ Cell Scheme with Novel S-RCAT Structure on 80nm Feature Size and Beyond, Proceedings of ESSDERC, Grenoble, France (2005). These publications describe the process for fabricating S-RCAT transistors. 
1(f)	A first conductivity type region located in said	In Samsung's DRAMs, there is a first conductivity type region in the substrate (i.e. the area below the "Junction" in the S-RCAT TEM reproduced above). It is

Claim	Claim Element Text	Infringement Support
	semiconductor substrate between said first and second impurity regions for defining a channel region and a channel-free region extending conformably under and along said concave surface	between the source and drain regions because it extends from one to the other. The channel region and the channel free region forms in the first impurity region under and along the gate oxide that extends under the portion of the gate labeled "Sphere Part" in the TEM reproduced above.
1(g)	wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and	It is readily apparent in the S-RCAT TEM reproduced above that depth of the concave surface is between one and two times the depth of the source/drain.
1(h)	wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not	In Samsung's DRAMs, the concave surface is continuously curved in the area just below the area labeled "junction" in the S-RCAT TEM depicted above, which is where the first and second impurity regions (i.e. the source/drain regions) exist. By virtue of this shape, the depletion region formed around the gate and the depletion regions formed around the impurity regions would merge together in a smooth way. As a result, excessive field concentration would not develop in the area of merger.

Claim	Claim Element Text	Infringement Support
	develop in the vicinity where the first and second depletion regions meet	
2	An insulated gate field effect device according to claim 1, wherein one of said first and second impurity regions constitutes a drain-region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region and the drain region and the conforming second depletion region formed in the vicinity of the gate	The source/drain regions are identified in response to section 1(e) above. One of the two functions as the source and the other as the drain. As is evident from the image of the cross section set forth in that section, the lower portion of the concave surface is continuously curved at least in the vicinity of the drain. This is also in the vicinity of the area where the channel free region develops during the off state of the device. A transistor shaped and configured in this fashion would cause depletion regions to develop with a smooth merger of two depletion regions (the one that develops in the vicinity of the channel-free region and drain and the one that forms in the vicinity of the gate electrode). Accordingly, excessive field concentration would not develop in the vicinity of the channel-free region.

Claim	Claim Element Text	Infringement Support
	electrode so that excessive field concentration will not develop in the vicinity of the channel-free region.	
3	An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulting film comprises an oxide film.	The transistors in Samsung's DRAMs are MOS transistors because they are comprised of a conductive electrode (i.e. polysilicon), oxide, and semiconductor. The insulating film (area labeled "gate oxide" in the figure reproduced in Section 1(a) above) is an oxide film.
4	An insulated gate field effect transistor comprising:	Samsung's DRAMs include insulated gate field effect transistors as set forth below.
4(a)	a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;	Samsung's DRAMS include a semiconductor substrate, a portion of which has a substantially planar (flat) main surface, and another portion of which has a concave (i.e., recessed below the main surface) surface that extends continuously from the main surface to a predetermined depth below the surface. This is shown in the TEM image of the exemplar Samsung S-RCAT reproduced in Section 1(a) above. This figure shows the presence of a semiconductor substrate (see area labeled "Substrate") with a substantially planar main surface (see area labeled "Main Surface"). A portion of the substrate has a concave surface (see area labeled "Concave Surface.") As is illustrated in the figure, the concave surface extends down without interruption into the substrate, to a predetermined depth.

Claim	Claim Element Text	Infringement Support
		Samsung's DRAMS containing RCATs also meet this claim element. The RCAT cross-section SEM image reproduced in Section 1(a) above shows that those products have a substrate with a substantially planar main surface (see area labeled "main surface"), and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface (see area labeled "concave surface.")
4(b)	an insulating layer conformably disposed on the main surface and the concave surface portion;	Samsung's DRAMs include an insulating layer on the substantially flat main surface, as well as the concave surface portion. The S-RCAT TEM image set forth in Section 1(a) above shows the insulating layer in the concave area (see area labeled "Gate Oxide"). In addition, the SEM image set out below, taken from the same S-RCAT exemplar product, confirms the presence of the insulating layer conformably disposed on the main surface (see area labeled "Gate Oxide.")

Claim	Claim Element Text	Infringement Support
		
4(c)	a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;	Samsung's DRAMs include a gate on the insulating layer over the concave surface. This is illustrated in the S-RCAT TEM (see area labeled "Gate" in Section 1(d) above). The location of this gate shows that it overlies the concave surface portion, and has two opposed sides, located to the left and the right of this figure.

Claim	Claim Element Text	Infringement Support
4(d)	implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and	The transistors in Samsung's DRAMs include source and drain regions located within the substrate, adjacent to the opposed sides of the gate. This is illustrated in the S-RCAT TEM reproduced in Section 1(e) above with relevant labeling (see area labeled "Source and Drain Regions)." These source/drain regions are self-aligned because two separate masks are not needed to align the gate and the edges of source/drain regions. This is confirmed by the publications cited in Section 1(e) above, which describe the process for fabricating S-RCAT Transistors.
4(e)	a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;	The transistors in the Samsung's DRAMs formed in accordance with the elements above will necessarily have a channel-region along the bottom of the area labeled "sphere part" running between the source and drain. This channel-region necessarily conducts current between the source and drain regions when the transistor is in a turned-on state. Otherwise, the transistor could not work.
4(f)	wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor	The transistors in Samsung's DRAMs formed in accordance with the elements above will necessarily have a channel-free zone that develops in the substrate, at the bottom of the area labeled "sphere part" running between the source and drain, when the transistor is in a turned-off state. Otherwise, the transistor would not work.

Claim	Claim Element Text	Infringement Support
	is in a turned-off state; and	
4(g)	wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.	The transistors in Samsung's DRAMs include a gate and concave surface portion that are curved at the bottom, as is illustrated in the TEMS set forth above. This curvature is in the vicinity of the channel-free zone because the channel-free zone is just below the gate and concave surface. As a result of the curved shape of the surface portion at the bottom of the gate, a smoothly-curved depletion zone boundary develops near the channel-free zone when the transistor is in a turned-off state.
5	An insulated-gate field effect transistor according to claim 4 wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate surface.	Because the bottom of the gate in Samsung's S-RCATs is spherical (see area labeled "Sphere Part" in the S-RCAT TEMs depicted above), the concave surface portion is curved in a transverse cross-sectional plane, where such plane extends through the transistor between but not intersecting the first and second sides of the gate. This shape would provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate surface.

Claim	Claim Element Text	Infringement Support
6	An insulated-gate field effect transistor according to claim 5 wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface.	Because the lower portion of the gate in Samsung's S-RCAT transistors is spherical, it is curved in the relevant portion (i.e. in such a way that it provides an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface.) Further, because it is spherical, the curvature exists both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane. As is plainly evident from the TEM reproduced above, the concave surface portion extends between and joins the first and second sides of the gate.
7	An insulated-gate field effect transistor according to claim 6 wherein the concave surface portion is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness	Because the lower portion of the gate in Samsung's S-RCAT transistors is spherical, it is equally curved in two planes (the transverse cross-sectional plane and in the non-transverse cross-sectional plane). This curvature exists in the relevant portion, because it would result in a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a turned-off state.

Claim	Claim Element Text	Infringement Support
	and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a turned-off state.	
11	An insulated-gate field effect transistor according to claim 4 wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions.	As is plainly evident from the TEMs set forth above, the transistor formed in Samsung's DRAMs infringe dependent Claim 11 because the depth of the concave surface portion (running from the main surface to the bottom of the "Sphere Part") is more than one but less than two times the depth of the source/drain regions. The source/drain regions extend from the main surface level only as deep as the line labeled "Junction" in the S-RCAT TEM images set forth above.

EXHIBIT E

ROBINS, KAPLAN, MILLER & CIRESI L.L.P.

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ATTORNEYS AT LAW

Cole M. Fauver
612-349-0948

July 30, 2008

U.S. MAIL & E-MAIL

Christine Saunders Haskett
Heller Ehrman LLP
333 Bush Street
San Francisco, CA 94104

Re: *Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al.*
3:08-CV-0986
Our File No.: 124318-0010

Dear Christine:

I write to follow up on the issues raised in our July 10, 2008 letter to you, particularly regarding Samsung's patent infringement allegations against AMD and ATI.

Samsung Electronics Company's ("SEC") counterclaims of infringement assert 6 different patents, which contain 120 separate claims. The counterclaims do not identify any specific accused products at all. SEC only alleges that these patents are infringed by, "among other things, semiconductor devices and/or products incorporating semiconductor devices." See, for example, paragraphs 82, 88, 93, 98, 105, and 111 of SEC's counterclaims. Even under the relatively liberal standards of notice pleading, the counterclaims do not fairly apprise AMD of the basis for the allegations. The allegations of induced and contributory infringement are similarly deficient.

Under the Federal Rules, a pleading is defective if it possesses insufficient facts to support a cognizable legal claim. *Robertson v. Dean Witter Reynolds, Inc.*, 749 F.2d 530, 534 (9th Cir. 1984). In patent litigation, one must do more than simply allege a bare statement of direct and indirect infringement within a counterclaim to demonstrate a plausible entitlement to relief. *AntiCancer, Inc. v. Xenogen Corp. et al.*, 248 F.R.D. 278, 281 (S.D. Cal. 2007) (applying Supreme Court law and finding that, to comply with F. R. Civ. P. 8, pleadings must express a "plausible entitlement to relief."). SEC has failed to meet these basic standards.

This creates an immediate problem with respect to discovery. While your discovery requests name over 30 different "series" of processors and chipsets, there is no correlation between this list and the asserted patents. For example, document request 76 asks for all

documents relating to the design, conception, research, development, reduction to practice, and manufacturing and testing of each AMD Accused Product and Process. As it stands, this request would encompass all documents relating to every feature of each of the several individual products within the broad series you have named. Document requests 75, 77 and 79 similarly would call for virtually all documents on every feature of all products. However, most of the six patents SEC has asserted against AMD are directed to fabrication methods, not to product design or product features. There is nothing that fairly limits your requests to the product features called out in the few apparatus claims in suit. There is also nothing that narrows the requests directed to fabrication processes. For example, SEC provides no indication of which aspect of which process used to manufacture which product potentially relates to which patent. These examples are selected for illustrative purposes; the same fundamental problem exists with many other document requests as well as Samsung's interrogatories.

As such, the discovery requests are improperly overbroad and should be substantially narrowed. However, because we are committed to producing documents to you on October 15, we raise this objection now, and also repeat our request of July 10 that you provide detailed information about SEC's infringement contentions. We will use this information to try to identify exemplar "accused products" to streamline both discovery and trial proofs. We gave you such detailed information on AMD's infringement contentions over two weeks ago. We will need the information on SEC's contentions from you soon, however, to meet the October 15 date. You must have this information readily available because the federal rules mandate that a party have conducted an adequate investigation before asserting a patent. In the context of patent infringement claims, this requires, at a minimum, a comparison between the allegedly infringing article and an asserted claim to determine if each claim limitation is met.

I look forward to your prompt response.

Sincerely,

ROBINS, KAPLAN, MILLER & CIRESI L.L.P.

Cole M. Fauver

CMF/ll

cc: Robert T. Haslam (via e-mail)
Michael K. Plimack (via e-mail)
Alan H. Blankenheimer (via e-mail)

cc: William H. Manning

EXHIBIT F

US005559990A

United States Patent [19]

Cheng et al.

[11] **Patent Number: 5,559,990**

[45] **Date of Patent: Sep. 24, 1996**

[54] **MEMORIES WITH BURST MODE ACCESS**

[75] Inventors: **Pearl P. Cheng**, Cupertino; **Michael S. Briner**; **James C. Yu**, both of San Jose, all of Calif.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **328,337**

[22] Filed: **Oct. 24, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 836,667, Feb. 14, 1992, abandoned.

[51] **Int. Cl.**[6] **G06F 12/00**

[52] **U.S. Cl.** **395/484**; 395/421.07; 395/405; 364/DIG. 1; 365/230.04; 365/230.08

[58] **Field of Search** 395/425, 500, 395/484, 405, 421.07, 401, 481; 365/230, 230.04, 230.08, 238.5

[56] **References Cited**

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John F. Wakerly, *Digital Design: Principles and Practices* (Prentice–Hall, 1990), pp. 123, 126–127, 246–254 and 567–568.

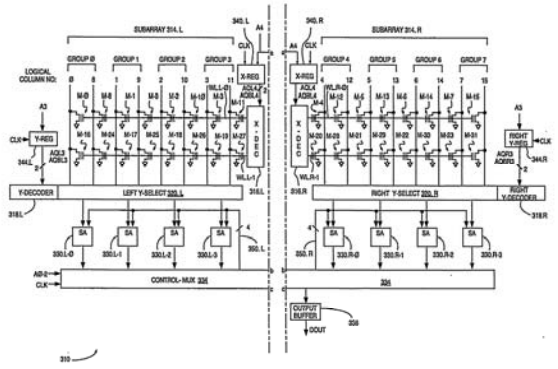
Primary Examiner—Rebecca L. Rudolph

Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel; Michael Shenker

[57] **ABSTRACT**

To provide a boundaryless burst mode access, a memory array is divided into two or more subarrays. Each subarray has its own row and column decoders. The columns of each subarray are divided into groups. A sense amplifier circuit is provided for each group of columns. The column decoder of each subarray selects simultaneously one column from each group so that the memory locations in one row in the selected columns have consecutive addresses. The memory locations in the selected row and columns are read by the sense amplifier circuits. While the contents of the sense amplifier circuits of one subarray are transferred one by one to the memory output, consecutive memory locations of another subarray are read to the sense amplifier circuits. In some embodiments, to save power, sense amplifier circuits are disabled when their outputs are not transferred to the memory output.

23 Claims, 37 Drawing Sheets



Cheng

U.S. Patent No. 5,559,990

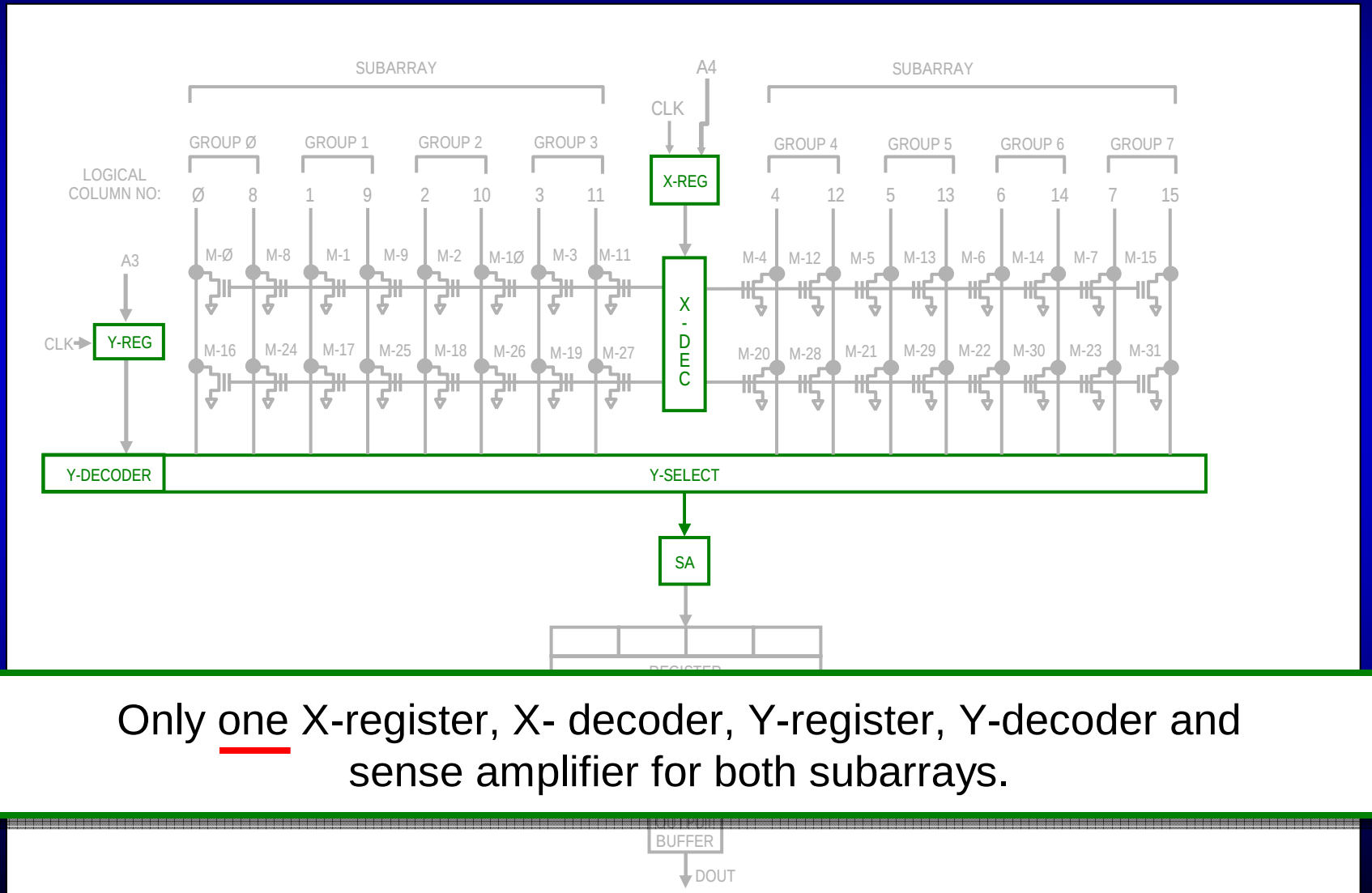
Cheng: '990 Patent

Statement of the Invention

The invention is a memory with dedicated circuitry for each of its subarrays that maximizes the performance of memory by providing for continuous burst mode reads and selective deactivation of sense amplifiers.

Cheng: ’990 Patent

Prior Art: Shared Circuitry for Subarrays



Only one X-register, X- decoder, Y-register, Y-decoder and sense amplifier for both subarrays.

Cheng: '990 Patent
Dedicated Circuitry for Each Subarray

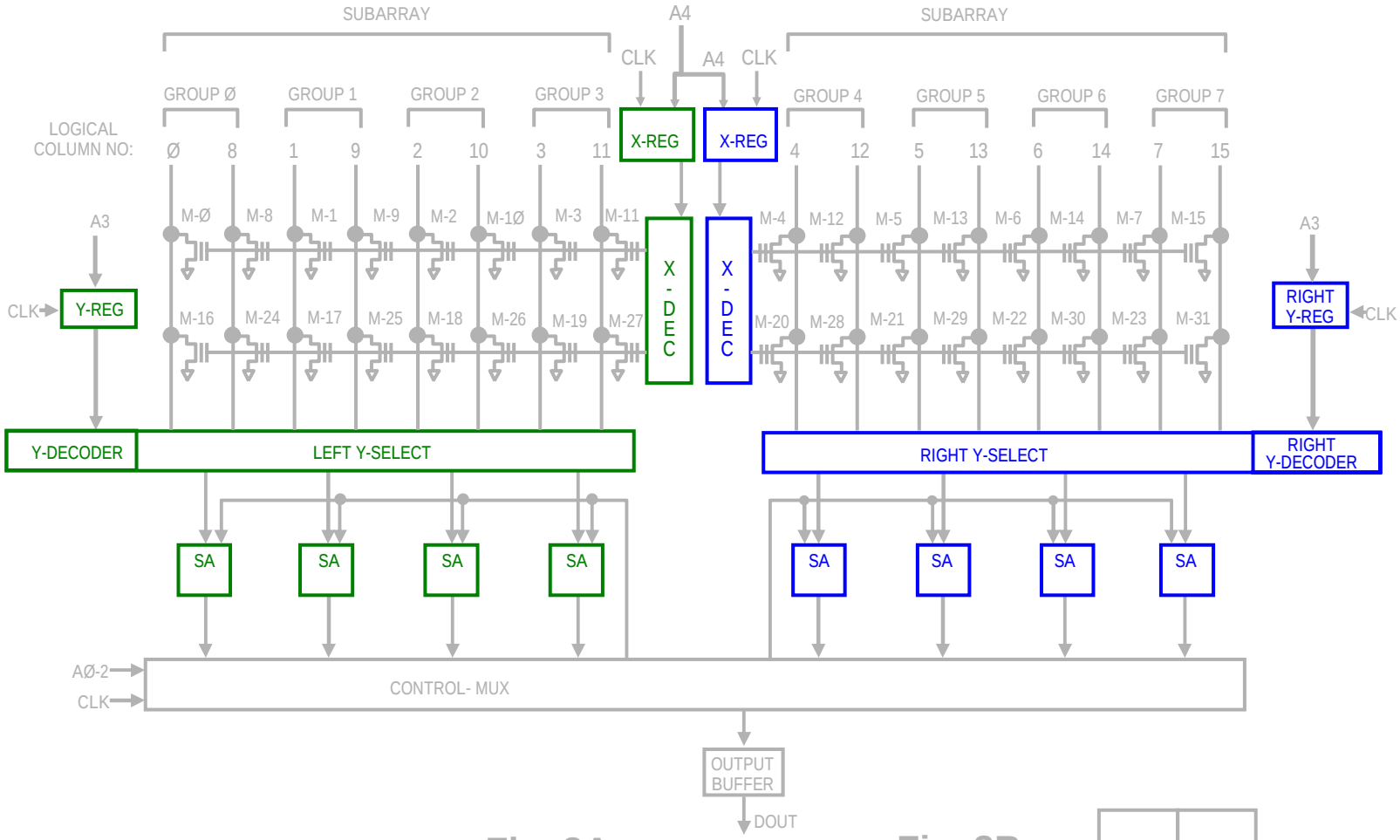
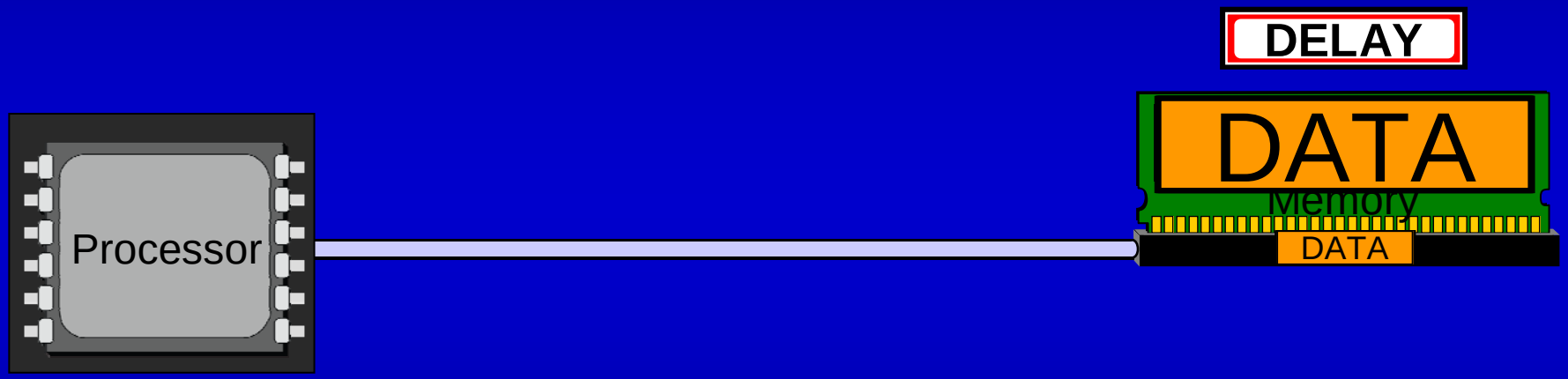


Fig. 3A Fig. 3B

Memory Access: Burst Mode Access



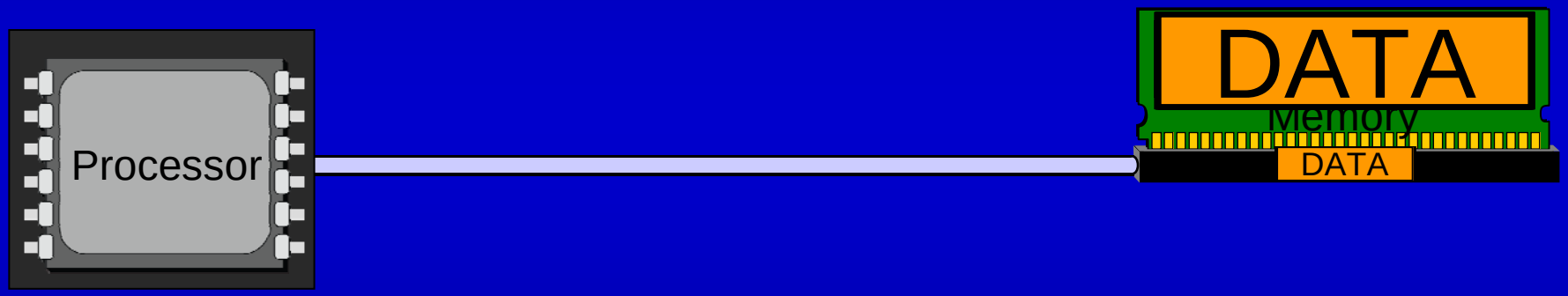
Request

DATA DATA DATA DATA

Request

DATA DATA DATA DATA

Continuous Burst Mode



Request

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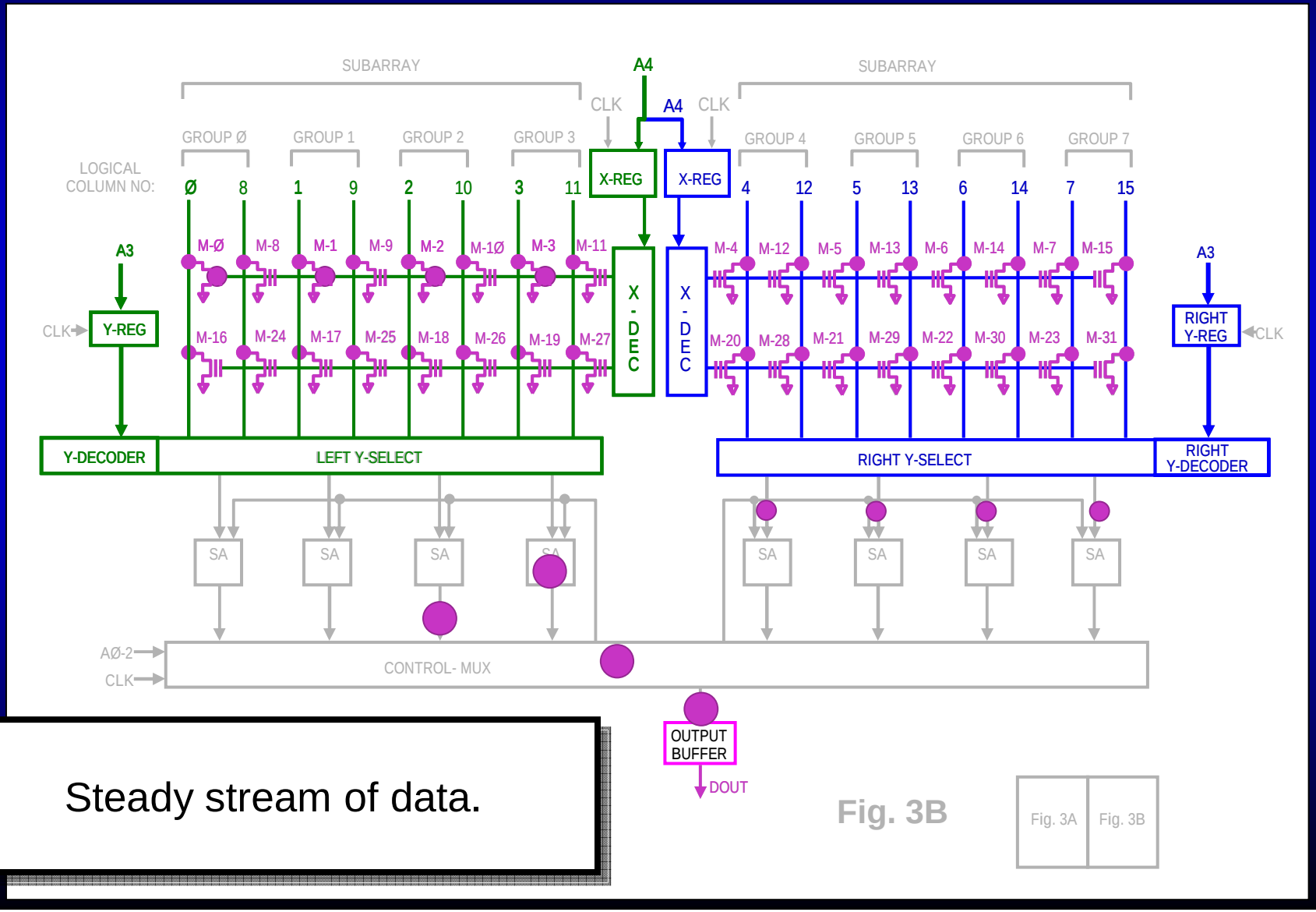
Cheng: '990 Patent
Continuous Burst Mode



Steady stream of data.

Fig. 3B

Fig. 3A | Fig. 3B

Cheng: '990 Patent
Sense Amplifier Deactivation

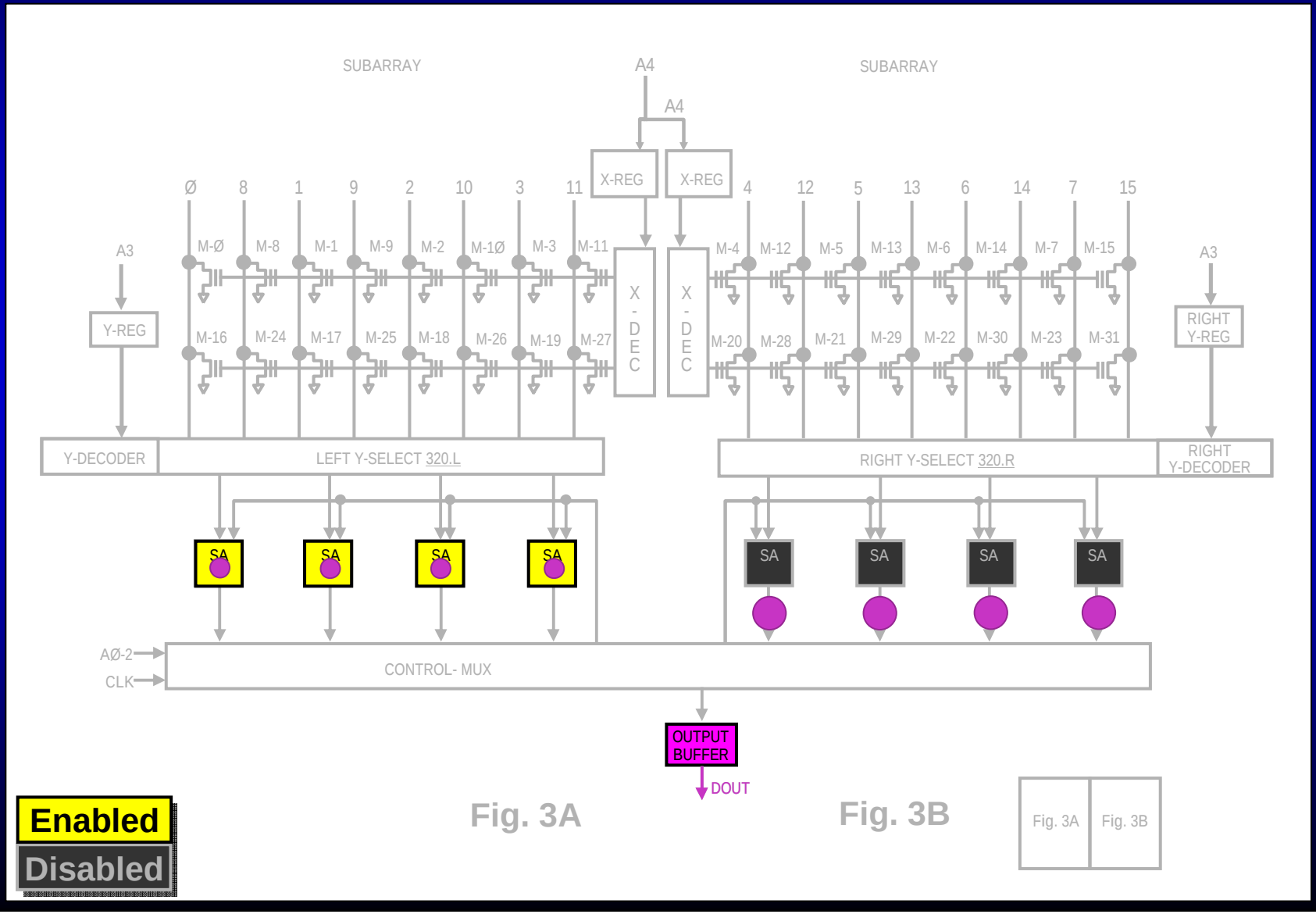


EXHIBIT G

US005248893A

United States Patent [19]

Sakamoto

[11] **Patent Number: 5,248,893**

[45] **Date of Patent: Sep. 28, 1993**

[54] **INSULATED GATE FIELD EFFECT DEVICE WITH A SMOOTHLY CURVED DEPLETION BOUNDARY IN THE VICINITY OF THE CHANNEL-FREE ZONE**

[75] Inventor: **Shinichi Sakamoto**, Atsugi, Japan

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **593**

[22] Filed: **Jan. 5, 1993**

Related U.S. Application Data

[63] Continuation of Ser. No. 660,522, Feb. 25, 1991, abandoned.

[30] **Foreign Application Priority Data**

Feb. 26, 1990 [JP] Japan 2-47100

[51] **Int. Cl.**[5] **H01L 29/76**; H01L 29/94

[52] **U.S. Cl.** **257/409**; 257/288

[58] **Field of Search** 357/23.1, 23.11, 55; 257/288, 409

[56] **References Cited**

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58-202560	11/1983	Japan	357/23.1
60-214570	10/1985	Japan	357/23.1
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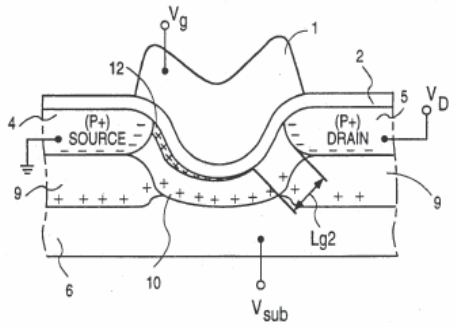
Primary Examiner—Rolf Hille
Assistant Examiner—Steven Loke
Attorney, Agent, or Firm—Fliesler, Dubb, Meyer & Lovejoy

[57] **ABSTRACT**

An apparatus and method for forming an insulated gate field effect device including a first conductivity-type semiconductor substrate having a concave with a curved surface formed on the main surface, an insulating film formed on the major surface including the concave, a first and second impurity regions of a second conductivity-type formed in the vicinity of the main surface at one side and the other side of the concave, respectively, and a conductive layer formed on the channel region which is formed along the concave between the first and second impurity regions with the insulating film interposed therebetween. The method includes forming a concave with the curve surface on the main surface of a semiconductor substrate; forming an insulating film on the main surface, forming a conductive layer above the concave with an insulating film interposed therebetween; forming a first and second impurity regions of a second conductivity type in the vicinity of the main surface at one side and the other side of the concave.

14 Claims, 5 Drawing Sheets



Sakamoto

U.S. Patent No. 5,248,893

Sakamoto: '893 Patent

The Goal: Smaller Transistors

Designers seek to make smaller transistors. When they shrink them, the distance between the source and the drain shrinks, and so does the channel and the channel-free length.

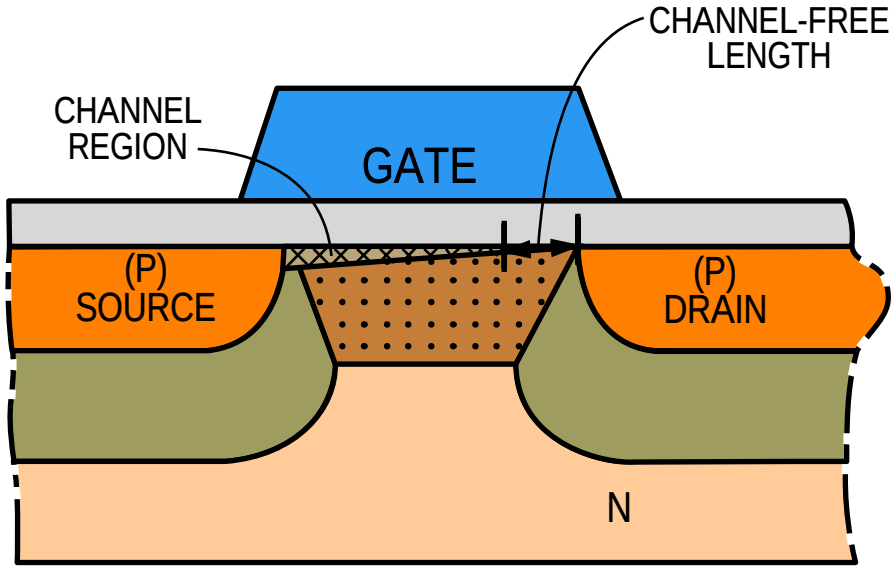


FIG. 9
PRIOR ART

Sakamoto: '893 Patent

The Goal: Smaller Transistors

When the channel-free length gets too small:

1) current can flow when it should not;

2) current can escape from the channel region into other parts of the transistor. This causes the transistor to degrade to the point that it stops functioning.

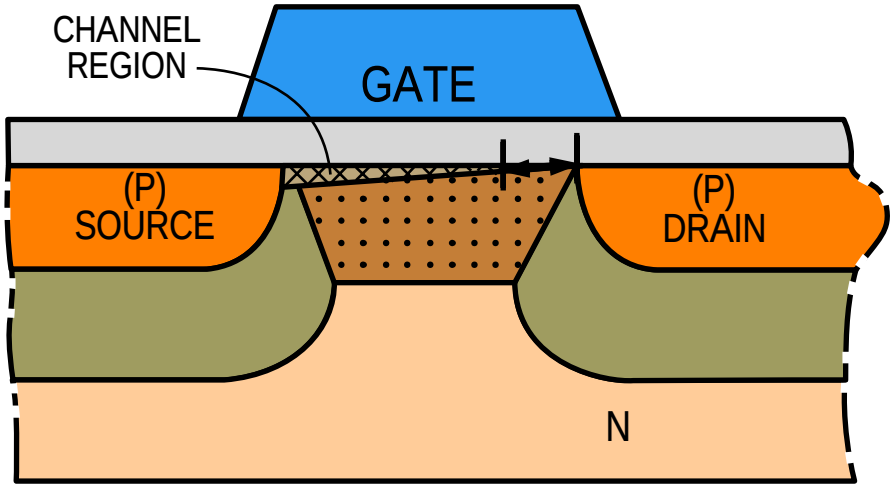


FIG. 9
PRIOR ART

Sakamoto: '893 Patent
Invention

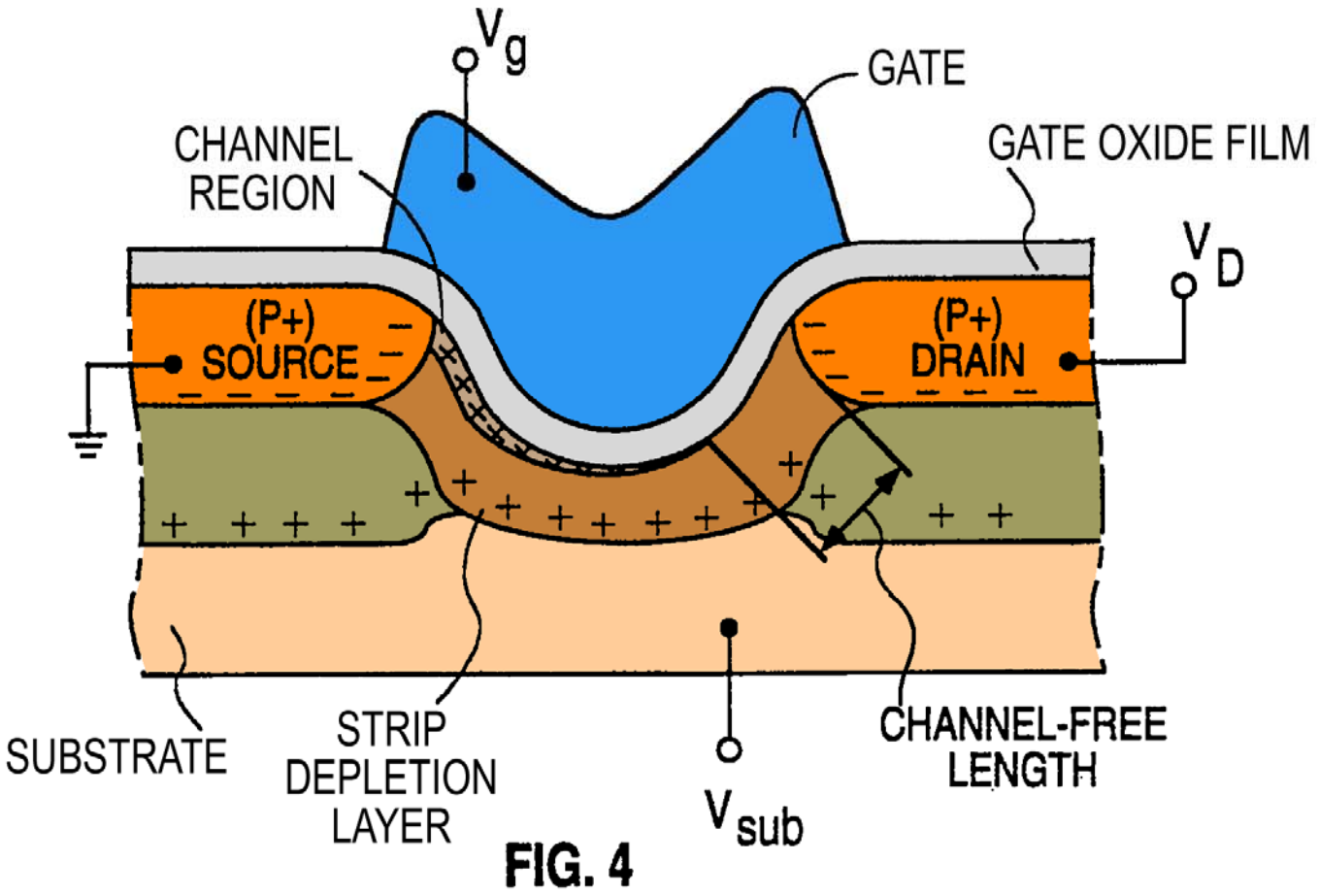
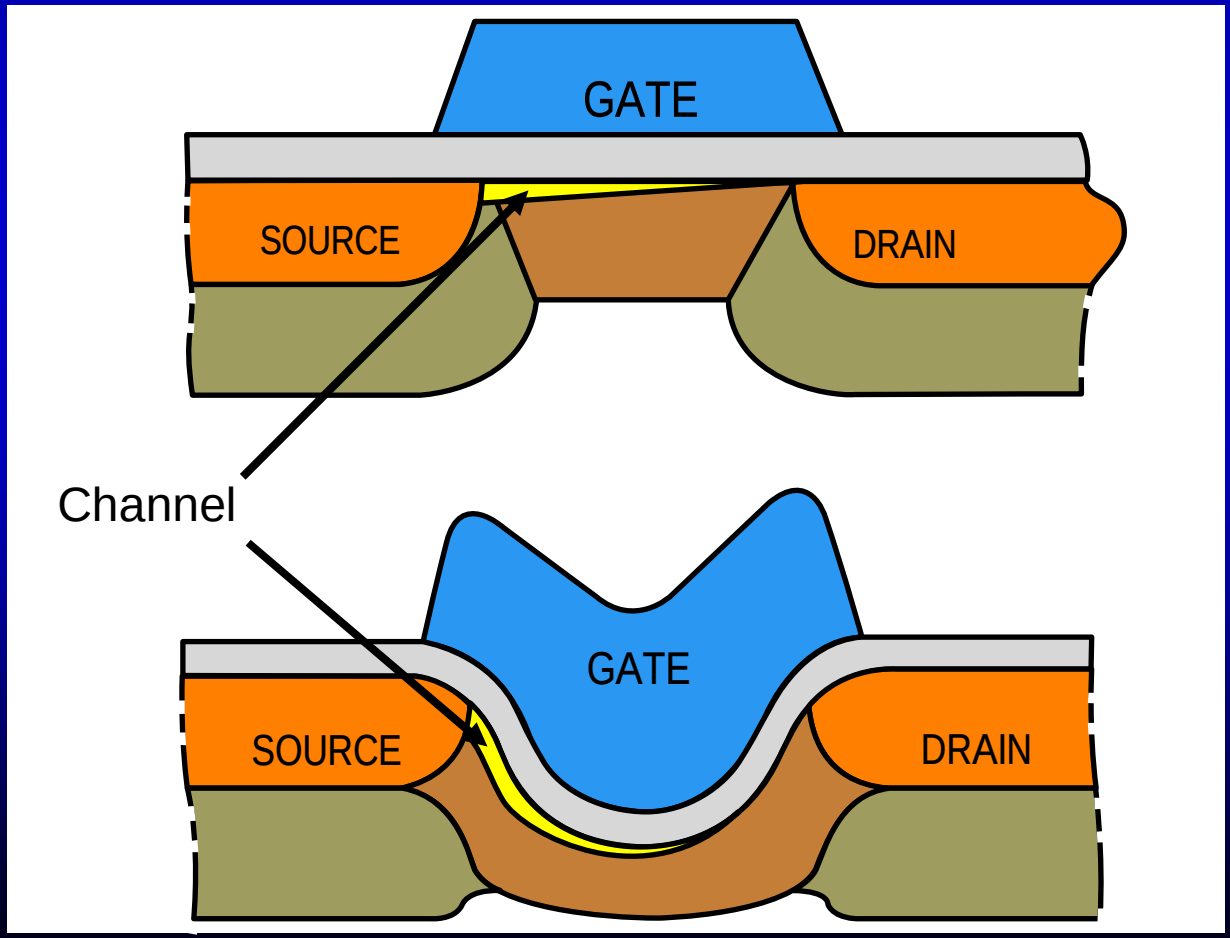


FIG. 4

Sakamoto: '893 Patent

Using a curved, recessed gate to create a longer channel without increasing the size of the transistor.



Prior Art

Invention

EXHIBIT H

United States Patent [19]
Patel et al.

[11] **Patent Number: 4,737,830**
[45] **Date of Patent: Apr. 12, 1988**

[54] **INTEGRATED CIRCUIT STRUCTURE HAVING COMPENSATING MEANS FOR SELF-INDUCTANCE EFFECTS**

[75] Inventors: **Bharat D. Patel**, San Jose; **Stephen Y. Tam**, San Francisco; **Pravin R. Shah**, Sunnyvale, all of Calif.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **817,227**

[22] Filed: **Jan. 8, 1986**

[51] **Int. Cl.**[4] **H01L 29/78**
[52] **U.S. Cl.** **357/23.6**; 357/41; 357/45; 357/46; 357/51; 357/68
[58] **Field of Search** 357/23.6, 51, 41, 45, 357/46, 68

[56] **References Cited**
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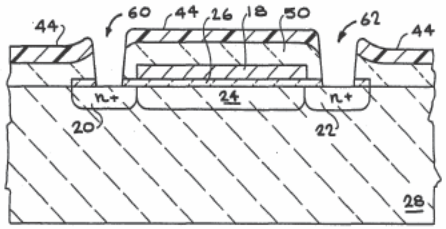
4,516,312 5/1985 Tomita 357/23.6
4,536,941 8/1985 Kuo et al. 357/23.6

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Patrick T. King; John P. Taylor; J. Vincent Tortolano

[57] **ABSTRACT**

An improved integrated circuit structure is disclosed which comprises a Vcc bus and a Vss bus having capacitance means coupled between the busses and distributed along the length of the busses to reduce the voltage spikes induced during switching. In a preferred embodiment, the capacitance means comprise one or more capacitors formed beneath one of the busses. Construction of MOS capacitors beneath one or more of the busses is disclosed.

6 Claims, 11 Drawing Sheets

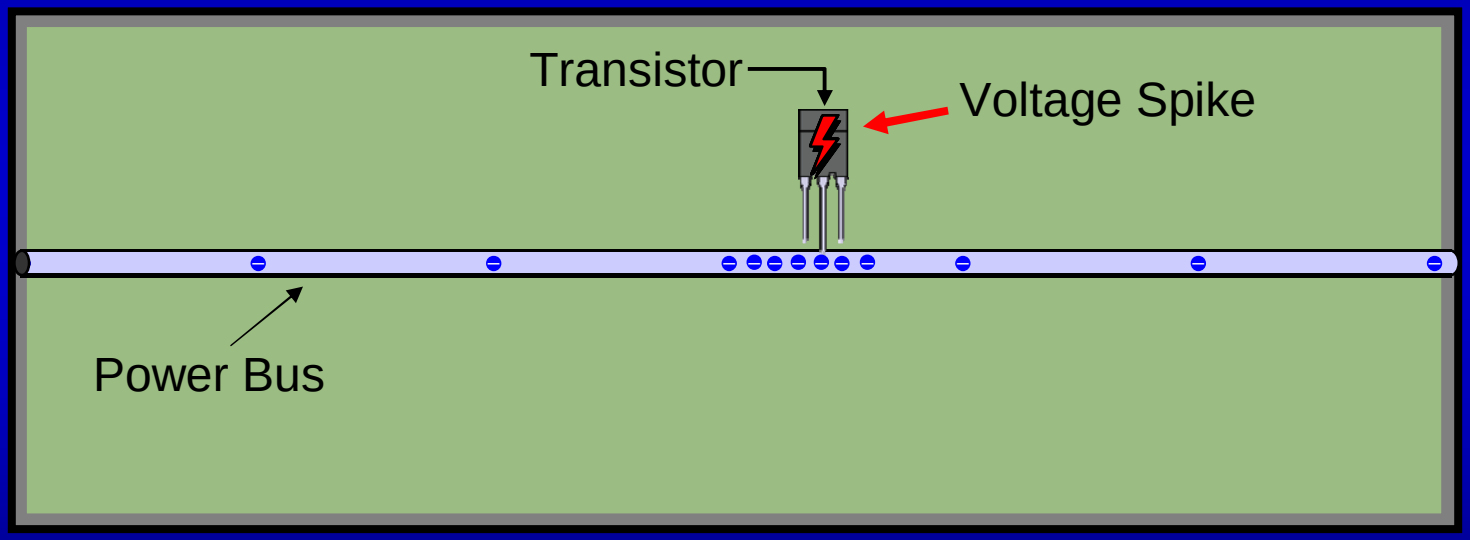


Patel

U.S. Patent No. 4,737,830

Patel: '830 Patent

Voltage Spikes Damaged Transistors Attached to Power Bus



Patel: '830 Patent

Statement of the Invention

Adding capacitance underneath the busses to reduce voltage spikes. The gate area of the capacitor is segmented, with each segment having a connection to the bus to improve efficiency and reliability.

Patel: '830 Patent
Invention

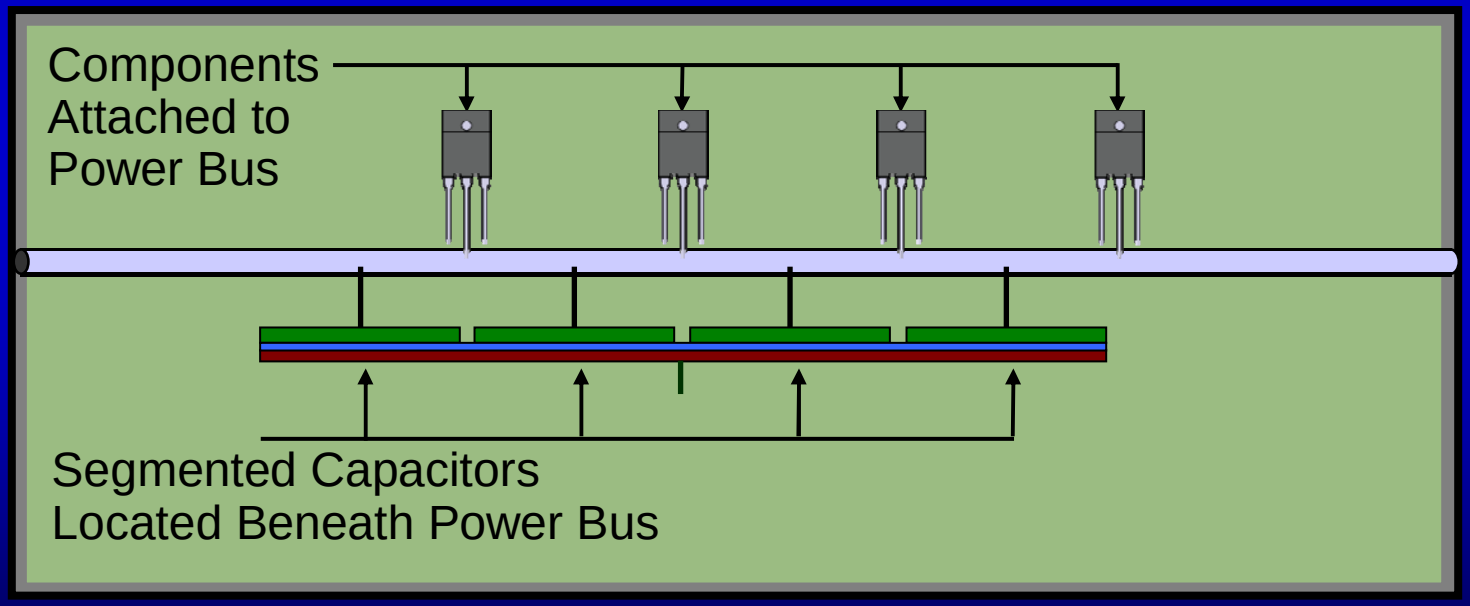


EXHIBIT I

US005545592A

United States Patent [19]

Iacoponi

[11] **Patent Number: 5,545,592**

[45] **Date of Patent: Aug. 13, 1996**

[54] **NITROGEN TREATMENT FOR METAL-SILICIDE CONTACT**

[75] Inventor: **John A. Iacoponi**, San Jose, Calif.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **393,635**

[22] Filed: **Feb. 24, 1995**

[51] **Int. Cl.**[6] **H01L 21/28**

[52] **U.S. Cl.** **437/200**; 437/192

[58] **Field of Search** 437/200, 201, 437/192, 190; 257/757, 764, 768

[56] **References Cited**

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S.W. Sun et al., "Al/W/TiN$_x$/TiSi$_x$/Si Barrier Technolgy for 1.0–μm Contacts," IEEE Electron Device Letters, Feb. 1988, vol. 9, No. 2, pp. 71–73.

Primary Examiner—George Pourson

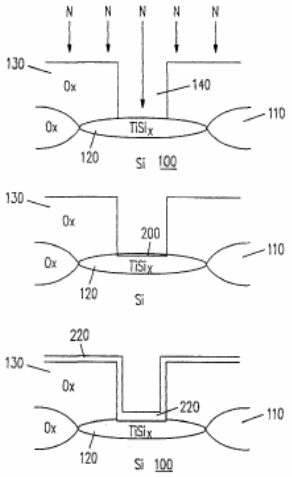
Assistant Examiner—Thomas G. Bilodeau

Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel; Arthur J. Behiel

[57] **ABSTRACT**

A low-resistance contact for use in integrated circuits is formed by creating a titanium silicide layer on a semiconductor body and treating the titanium silicide layer with active free nitrogen to form a surface comprised of titanium nitride. This titanium nitride surface is then overlaid with an additional deposition of titanium nitride. Finally, a layer of conductive metal, such as tungsten, is formed over the second titanium nitride layer by chemical vapor deposition. This process eliminates the need for a titanium-metal deposition step and the defects associated with potential reactions between tungsten hexafluoride gas and titanium metal.

9 Claims, 4 Drawing Sheets

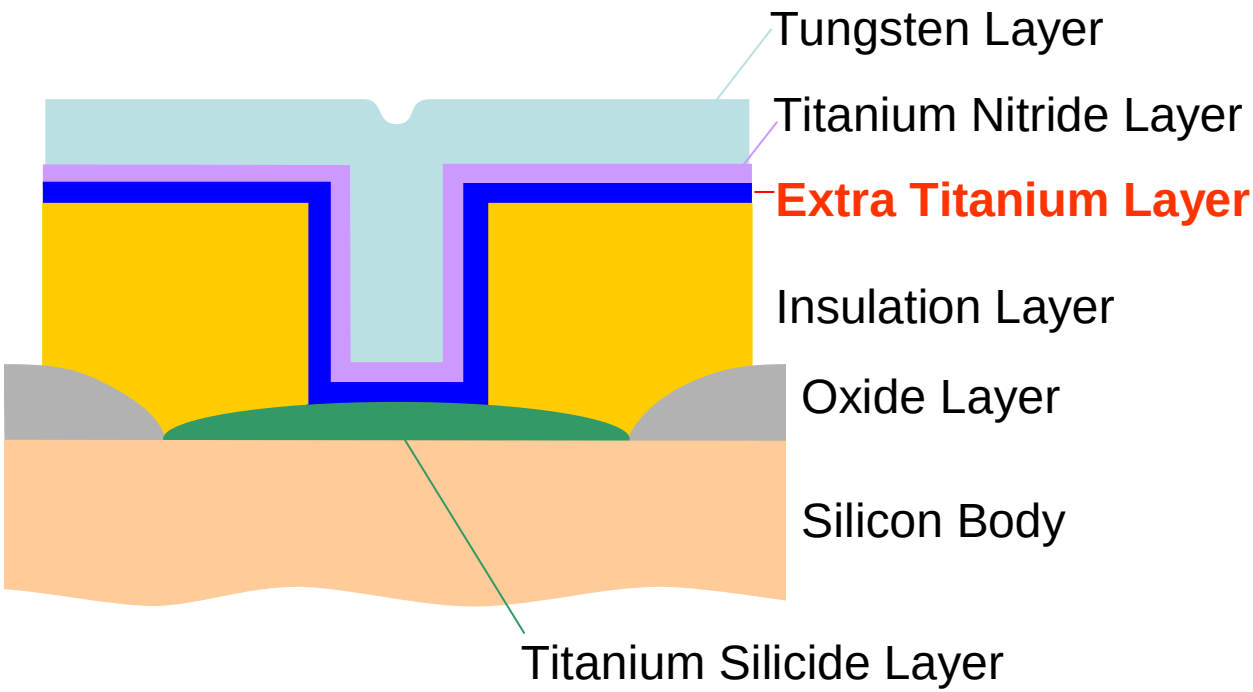


Iacoponi

U.S. Patent No. 5,545,592

Iacoponi: '592 Patent

Before Iacoponi: Extra Titanium Layer



PRIOR ART CONTACT

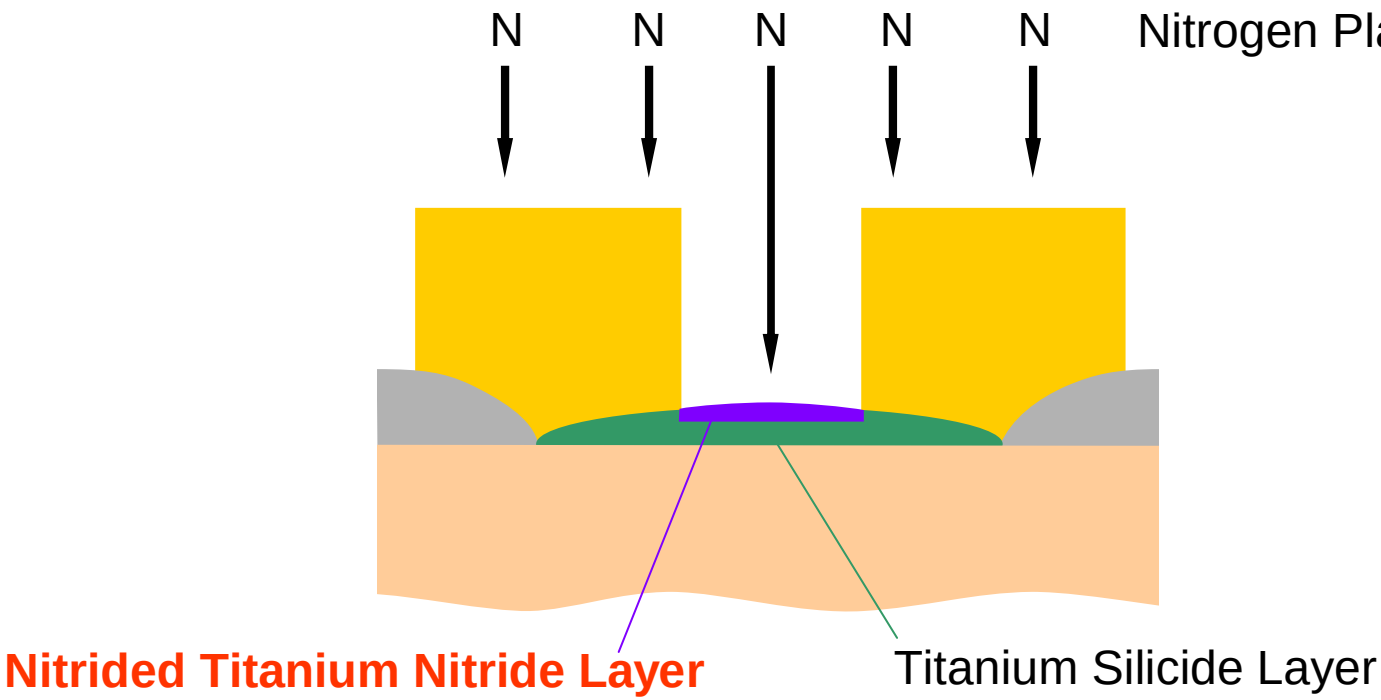
Iacoponi: '592 Patent

Statement of Invention

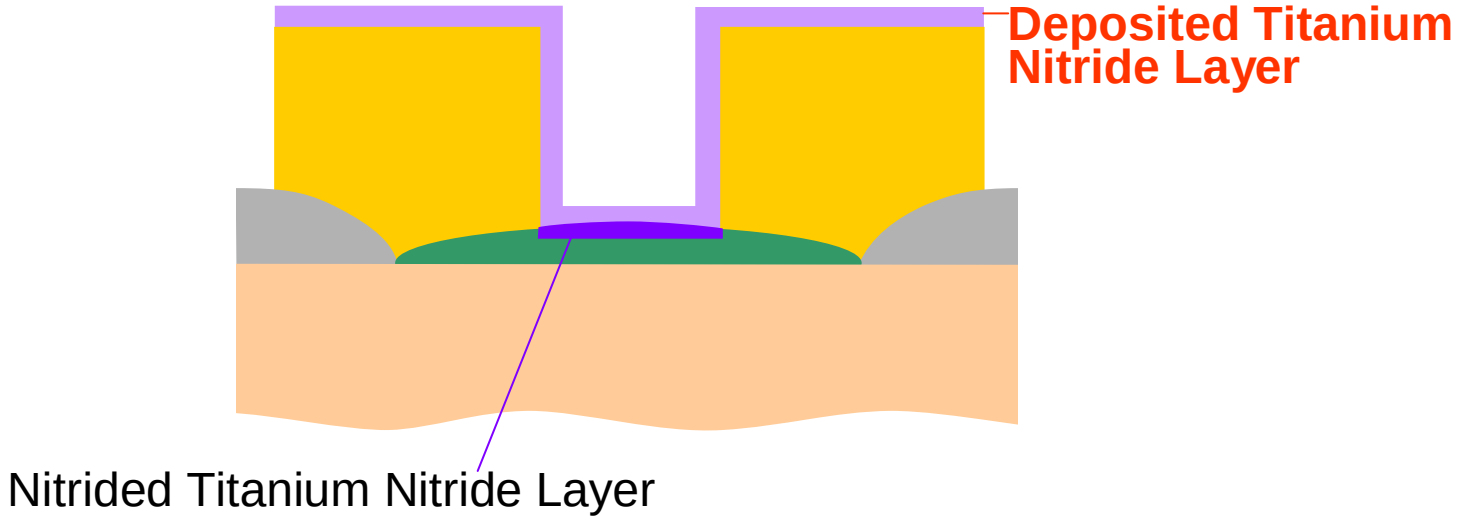
The invention is an improved process for creating a contact without depositing multiple titanium layers. This is accomplished by nitriding the surface of the titanium silicide to create titanium nitride and depositing a titanium nitride layer over it.

Iacoponi: '592 Patent

Nitriding the Titanium Silicide to Create Titanium Nitride

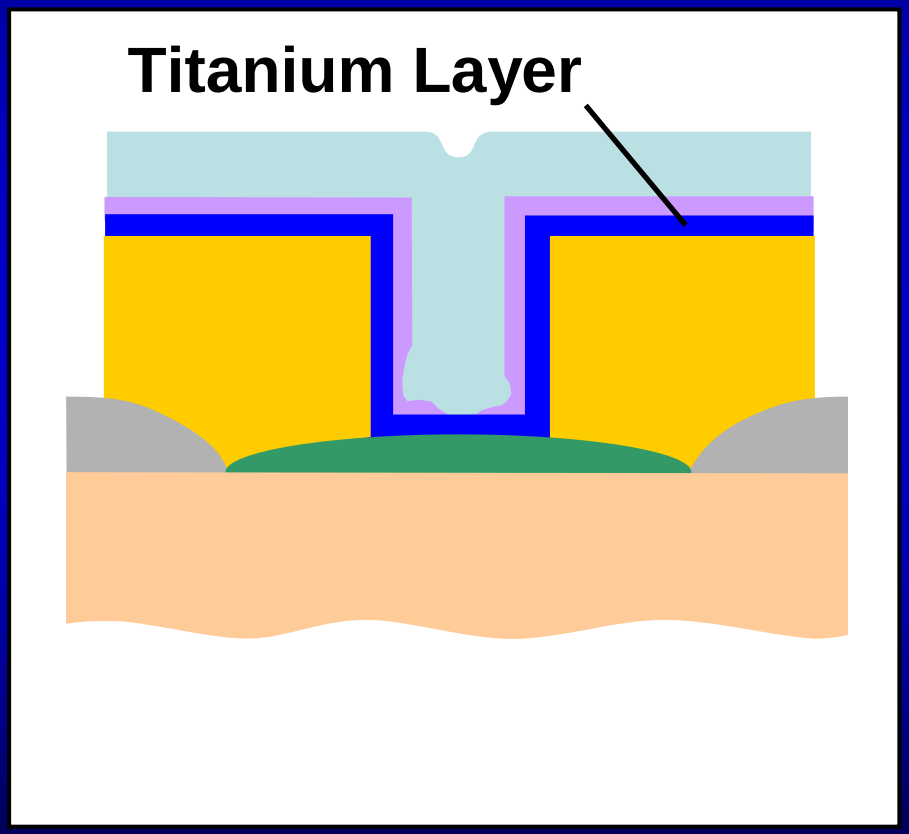


Iacoponi: '592 Patent
Depositing a Titanium Nitride Layer



Iacoponi: '592 Patent
Titanium Layer Eliminated

Prior Art



Iacoponi Invention

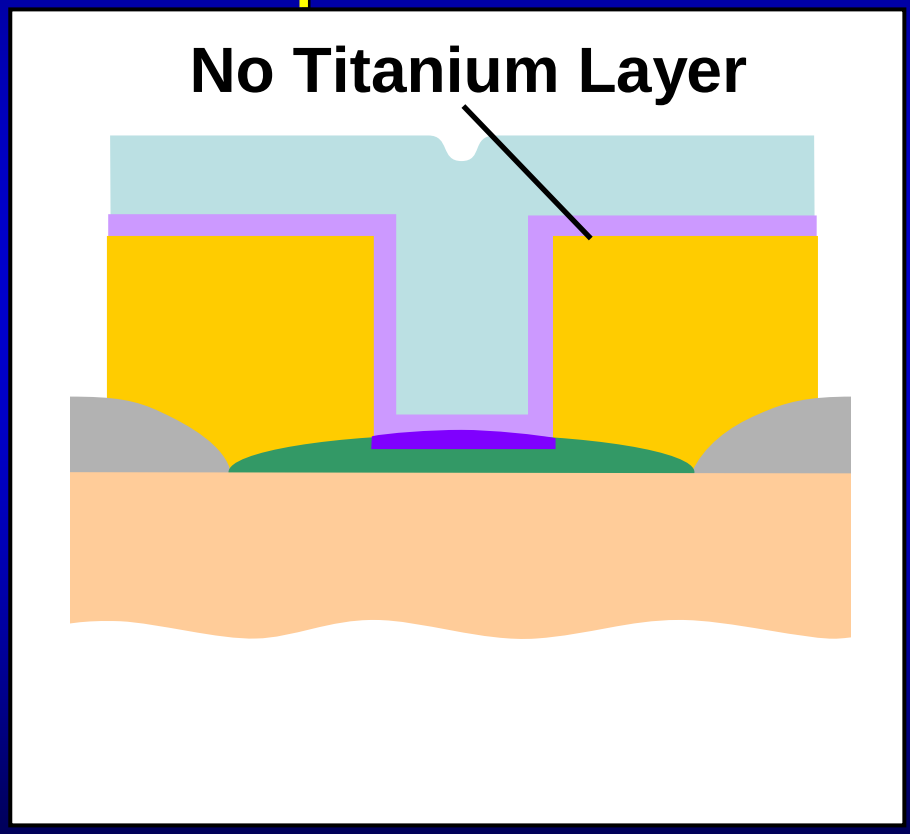


EXHIBIT J

US005623434A

United States Patent [19]

Purcell

[11] **Patent Number: 5,623,434**

[45] **Date of Patent: Apr. 22, 1997**

[54] **STRUCTURE AND METHOD OF USING AN ARITHMETIC AND LOGIC UNIT FOR CARRY PROPAGATION STAGE OF A MULTIPLIER**

[75] Inventor: **Stephen C. Purcell**, Mountain View, Calif.

[73] Assignee: **Chromatic Research, Inc.**, Santa Clara County, Calif.

[21] Appl. No.: **281,377**

[22] Filed: **Jul. 27, 1994**

[51] **Int. Cl.**[6] **G06F 7/52**; G06F 7/50

[52] **U.S. Cl.** **364/757**; 364/736; 364/754; 364/787

[58] **Field of Search** 364/757, 754, 364/758, 759, 760, 736, 755, 756, 768, 784–788

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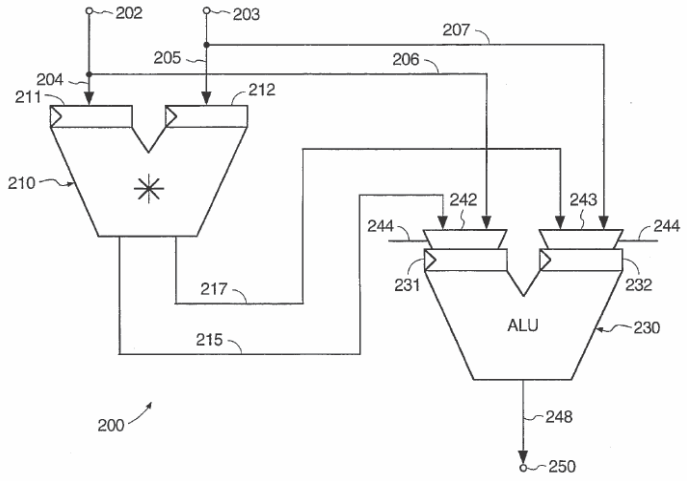
Primary Examiner—Paul P. Gordon
Assistant Examiner—Emmanuel L. Moise
Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel; Alan H. MacPherson; E. Eric Hoffman

[57] **ABSTRACT**

A multiplier circuit for use in a system which includes an arithmetic and logic unit (ALU). The multiplier circuit includes a carry save stage which receives a first data value and a second data value, and in response, creates a carry signal and a sum signal. The carry and sum signals are provided to input leads of the ALU. The ALU is used to add the carry and sum signals to create a third data value which is equal to the product of the first and second data values. In one embodiment, the input leads to the ALU are multiplexed. Thus, one input lead of the ALU receives either the carry signal or a signal from a first input node and the second input lead of the ALU receives either the sum signal or a signal from a second input node.

11 Claims, 5 Drawing Sheets



Purcell

U.S. Patent No. 5,623,434

Purcell: '434 Patent
Background for the Purcell Invention

Structure and method for using an arithmetic and logic unit ("ALU") as the carry propagation stage of a multiplier.

- Computer processors perform basic mathematical functions such as addition and multiplication.
- Traditionally, processors used separate, duplicative circuitry to perform addition and multiplication.

Purcell: '434 Patent
Prior Art

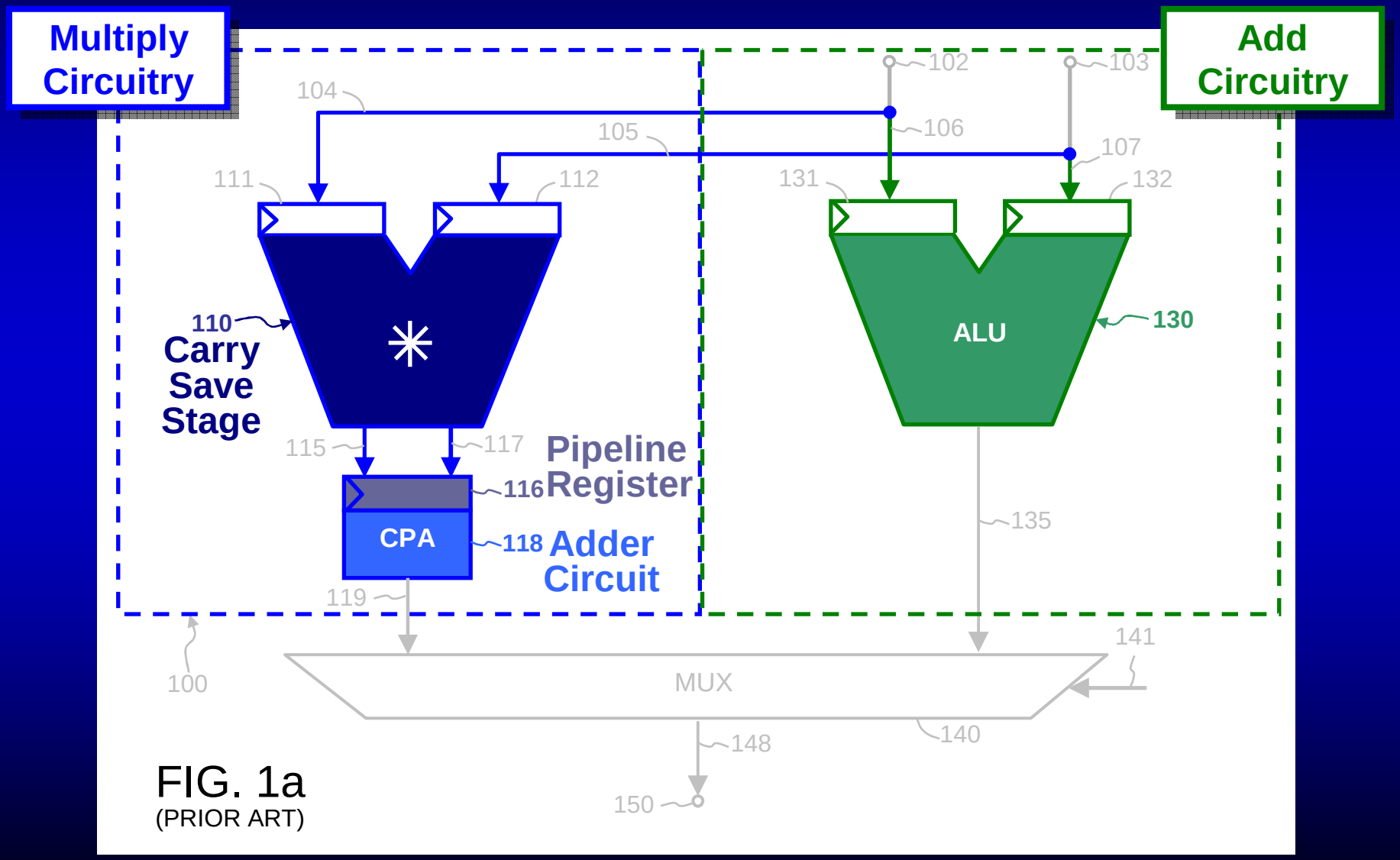


FIG. 1a
(PRIOR ART)

Purcell: '434 Patent

Statement of the Invention

The invention is a novel circuit that requires only one-half of a traditional multiplier circuit connected to an existing ALU to perform a complete multiply operation.

Purcell: '434 Patent
Purcell's Invention

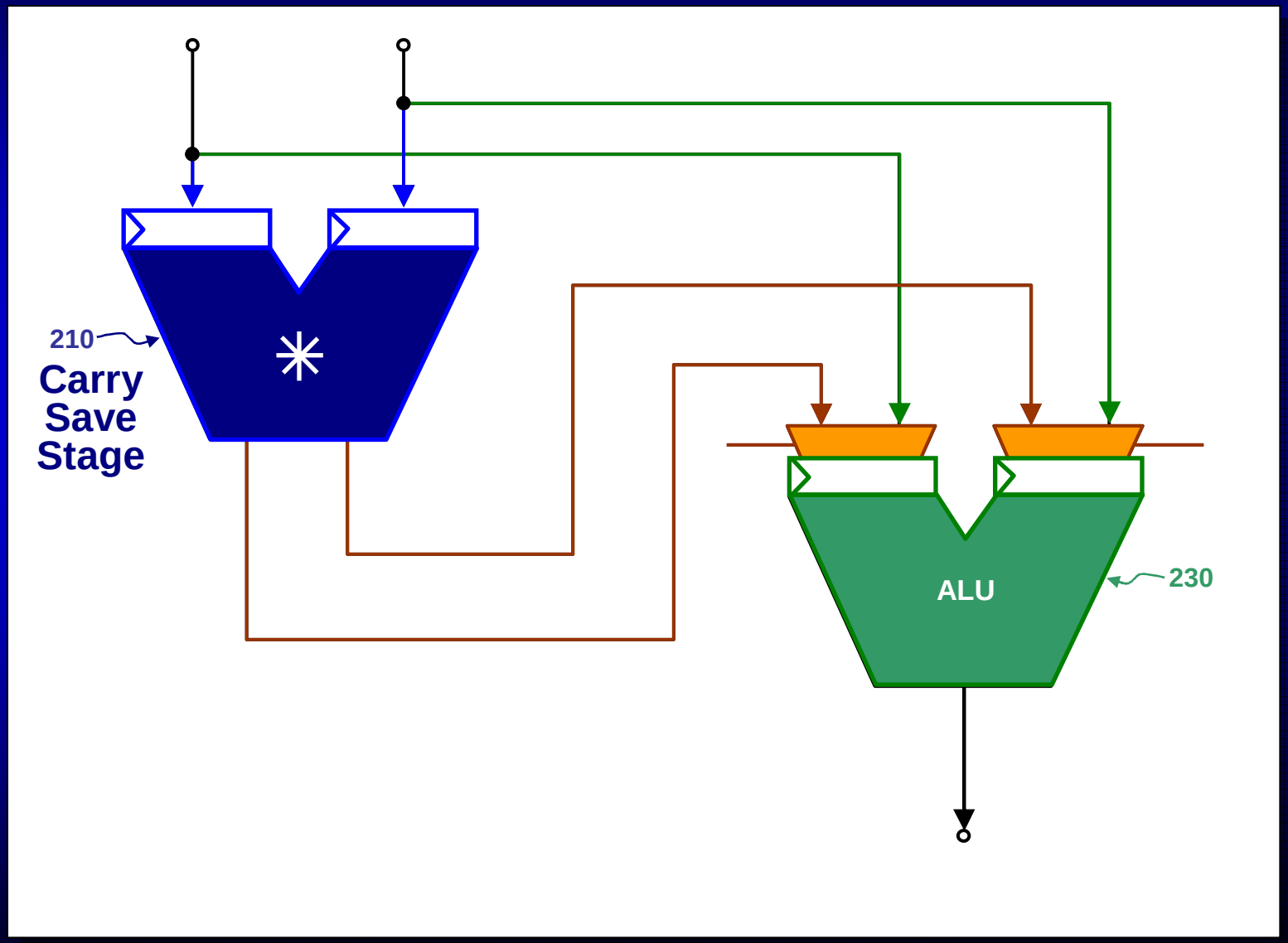


EXHIBIT K

US005377200A

United States Patent [19]

Pedneau

[11] **Patent Number: 5,377,200**

[45] **Date of Patent: Dec. 27, 1994**

[54] **POWER SAVING FEATURE FOR COMPONENTS HAVING BUILT-IN TESTING LOGIC**

[75] Inventor: **Michael D. Pedneau**, Austin, Tex.

[73] Assignee: **Advanced Micro devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **936,896**

[22] Filed: **Aug. 27, 1992**

[51] **Int. Cl.**[5] **H04B 17/00**; G01R 31/02; G06F 1/30

[52] **U.S. Cl.** **371/22.5**; 324/158.1; 395/425; 395/750

[58] **Field of Search** ..... 371/22.1, 22.5, 22.6, 371/15.1, 21.1; 395/275, 750, 650, 425; 370/85.1, 94.1; 324/158 R, 158 SY

[56] **References Cited**

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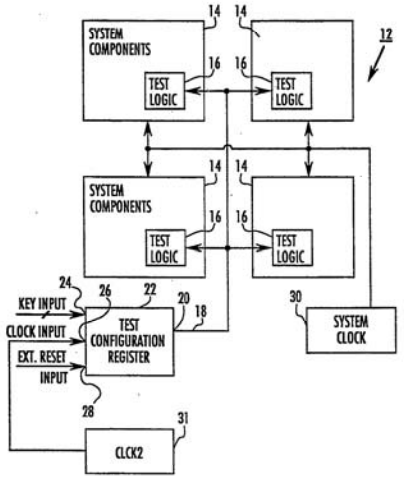
Primary Examiner—Emanuel T. Voeltz
Assistant Examiner—Alan Tran
Attorney, Agent, or Firm—Foley & Lardner

[57] **ABSTRACT**

A configuration register enables built-in testing logic during testing operations, and disables the testing logic during non-testing operations. When enabled, the testing logic is in a normal state, and when disabled the testing logic is in a low power state. The configuration register generates a control signal to the testing logic, the control signal being is responsive to signals received at a key input and a reset input of the configuration register. When the reset input of the configuration register is triggered, the control signal drives the testing logic to the low power state. When a signal matching a predetermined data pattern is applied to the key input, the control signal drives the testing logic to the normal state.

24 Claims, 3 Drawing Sheets



Pedneau

U.S. Patent No. 5,377,200

Pedneau: '200 Patent
Technology

Power-saving feature for processors having testing logic.

- Testing logic is used during product design to work out bugs and streamline the manufacturing process.
- Testing logic is used during the manufacturing process to improve yield (percent of products with no defects).
- Testing logic consumes power.

Pedneau: '200 Patent

The Problem the Invention Addresses

- In the prior art, the testing logic was always powered even though it was used only a miniscule percentage of the time. This was a waste of power.

Pedneau: '200 Patent

Statement of the Invention

The invention is a system for controlling the power consumed by testing logic so that it consumes minimal power when not being utilized.

Pedneau: '200 Patent

Pedneau's Invention

Key Input Activated – Test Circuitry in Normal Power State

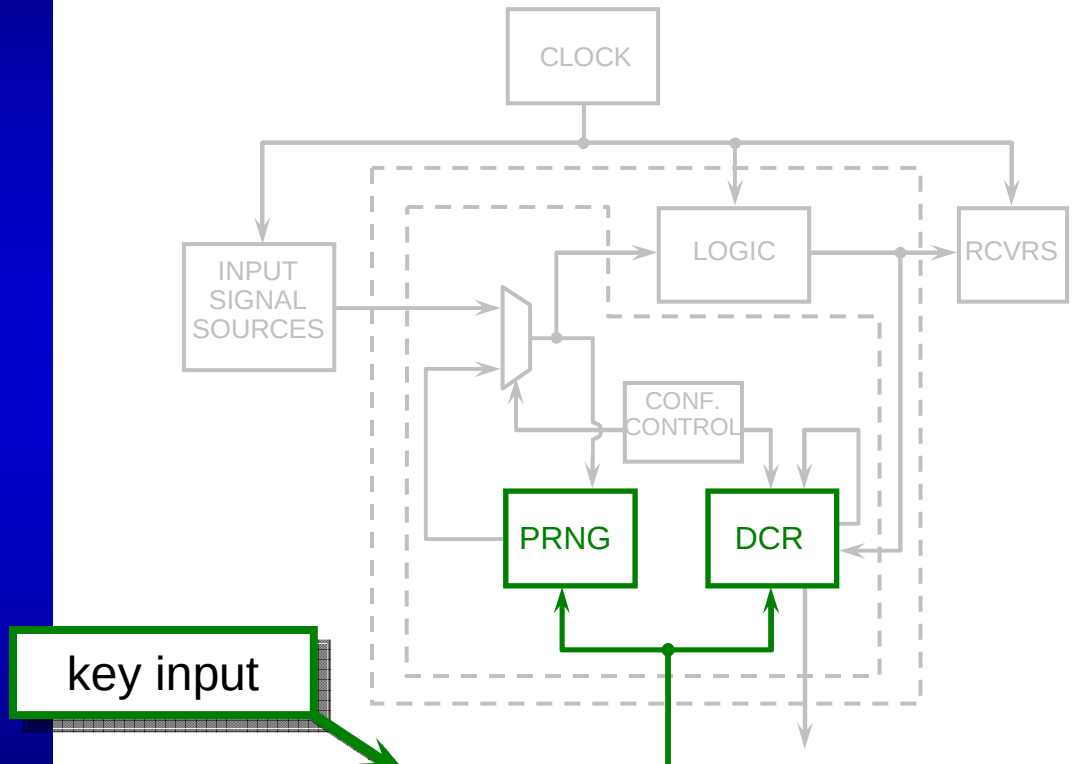


FIG. 2

Pedneau: '200 Patent

Pedneau's Invention

Reset Input Activated – Test Circuitry in Low Power State

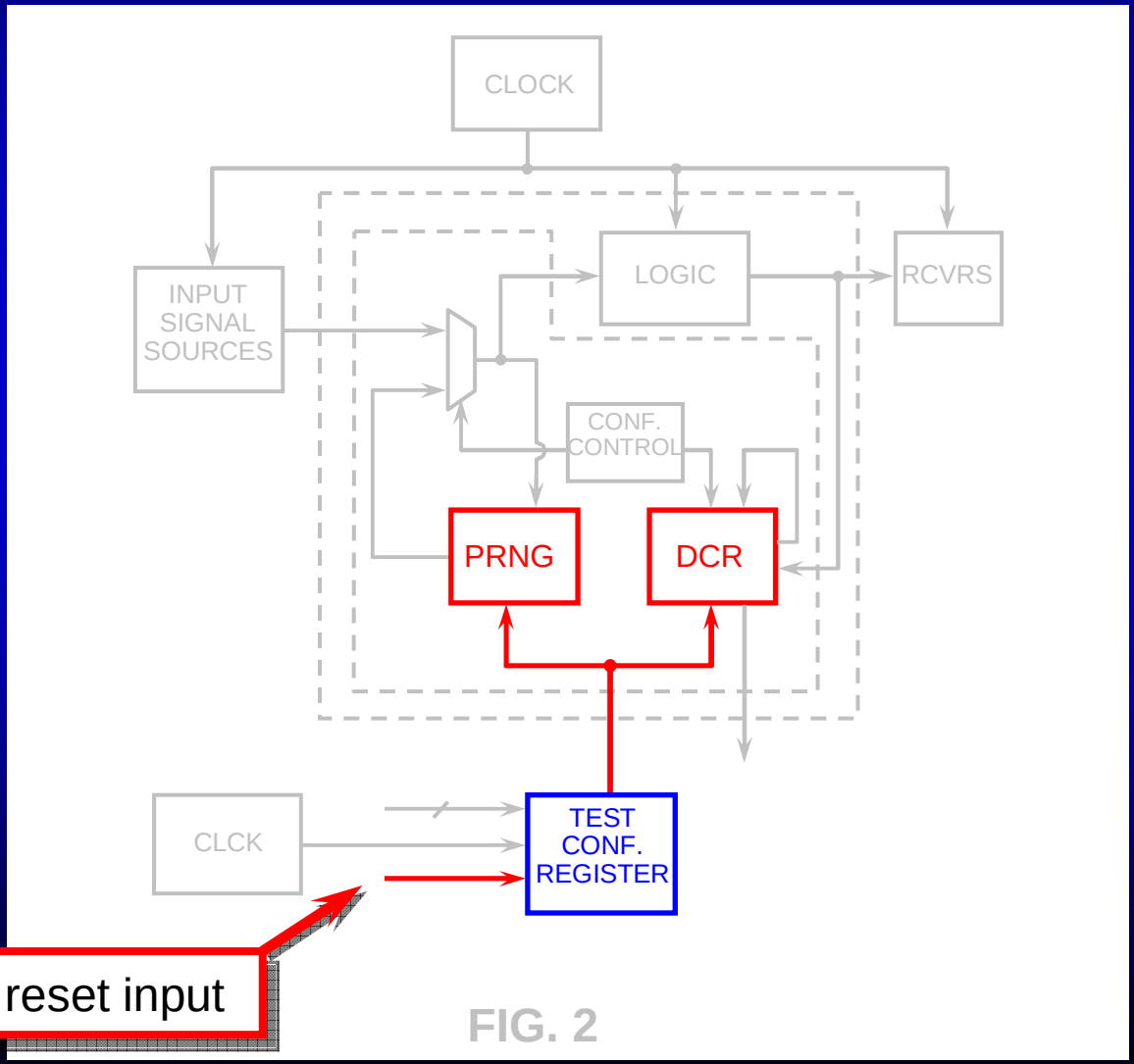


FIG. 2

EXHIBIT L

US006784879B1

(12) **United States Patent**
Orr

(10) **Patent No.: US 6,784,879 B1**
(45) **Date of Patent: Aug. 31, 2004**

(54) **METHOD AND APPARATUS FOR PROVIDING CONTROL OF BACKGROUND VIDEO**

(75) Inventor: **Stephen Jonathan Orr**, East York (CA)

(73) Assignee: **ATI Technologies Inc.**, Markham (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/892,472**

(22) Filed: **Jul. 14, 1997**

(51) **Int. Cl.**[7] **G09G 5/00**
(52) **U.S. Cl.** **345/212**; 345/204
(58) **Field of Search** 345/205, 211, 345/348, 327, 352, 354, 629, 630, 634, 581, 204, 212, 214; 348/563, 564, 565, 569, 570; 725/39, 40, 49

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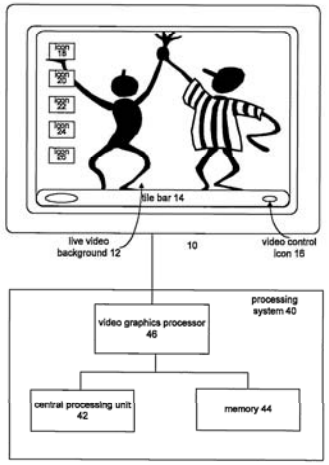
Primary Examiner—Vijay Shankar
(74) *Attorney, Agent, or Firm*—Vedder, Price, Kaufman & Kammholz, P.C.

(57) **ABSTRACT**

A method and apparatus for controlling background video on a computer display is accomplished by providing a video control icon, which is visible on the display. The video control icon relates to the live video being displayed as the background. Once selection of the video control icon has been detected, the computer displays a control panel for the live video while the live video remains in the background. As such, when a user desires to change an attribute of the live video, the user selects the video control icon which pops up a control panel. The user then makes an adjustment via the control panel to the live video and once such an adjustment is made, the control panel is removed from the screen. All this done while the live video remains in the background, thus other applications that were in focus remain in focus.

24 Claims, 3 Drawing Sheets



Orr

U.S. Patent No. 6,784,879

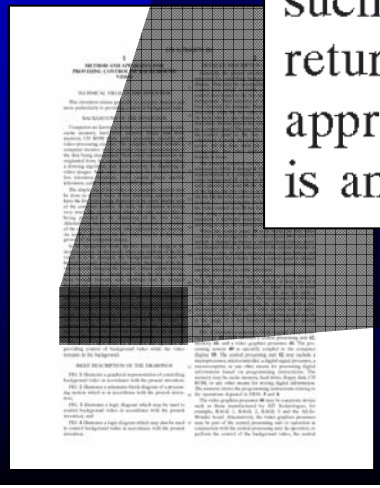
Orr: '879 Patent
Background for the Orr Invention

Method and apparatus for providing control of background video.

- Many consumer electronics products display video.
- Consumer products provide user interfaces for controlling the displayed video.
- A user may view two different applications on the same screen – one in the foreground (such as a battery meter) and one in the background (such as live video).

Orr: '879 Patent
Problems with the Prior Art

Prior art systems could not control background video without losing focus on foreground applications:



When an attribute of the live video is to be changed, other applications that were in focus (i.e., actively being displayed and/or being worked upon) must go into a background mode (i.e., taken out of focus). As such, the adjusting of attributes of the live video consume the activity of the computer until such attributes have been changed and the live video is returned to the background mode. As one can readily appreciate, this can be somewhat burdensome to the user and is an ineffective use of the computer system.

Orr: '879 Patent

Statement of the Invention

The invention is a video graphics processing system that allows control of background video without obscuring a foreground application.

Orr: '879 Patent

Orr Allows Focus to Remain on Foreground Applications While Controlling Background Video

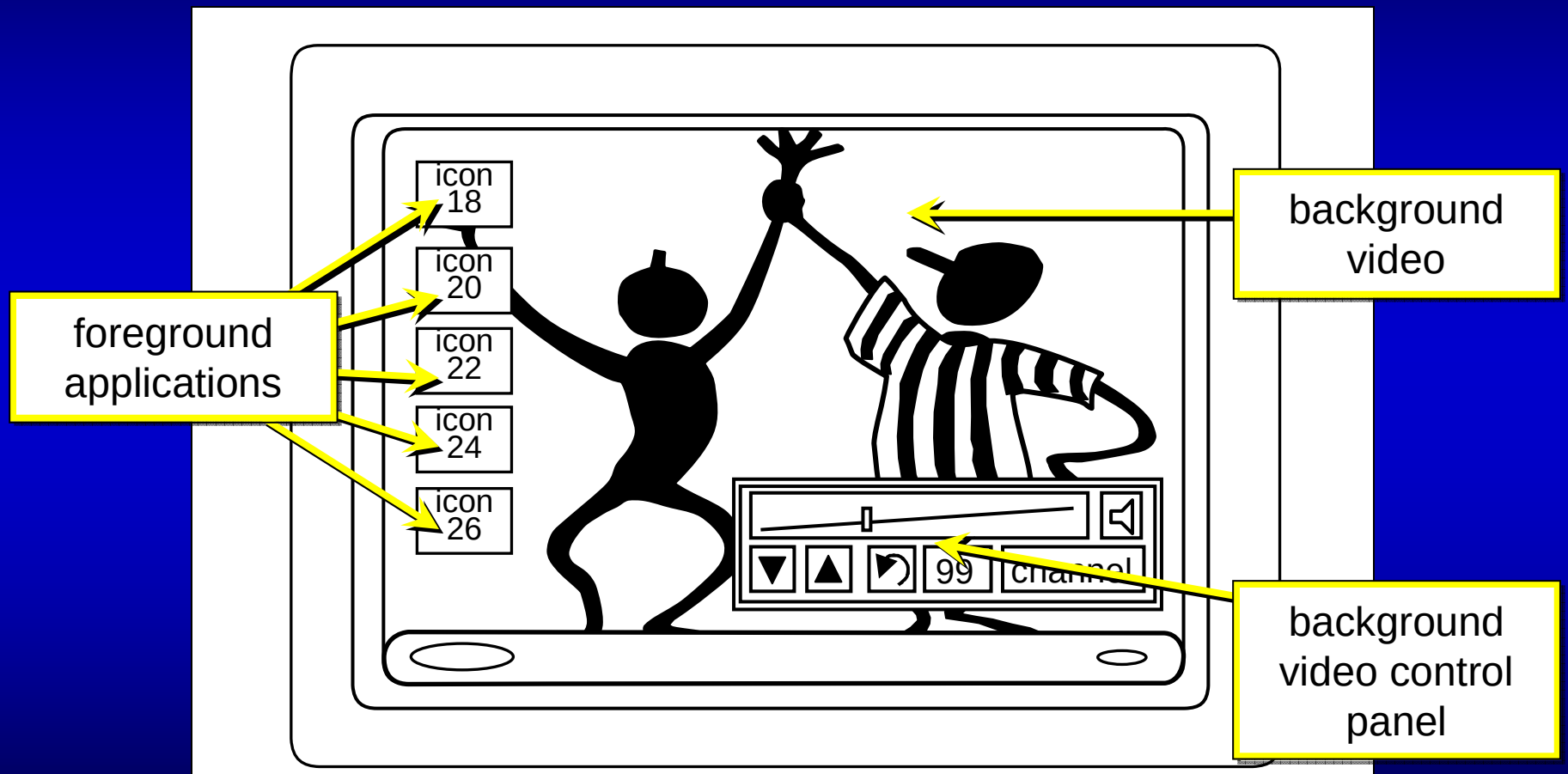


Figure 1